An analytical model for the drain–source breakdown voltage of RF LDMOS power transistors with a Faraday shield

Zhang Wenmin(张文敏)[1,†], Zhang Wei(张为)[1], Fu Jun(付军)[2], and Wang Yudong(王玉东)[2]

[1]School of Electronic Information Engineering, Tianjin University, Tianjin 300072, China
[2]Institute of Microelectronics, Tsinghua University, Beijing 100084, China

Abstract: An analytical model for the drain–source breakdown voltage of an RF LDMOS power transistor with a Faraday shield is derived on the basis of the solution of the 2D Poisson equation in a p-type epitaxial layer, as well as an n-type drift region by means of parabolic approximation of electrostatic potential. The model captures the influence of the p-type epitaxial layer doping concentration on the breakdown voltage, compared with the previously reported model, as well as the effect of the other device parameters. The analytical model is validated by comparing with a numerical device simulation and the measured characteristics of LDMOS transistors. Based on the model, optimization of LDMOS device parameters to achieve proper trade-off between the breakdown voltage and other characteristic parameters such as on-resistance and feedback capacitance is analyzed.

Key words: RF LDMOSFET; Faraday shield; breakdown voltage; surface electrical field; drift region
DOI: 10.1088/1674-4926/33/4/044001 **EEACC:** 2530F; 2560B; 2560P

1. Introduction

Currently, radio frequency laterally diffused metal oxide semiconductor (RF LDMOS) power transistors are widely used in power amplifiers (PAs) for wireless base-stations, television/broadcast and radar applications. High output power and good linearity are very important for power transistors to achieve high efficiency operation. As the drain–source breakdown voltage (BV_{DS}) will limit the maximum voltage swing and greatly affect the linearity of RF LDMOS power transistors, the linearity and output power requirements for PA applications make it necessary to maintain a sufficiently high breakdown voltage.

In the practical design, there have been many methods used for increasing breakdown voltage. Apples and Vaes suggested the reduced surface field (RESURF) concept[1]. The RESURF concept can be used to realize a uniformly distributed electrical field across the silicon surface in the drift region and achieve a high breakdown voltage for RF LDMOS power transistors. Furthermore, double RESURF implements an extra p-doped layer in the surface of the drift region[2]. The Faraday shield is another widely used technique in RF LDMOS power transistors. Adding a separate electrode (Faraday shield) above the drift region may improve the breakdown voltage and decrease the gate-drain capacitance[3]. Other methods, such as the multi-resistivity drift region technique[4] and p-top[5], have also been proposed to increase the breakdown voltage.

Many works have discussed and studied the analytical breakdown voltage model[6−8], but they have been either too simple or based on the approximate 1D Poisson equation solution. He *et al.* reported an analytical model of surface field distribution and breakdown voltage for an RESURF LDMOS transistor based on an approximate solution of the 2D Poisson equation in the drift region[9]. Chen *et al.* extended the model to an LDMOS with a Faraday shield[10]. However, both works ignored the influence of the doping concentration of the p^- substrate or p^- epitaxial layer on breakdown voltage.

In this paper, we have derived a closed form analytical model of the source–drain breakdown voltage for RF LDMOS power transistors with a Faraday shield by solving the Poisson equation in the p-epitaxial layer as well as in the n-drift region based on a parabolic approximation of electrostatic potential.

The breakdown voltages calculated by the presented analytical model show a good agreement with the numerical simulation results given by the Sentaurus TCAD simulator and the experimental data. The dependence of the breakdown voltage on the device and process parameters, such as the drift region length, the Faraday shield length, the doping concentration of the drift region and the p-epitaxial layer has been discussed and analyzed in detail. Based on the model, optimization of breakdown voltage and other characteristic parameters, such as on-resistance and feedback capacitance for the RF LDMOS power transistors, is analyzed.

2. Model derivation

Figure 1 shows the cross section of the n-channel RF LDMOS power transistor with a Faraday shield investigated during this work. It includes a p^+ sink to connect the source to the substrate contact. A part of the n^+ poly gate and the n^- drift region is covered with the Faraday shield metal layer with an isolating oxide layer in-between. The device is biased in the off-state configuration, with substrate and gate grounded and drain biased at a positive voltage V_{DS}. Normally, the Faraday shield is connected to the source, which is grounded in common source configuration, to reduce feedback capacitance C_{GD} and thus improve the device linearity by screening the poly gate electrode from the drain metal[11]. So in this work the shield is biased at 0 V for the following modeling derivation and numerical device simulation. Breakdown is thought to occur when

† Corresponding author. Email: tjumin@126.com
Received 30 August 2011, revised manuscript received 25 October 2011

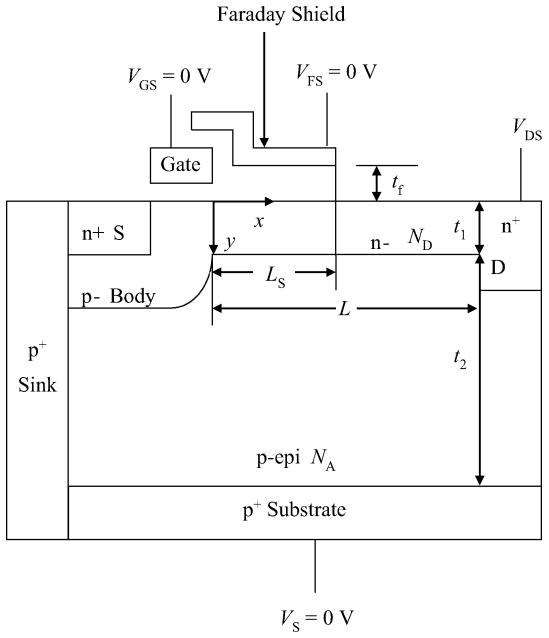

Fig. 1. Cross section of the n-channel RF LDMOS power transistor with Faraday shield.

the maximum surface electrical field reaches the silicon critical field (2.5×10^5 V/cm), and at this moment the applied drain bias V_{DS} is defined as the breakdown voltage BV_{DS}. At the breakdown point, it would be reasonable to assume that both the n^- drift region and the p-epitaxial region under the drift region are fully depleted.

The drift region length L is defined as the lightly doped n^- region length between the heavily doped n^+ drain region and the channel region. L_S is the overlap length of the Faraday shield above the drift region. t_1 and t_2 are the thickness of the n^- drift region and p-epitaxial layer, respectively. t_f is the thickness of oxide layer between the Faraday shield and the drift region. The drift region and the epitaxial layer are assumed to be uniformly doped with impurity concentration of N_D and N_A, respectively.

Since both the drift region and the epitaxial layer under the drift region can be reasonably assumed to be fully depleted under the breakdown bias condition, according to the Poisson equation, the electrostatic potential distribution in the drift region and epitaxial layer can be given by

$$\frac{\partial^2\phi_1(x,y)}{\partial x^2}+\frac{\partial^2\phi_1(x,y)}{\partial y^2}=-\frac{qN_D}{\varepsilon_{si}}, \quad 0\leqslant x\leqslant L, 0\leqslant y\leqslant t_1, \tag{1}$$

$$\frac{\partial^2\phi_2(x,y)}{\partial x^2}+\frac{\partial^2\phi_2(x,y)}{\partial y^2}=\frac{qN_A}{\varepsilon_{si}}, \quad 0\leqslant x\leqslant L, t_1\leqslant y\leqslant t_1+t_2, \tag{2}$$

where $\phi_1(x,y)$ is the potential function in the drift region, $\phi_2(x,y)$ is the potential function in the p-epitaxial layer, and q, ε_{si} are elementary electronic charge and dielectric constant of silicon, respectively.

It is possible to convert the 2D Poisson equation into a 1D equation describing the surface potential in the lateral coordinate x through potential parabolic approximation. In this work, we approximate the y dependence of $\phi(x,y)$ by a simple parabolic function as[12]

$$\phi_1(x,y)=c_0(x)+c_1(x)y+c_2(x)y^2, \tag{3}$$

$$\phi_2(x,y)=d_0(x)+d_1(x)(y-t_1)+d_2(x)(y-t_1)^2, \tag{4}$$

where the coefficients $c_i(x)$ $(i=0,1,2)$ and $d_i(x)$ $(i=0,1,2)$ are functions of x only.

The boundary conditions for the potential functions are

$$\phi_f(x)=\phi_1(x,0), \tag{5}$$

$$\phi_b(x)=\phi_2(x,t_1+t_2)=0, \tag{6}$$

$$\left.\frac{d\phi_1(x,y)}{dy}\right|_{y=0}=\begin{cases}\dfrac{\varepsilon_{ox}}{\varepsilon_{si}}\dfrac{\phi_f+V_{FB}}{t_f}, & 0\leqslant x\leqslant L_S,\\ \approx 0, & L_S<x\leqslant L,\end{cases} \tag{7}$$

$$\phi_1(x,t_1)=\phi_2(x,t_1), \tag{8}$$

$$\left.\frac{d\phi_1(x,y)}{dy}\right|_{y=t_1}=\left.\frac{d\phi_2(x,y)}{dy}\right|_{y=t_1}, \tag{9}$$

$$V_{FB}=W_{MS}-\frac{Q_{OX}}{C_{OX}}=W_M-W_S-\frac{Q_{OX}}{C_{OX}}, \tag{10}$$

$$C_{OX}=\frac{\varepsilon_{ox}}{t_f}, \tag{11}$$

where $\phi_f(x)$ is the drift region surface potential, ε_{ox} is the dielectric constant of oxide, V_{FB} is the flatband voltage dependent on the oxide charge and the workfunction difference between the Faraday shield metal and silicon, W_M and W_S are the workfunctions of the Faraday shield metal and the n-type drift region, respectively. Q_{OX} is areal density of the fixed oxide charge. Equation (7) is obtained from the continuity of the electric field at the Si/SiO_2 interface, Equations (8) and (9) stem from the continuity of the potential and electrical field at the n-/p- interface, respectively.

As for V_{FB}, firstly, Q_{OX} is here assumed to be in the order of 1×10^{10} cm^{-2}. Secondly, it should be noted that titanium, whose workfunction is 4.33 eV, is used as the Faraday metal in this work for the device fabrication. Thirdly, about 4.25 eV can be taken for the workfunction of the n-type silicon drift region. Lastly, t_f is at most a few tenths of micron. Therefore, according to Eq. (10), when the device is near breakdown, over the most part of the drift region surface the V_{FB} value can be estimated to be much smaller than ϕ_f which is greatly elevated by the high drain bias voltage. This will be confirmed later by the simulated surface potential distribution shown in Fig. 2.

As a result, V_{FB} can be reasonably neglected compared with ϕ_f, just as done in Refs. [9, 10], Equation (7) can be simplified into

$$\left.\frac{d\phi_1(x,y)}{dy}\right|_{y=0}\approx\begin{cases}\dfrac{\varepsilon_{ox}}{\varepsilon_{si}}\dfrac{\phi_f}{t_f}, & 0\leqslant x\leqslant L_S\\ 0, & L_S<x\leqslant L.\end{cases} \tag{12}$$

Combining Eqs. (1)–(12), the following 1D ordinary differential equation can be derived from the two 2D partial differential Poisson equations.

$$\frac{\mathrm{d}^2\phi_{\mathrm{f}}(x)}{\mathrm{d}x^2} - \alpha\phi_{\mathrm{f}}(x) = \beta, \tag{13}$$

where

$$\alpha = \begin{cases} \alpha_1 = \dfrac{2}{t_1^2 + 2t_1t_2} + \dfrac{2\varepsilon_{\mathrm{ox}}(t_1+t_2)}{\varepsilon_{\mathrm{si}}t_{\mathrm{f}}\left(t_1^2+2t_1t_2\right)}, & 0 \leqslant x \leqslant L_{\mathrm{S}}, \\ \alpha_2 = \dfrac{2}{t_1^2+2t_1t_2}, & L_{\mathrm{S}} < x \leqslant L, \end{cases} \tag{14}$$

$$\beta = -\frac{qN_{\mathrm{D}}}{\varepsilon_{\mathrm{si}}} + \frac{qN_{\mathrm{A}}t_2^2}{\varepsilon_{\mathrm{si}}\left(t_1^2+2t_1t_2\right)}. \tag{15}$$

Solving Eq. (13) with the boundary conditions of $\phi_{\mathrm{f}}(0) = 0$, $\phi_{\mathrm{f}}(L_{\mathrm{S}}) = V_{\mathrm{LS}}$ and $\phi_{\mathrm{f}}(L) = V_{\mathrm{DS}}$, the surface potential is given as

$$\phi_{\mathrm{f}}(x) = \begin{cases} \theta_1 + \dfrac{(V_{\mathrm{LS}}-\theta_1)\sinh\dfrac{x}{\tau_1} - \theta_1\sinh\dfrac{L_{\mathrm{S}}-x}{\tau_1}}{\sinh\dfrac{L_{\mathrm{S}}}{\tau_1}}, \\ \qquad 0 \leqslant x \leqslant L_{\mathrm{S}}, \\ \theta_2 + \\ \dfrac{(V_{\mathrm{DS}}-\theta_2)\sinh\dfrac{x-L_{\mathrm{S}}}{\tau_2} + (V_{\mathrm{LS}}-\theta_2)\sinh\dfrac{L-x}{\tau_2}}{\sinh\dfrac{L-L_{\mathrm{S}}}{\tau_2}}, \\ \qquad L_{\mathrm{S}} < x \leqslant L, \end{cases} \tag{16}$$

where $\theta_{\mathrm{i}} = -\frac{\beta}{\alpha_{\mathrm{i}}}$ and $\tau_{\mathrm{i}} = \left(\frac{1}{\alpha_i}\right)^{1/2}$ are introduced ($i = 1, 2$).

Equation (16) indicates that the surface potential is closely related to the doping concentrations of the drift region and epitaxial layer, i.e. N_{D} and N_{A}, as well as to the drift region length L and the Faraday shield overlap length L_{S}.

The magnitude of the drift region surface field is obtained by differentiating Eq. (16) with respect x as

$$E_{\mathrm{f}}(x) = \frac{\mathrm{d}\phi_{\mathrm{f}}(x)}{\mathrm{d}x} = \begin{cases} \dfrac{(V_{\mathrm{LS}}-\theta_1)\cosh\dfrac{x}{\tau_1} + \theta_1\cosh\dfrac{L_{\mathrm{S}}-x}{\tau_1}}{\tau_1\sinh\dfrac{L_{\mathrm{S}}}{\tau_1}}, \\ \qquad 0 \leqslant x \leqslant L_{\mathrm{S}}, \\ \dfrac{(V_{\mathrm{DS}}-\theta_2)\cosh\dfrac{x-L_{\mathrm{S}}}{\tau_2} - (V_{\mathrm{LS}}-\theta_2)\cosh\dfrac{L-x}{\tau_2}}{\tau_2\sinh\dfrac{L-L_{\mathrm{S}}}{\tau_2}}, \\ \qquad L_{\mathrm{S}} < x \leqslant L, \end{cases} \tag{17}$$

According to the continuity of $E_{\mathrm{f}}(x)$ at $x = L_{\mathrm{S}}$, V_{LS} can be expressed as

$$\begin{aligned} V_{\mathrm{LS}} = {} & \left[\tau_1(V_{\mathrm{DS}}-\theta_2)\operatorname{csc\,h}\frac{L-L_{\mathrm{S}}}{\tau_2} + \tau_1\theta_2\coth\frac{L-L_{\mathrm{S}}}{\tau_2}\right. \\ & \left. + \tau_2\theta_1\left(\coth\frac{L_{\mathrm{S}}}{\tau_1} - \operatorname{csc} h\frac{L_{\mathrm{S}}}{\tau_1}\right)\right] \\ & \times\left(\tau_2\coth\frac{L_{\mathrm{S}}}{\tau_1} + \tau_1\coth\frac{L-L_{\mathrm{S}}}{\tau_2}\right)^{-1}. \end{aligned} \tag{18}$$

As confirmed by the following calculation and simulation results, the drift region surface electrical field peaks are always located at the Faraday shield edge or drain edge as $E_{\mathrm{f}}(L_{\mathrm{S}})$ and $E_{\mathrm{f}}(L)$, respectively, which can be derived as below by substituting $x = L_{\mathrm{S}}$ and $x = L$ into Eq. (17), respectively.

$$E_{\mathrm{f}}(L_{\mathrm{S}}) = \frac{(V_{\mathrm{DS}}-\theta_2) - (V_{\mathrm{LS}}-\theta_2)\cosh\dfrac{L-L_{\mathrm{S}}}{\tau_2}}{\tau_2\sinh\dfrac{L-L_{\mathrm{S}}}{\tau_2}}, \tag{19}$$

$$E_{\mathrm{f}}(L) = \frac{(V_{\mathrm{DS}}-\theta_2)\cosh\dfrac{L-L_{\mathrm{S}}}{\tau_2} - (V_{\mathrm{LS}}-\theta_2)}{\tau_2\sinh\dfrac{L-L_{\mathrm{S}}}{\tau_2}}. \tag{20}$$

When breakdown occurs at the shield end ($x = L_{\mathrm{S}}$), by equating Eq. (19) with the critical electrical field E_{C}, the V_{DS} can be solved for as $\mathrm{BVL_S}$.

$$\begin{aligned} \mathrm{BVL_S} = {} & E_{\mathrm{C}}\left(\tau_2\sinh\frac{L-L_{\mathrm{S}}}{\tau_2} + \tau_1\tanh\frac{L_{\mathrm{S}}}{\tau_1}\cosh\frac{L-L_{\mathrm{S}}}{\tau_2}\right) \\ & + \theta_1\cosh\frac{L-L_{\mathrm{S}}}{\tau_2}\left(1-\operatorname{sec} h\frac{L_{\mathrm{S}}}{\tau_1}\right) \\ & + \theta_2\left(1-\cosh\frac{L-L_{\mathrm{S}}}{\tau_2}\right). \end{aligned} \tag{21}$$

When breakdown occurs at drift region end ($x = L$), and vice versa, by equating Eq. (20) with E_{C}, the V_{DS} can be solved for as BVL.

$$\begin{aligned} \mathrm{BVL} = {} & \frac{1}{\tau_1\sinh\dfrac{L-L_{\mathrm{S}}}{\tau_2} + \tau_2\cosh\dfrac{L-L_{\mathrm{S}}}{\tau_2}\coth\dfrac{L_{\mathrm{S}}}{\tau_1}} \\ & \times\left[E_{\mathrm{c}}\tau_2\sinh\frac{L-L_{\mathrm{S}}}{\tau_2}\left(\tau_2\coth\frac{L_{\mathrm{S}}}{\tau_1} + \tau_1\coth\frac{L-L_{\mathrm{S}}}{\tau_2}\right)\right. \\ & + \theta_1\tau_2\left(\coth\frac{L_{\mathrm{S}}}{\tau_1} - \operatorname{csc} h\frac{L_{\mathrm{S}}}{\tau_1}\right) - \theta_2\left(\tau_1\operatorname{csc} h\frac{L-L_{\mathrm{S}}}{\tau_2}\right. \\ & + \tau_2\coth\frac{L_{\mathrm{S}}}{\tau_1} - \tau_1\cosh\frac{L-L_{\mathrm{S}}}{\tau_2}\coth\frac{L-L_{\mathrm{S}}}{\tau_2} \\ & \left.\left. -\tau_2\cosh\frac{L-L_{\mathrm{S}}}{\tau_2}\coth\frac{L_{\mathrm{S}}}{\tau_1}\right)\right]. \end{aligned} \tag{22}$$

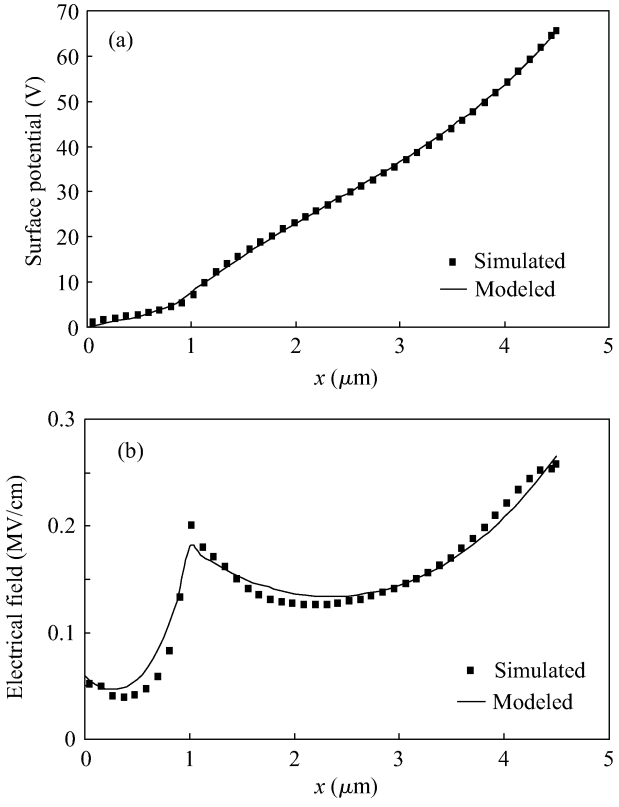

Fig. 2. (a) Surface potential distribution along the lateral distance and (b) surface electrical field distribution along the lateral distance for the RF LDMOS power transistor. $N_D = 1 \times 10^{16}$ cm^{-3}, $N_A = 1 \times 10^{15}$ cm^{-3}, $L = 4.5$ μm, $L_S = 1$ μm, $t_f = 0.08$ μm, $t_1 = 0.6$ μm, $t_2 = 4.2$ μm, $V_{DS} = 65$ V.

Being defined as the drain–source voltage at which either of the two peak fields reaches E_C, BV_{DS} can be taken as the smaller one of BVL_S and BVL.

$$BV_{DS} = \min(BVL_S, BVL). \tag{23}$$

Finally, Equations (21) and (22) constitute the analytical model of the drain–source breakdown voltage for the RF LDMOS power transistors. Compared with the previous models presented by He[9] and Chen[10], the model proposed in this work is an improvement in at least two aspects. Firstly, the dependence of BV_{DS} on N_A is explicitly described (see Eq. (15)) owing to a consideration of the Poisson equation in the p-epitaxial layer in addition to the n^- drift region. Secondly, through an appropriate mathematical derivation, the analytical BV_{DS} model is finally given in an explicit closed from. Of course, as no charge carriers are included in Poisson equations (1) and (2), on which our model is based, full depletion in both the n-drift region and the p-epitaxial layer is a prerequisite for the model. Fortunately, when the RF LDMOS is at the onset of drain–source breakdown, on the one hand, usually V_{DS} is high enough to fully deplete the p-epitaxial layer as well as the n^- drift region, and, on the other hand, the densities of the charge carriers caused by the initial breakdown current are still negligibly low compared to the ionized impurity concentrations. So as verified by the device simulation results, the above-mentioned full depletion condition is always satisfied for the device under investigation in this work.

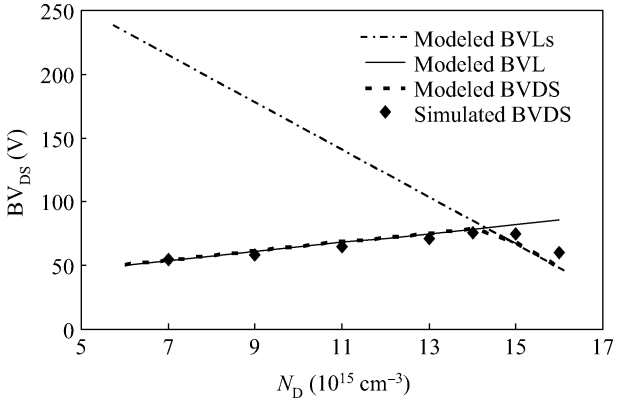

Fig. 3. Dependence of breakdown voltage on N_D. $N_A = 1 \times 10^{15}$ cm^{-3}, $L = 5$ μm, $L_S = 1$ μm, $t_f = 0.08$ μm, $t_1 = 0.6$ μm, $t_2 = 4.2$ μm.

3. Results and discussions

The proposed model is validated by numerical device simulation performed with the Sentaurus TCAD simulator. The electrostatic potential and charge carrier density are computed by solving both the Poisson equation and the two carrier continuity equation during simulation.

Figures 2(a) and 2(b) compare modeled and simulated surface potential and surface field along the drift region at the onset of breakdown with $V_{GS} = V_S = 0$ V and $V_{DS} = 65$ V. The analytical and simulation results are obtained with $N_D = 1 \times 10^{16}$ cm^{-3}, $N_A = 1 \times 10^{15}$ cm^{-3}, $L = 4.5$ μm, $L_S = 1$ μm, $t_f = 0.08$ μm, $t_1 = 0.6$ μm, $t_2 = 4.2$ μm. From Fig. 2(a) one can see that the analytically modeled potential curve is in very good accordance with the Sentaurus simulation results. In addition, as demonstrated by the simulation, the maximum electric field along the drift region surface is either located at the drain end ($x = L$) or at the Faraday edge ($x = L_S$). The simulated surface field distribution is reproduced on the whole by the model in Fig. 2(b).

As in the practical design of an LDMOS transistor, it is a fundamental requirement to minimize the on-resistance while still maintaining a high breakdown voltage. The on-resistance is closely related to the drift region doping concentration. The charge of the n-layer will determine the sheet resistance of that layer and it is the most critical parameter for the high voltage device. So first we consider the effect of N_D on the breakdown voltage. Figure 3 shows the modeled and simulated effect of drift region doping concentration on breakdown voltage. It can be seen that the modeled BVL curve increases while BVL_S curve decreases with N_D and the two curves intersect at a certain point. As the smaller one of BVL and BVL_S, the modeled BV_{DS} experiences an initial rise followed by a subsequent fall with a peak occurring at the intersection point. When N_D is lower than the critical concentration corresponding to the peak BV_{DS}, breakdown occurs at the drain end, i.e. $BV_{DS} = BVL$. When N_D gets larger than the critical value, breakdown occurs at the shield end, i.e. $BV_{DS} = BVL_S$. As shown in Fig. 3, the simulated BV_{DS} also initially increases and then decreases with N_D. The modeled BV_{DS} are found to agree quite well with the simulated BV_{DS} over the range of low N_D, but begin to deviate from the simulation data with increasing N_D approaching

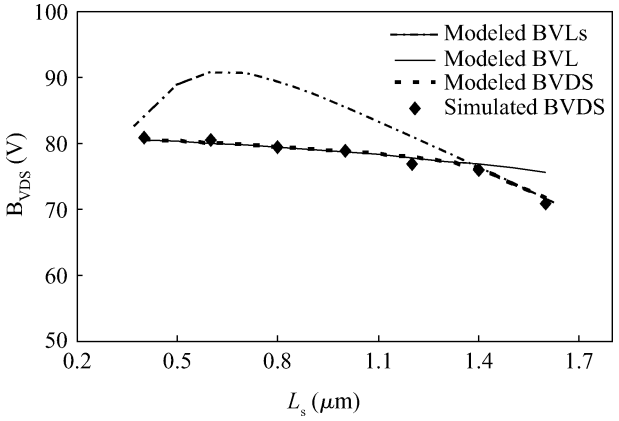

Fig. 4. Dependence of breakdown voltage on Faraday shield length. $N_D = 1.4 \times 10^{16}$ cm^{-3}, $N_A = 1 \times 10^{15}$ cm^{-3}, $L = 5$ μm, $t_f = 0.08$ μm, $t_1 = 0.6$ μm, $t_2 = 4.2$ μm.

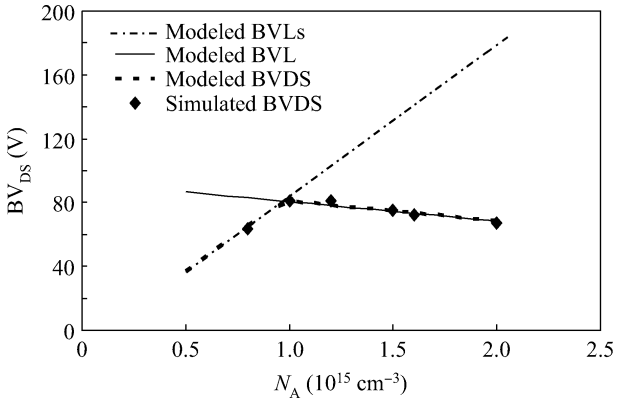

Fig. 5. Dependence of breakdown voltage on epitaxial layer doping concentration. $N_D = 1.4 \times 10^{16}$ cm^{-3}, $L = 5$ μm, $L_S = 0.4$ μm, $t_f = 0.08$ μm, $t_1 = 0.6$ μm, $t_2 = 4.2$ μm.

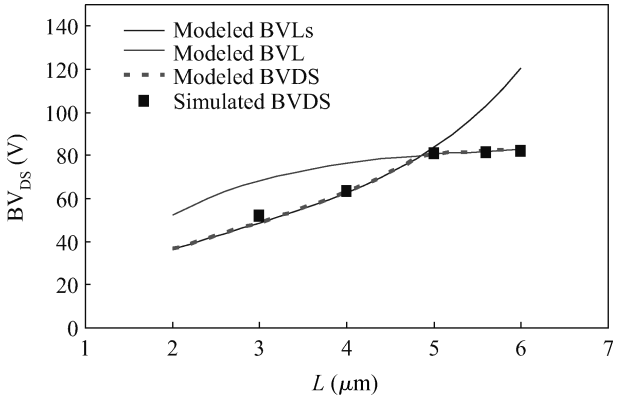

Fig. 6. Breakdown voltage versus drift region length. $N_D = 1.4 \times 10^{16}$ cm^{-3}, $N_A = 1 \times 10^{15}$ cm^{-3}, $L_S = 0.4$ μm, $t_f = 0.08$ μm, $t_1 = 0.6$ μm, $t_2 = 4.2$ μm.

the critical concentration. Physically, the drift region cannot be fully depleted any more as N_D increases above a certain value, then Poisson Eq. (1) is not valid for the whole drift region. This may be the reason for the discrepancies between the modeled and simulated BV_{DS} when N_D is very high. So the model is valid for devices whose N_D is smaller than the critical value to fully deplete the drift region. In practice, the critical value of N_D would help mark a local optimum concentration in device and process design for the RF LDMOS power transistors in terms of the trade-off between breakdown voltage and on-resistance.

Figure 4 shows the modeled and simulated effect of Faraday shield length on breakdown voltage. It can be seen that, on the whole, the breakdown voltage decreases with increasing L_S. A closer look at the figure indicates that the modeled BV_{DS} curve as a function of L_S is divided into two segments by the intersection point of the modeled curves of BVL_S and BVL. To the left of the point, BV_{DS} decreases gradually with increasing L_S, tracing BVL versus L_S, while to the right of the point, BV_{DS} drops sharply down the BVL_S locus with respect to L_S. As also shown in Fig. 4, the modeled BV_{DS} results are found to be in good agreement with the corresponding simulation data, justifying the two-segment L_S dependence of BV_{DS}. As reported by Ref. [13], longer L_S can result in lower feedback capacitance C_{GD}, which may help improve the linearity of the RF LDMOS power transistor. In this sense, at least in the operation region of interest in this work, prolonging L_S for the purpose of reducing feedback capacitance may incur a breakdown penalty. So in practical design such a trade-off may need to be considered, for example, the L_S at the intersection point in Fig. 4 might be a fairly good choice to ensure greatly reduced feedback capacitance at the modest cost of breakdown voltage loss.

The breakdown voltage dependence on the epitaxial layer doping concentration N_A shown in Fig. 5 is similar to N_D dependence shown in Fig. 3. When N_A is very low, the electrical field peak is located at the shield edge, and breakdown occurs when the peak field reaches E_c. So BV_{DS} is equal to BVL_S, which is determined by Eq. (21) and increases with N_A as shown in Fig. 5. Electrical field peak moves to the drain end when N_A is very high and breakdown occurs at the drain end. Now, BV_{DS} becomes BVL, which is determined by Eq. (22) and decreases with N_A. So there exits an optimal doping concentration, where the electrical field at the shield edge is equal to that at the drain edge, and breakdown voltage reaches the largest value. As can be seen also in Fig. 5, the modeled N_A dependence of BV_{DS} is verified by the simulation data which coincide well with the calculation curve. This demonstrates that the doping concentration in the p-epitaxial layer can indeed affect the source–drain breakdown voltage by modulating the surface potential and field in the n^- drift region. As a result, the N_A influence cannot be ignored, as in Refs. [9, 10], in order to accurately model the breakdown voltage.

Figure 6 shows the dependence of the breakdown voltage on drift region length L. Again, good agreement is obtained between modeling curve and simulation data points. On the contrary to L_S in Fig. 4, the breakdown voltage increases as L. Obviously longer drift region can reduce the lateral electrical field under a given drain bias voltage, thus increasing BV_{DS}. A more careful investigation shows that the modeled curves of BVL_S and BVL go up with increasing L at an accelerating and decelerating rate, respectively, intersecting at a critical L whose value is about 5 μm for the device under study in Fig. 6. When $L < 5$ μm, electrical field peak is located at the shield edge, and breakdown occurs in this region, $BVL_S = \min(BVL_S, BVL)$ as shown in the figure, BV_{DS} is determined by Eq. (21) increas-

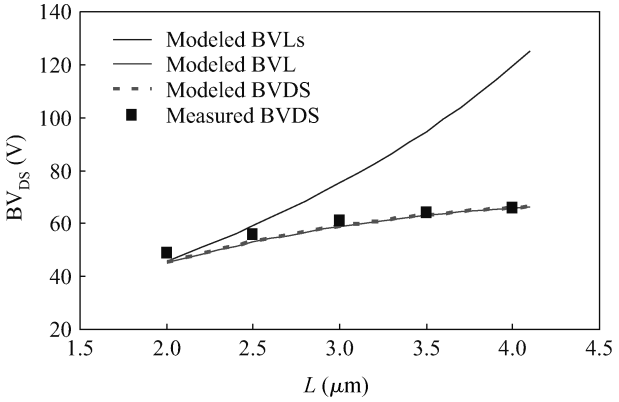

Fig. 7. Breakdown voltage versus drift length. $N_D = 1 \times 10^{16}$ cm^{-3}, $N_A = 1 \times 10^{15}$ cm^{-3}, $L_S = 0.75$ μm, $t_f = 0.32$ μm, $t_1 = 0.6$ μm, $t_2 = 5$ μm.

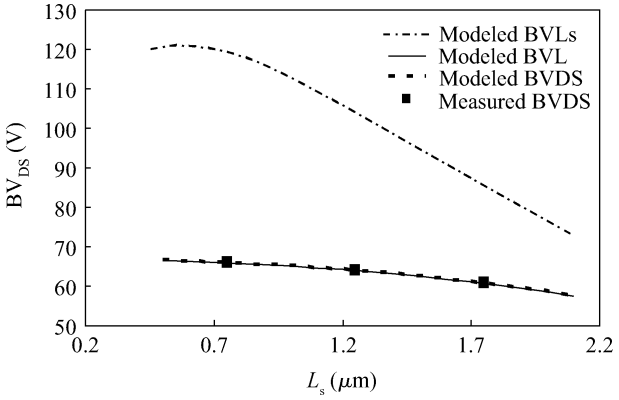

Fig. 8. Breakdown voltage versus Faraday shield length. $N_D = 1 \times 10^{16}$ cm^{-3}, $N_A = 1 \times 10^{15}$ cm^{-3}, $L = 4$ μm, $t_f = 0.32$ μm, $t_1 = 0.6$ μm, $t_2 = 5$ μm.

ing rapidly with L. When $L \geqslant 5$ μm, the electrical field peak moves to the drain edge, BVL $=$ min (BVL$_S$, BVL) as shown in the figure, and BV_{DS} is determined by Eq. (22) going on increasing but rather slowly with L. Finally BV_{DS} saturates with L. In practical design, the above-mentioned critical L may be taken as a limit for drift region length since a further increase in L will lead to a little BV_{DS} benefit but a considerable on-resistance penalty.

The proposed LDMOS model is also validated on the measured breakdown characteristics of LDMOS transistors in different configurations. Figures 7 and 8 show the measured and modeled dependence of breakdown voltage on the drift region length and Faraday shield length, respectively. The device parameters necessary for the modeling calculation are listed under the figures. The values for these parameters are determined in the following way. Firstly, L, L_S, N_A and t_f are known directly from the device layout and fabrication process information. Secondly, t_1, t_2 and N_D are estimated with the help of the Sentaurus process simulation.

As a consequence, fairly good agreements between modeling calculation results and the corresponding measurement data shown in the two figures further confirm the validity of the proposed model.

4. Conclusion

In this paper, an analytical model of the drain–source breakdown voltage of an RF LDMOS power transistor with a Faraday shield is presented on the basis of an approximate solution to the 2D Poisson equation in the p-epitaxial layer as well as the n$^-$ drift region. The modeling calculation results show a good agreement with the corresponding device simulation and measurement data over a wide range of device parameters. With the help of analysis by using the proposed model, the dependence of BV_{DS} on different device parameters is revealed to be closely associated with the transition of breakdown position along the drift region surface. The device parameters corresponding to these modeled transition points may be chosen in practical RF LDMOS device design for optimizing trade-offs between the breakdown voltage and other characteristic parameters such as on-resistance and feedback capacitance.

Acknowledgements

The authors would like to thank Shanghai Beiling Corp., Ltd for manufacturing the RF LDMOS power transistors, from which the experimental results used in this work are measured.

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