Low power fast settling multi-standard current reusing CMOS fractional-*N* frequency synthesizer*

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Abstract: A low power fast settling multi-standard CMOS fractional-*N* frequency synthesizer is proposed. The current reusing and frequency presetting techniques are adopted to realize the low power fast settling multi-standard fractional-*N* frequency synthesizer. An auxiliary non-volatile memory (NVM) is embedded to avoid the repetitive calibration process and to save power in practical application. This PLL is implemented in a 0.18 μm technology. The frequency range is 0.3 to 2.54 GHz and the settling time is less than 5 μs over the entire frequency range. The LC-VCO with the stacked divide-by-2 has a good figure of merit of –193.5 dBc/Hz. The measured phase noise of frequency synthesizer is about –115 dBc/Hz at 1 MHz offset when the carrier frequency is 2.4 GHz and the reference spurs are less than –52 dBc. The whole frequency synthesizer consumes only 4.35 mA @ 1.8 V.

Key words: phase-locked loop; current reusing; forward-body bias; divide-by-2; multi-standard; fast settling

DOI: 10.1088/1674-4926/33/4/045004 **EEACC:** 1205; 1230

1. Introduction

With the development of communication，more and more communication standards have emerged in recent years. Wireless local area networks, wireless body area networks, wireless personal area networks and cell phones are widespread. It is highly desirable that one hardware system can serve a wide variety of communication standards in real time. This suggests that we need to design a reconfigurable single chip which is software configurable across many channels in the wide frequency bands and is compatible with more communication services. Recently there has been a significant progress in wireless communications in terms of the multi-standard single RF transceiver chip[1]. However, one of challenges in such an RF transceiver is to design a low power fast settling multi-standard frequency synthesizer. It should enable proper interoperability and seamless connectivity among the various communication standards. Thus a low power and fast settling design is necessary in order to prolong the life of a battery and to switch the communication channels rapidly. A SiGe BiCMOS frequency synthesizer that is fully compliant with the multi-standard was presented[2]. It used two VCOs so that the whole system consumed large current. Another BiCMOS multimode frequency synthesizer was developed[3]. It used two PLL loops to generate the LO signals. Power consumption and die area were also the main drawbacks in that design. There has not been an intensive innovation effort about fast settling speed.

This paper proposes a low power fast settling multi-standard fractional-*N* frequency synthesizer for multi-standard applications. The synthesizer uses one LC-VCO with current reusing and a frequency presetting function. The current reusing technique reduces the synthesizer power obviously. The frequency presetting technique shortens the settling time, which can satisfy the different settling time requirements. Then a forward-body bias (FBB) technique is employed in the LC-VCO circuits to reduce the threshold voltage (V_{TH}) of the transistors and to improve the phase noise performance. A standard CMOS non-volatile memory (NVM) is embedded to store the configuration and calibration parameters so that the PLL frequency synthesizer can avoid the repetitive calibration process. A novel low power divide-by-32/33 dual mode prescaler (DMP) is developed, which adopts a low power optimization technique. The rest of the paper is organized in four parts. Firstly we will introduce the frequency synthesizer architecture. Then the detailed circuit design of the frequency synthesizer will be presented. Furthermore, we show the experimental results of this synthesizer. Finally we give the conclusions.

2. Frequency synthesizer architecture

It is often difficult to generate the multi-standard carrier using one integer-*N* frequency synthesizer whose step size is limited by reference frequency. So the fractional-*N* synthesizer is the more preferable option. The fractional-*N* frequency synthesizer has the following advantages: (1) realizing high frequency resolution; (2) higher reference frequency is used to avoid higher division ratios; and (3) bandwidth of the loop is not limited by the channel spacing. However, the fractional spur is the major issue in the fractional-*N* frequency synthesizer. Figure 1 shows the architecture of the proposed frequency synthesizer. It is the typical fractional-*N* architecture that consists of a phase frequency detector (PFD), a charge pump (CP), an LC-VCO with stack divide-by-2, a divide-by-3, a dual mode prescaler (DMP), a 3rd loop filter (LPF), a presetting module, a digital processor, an auxiliary non-volatile memory (NVM), a multiplexer and an output buffer.

* Project supported by the National Natural Science Foundation of China (No. 60976023) and the National Science and Technology Major Project of China (Nos. 2009ZX03007-001, 2012ZX03004007-002).

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Received 31 August 2011, revised manuscript received 15 October 2011

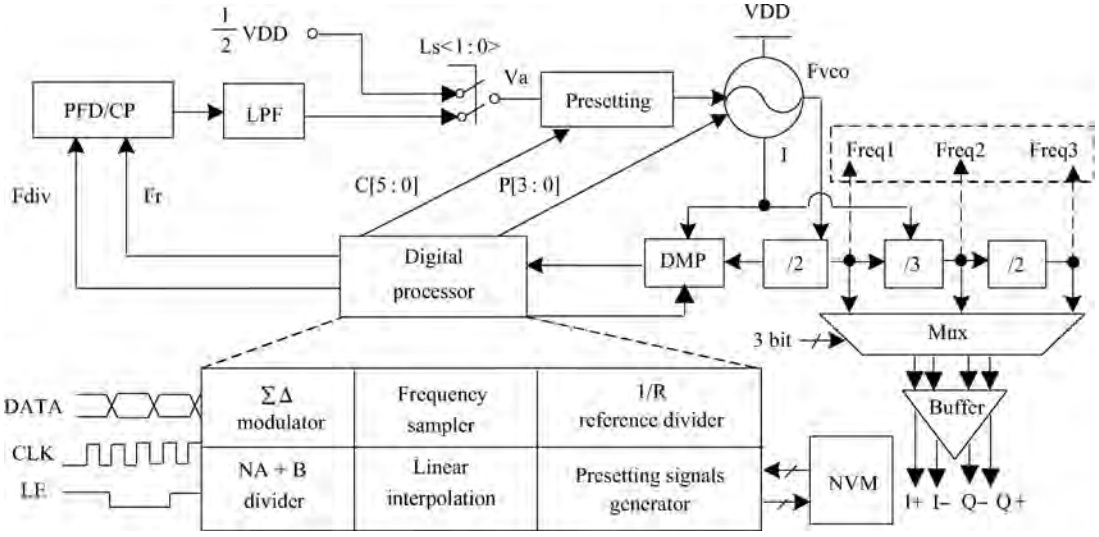

Fig. 1. Architecture of the proposed frequency synthesizer.

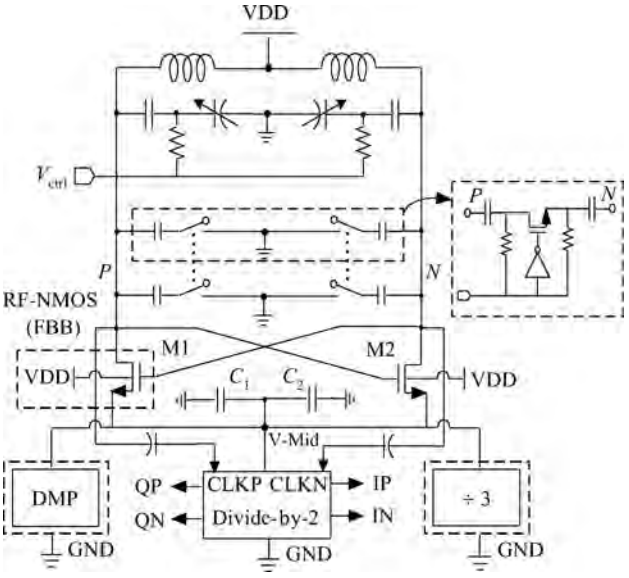

Fig. 2. Current reusing LC-VCO and stacked modules.

This frequency synthesizer generates three frequency bands: Freq1, Freq2 and Freq3. The LC-VCO is the most power hungry block in the frequency synthesizer. The current through the LC-VCO is shared with the stack divide-by-2, divide-by-3 and DMP modules. It makes the $I_{\text{LC-VCO}}$ equal to $I_{/2} + I_{/3} + I_{\text{DMP}}$. The technique can reduce the power consumption of the synthesizer effectively. The presetting module is used to shorten the settling time. The technique accurately presets the frequency of the VCO with little initial frequency error and greatly reduces the settling time. The details of current reusing and frequency presetting techniques will be discussed in the following section. Most transceivers with a quadrature modulation scheme require I/Q LO signals. An efficient method for I/Q generation is that a two-times higher frequency of the LC-VCO is divided by a divide-by-2 module. It can provide accurate I/Q signals with minimal mismatch. Although it costs higher power consumption than the passive I/Q generation techniques because there is an additional high frequency divide-by-2 circuit, it avoids the problem in our design that the current of LC-VCO is reused by the divide-by-2. In this design the LC-VCO oscillates at a two-times higher frequency than the required frequency. It will overcome the problems of the injection pulling and PA pulling in the transceiver environment[4].

3. The detail circuit design

3.1. LC-VCO and stack modules

Figure 2 shows the current reusing LC-VCO with stacked modules. Three modules including divide-by-2, divide-by-3 and DMP are stacked under LC-VCO. These three modules share the current through the LC-VCO module. The current reusing reduces the power consumption effectively. The LC-VCO only uses one pair cross-coupled NMOS transistors M1 and M2 to minimize the number of stacked transistors between the two supply rails. It can provide enough voltage headroom for the under stack circuit. In order to realize a wide tuning range and a small VCO gain (K_v), a 4-bit binary switchable capacitors array (SCA) is connected to the LC tank for coarse frequency tuning and is controlled by a presetting signal P[3:0]. The divide-by-2, divide-by-3 and DMP are stacked under the LC-VCO through the node V-Mid. To avoid the variation of the V-Mid, a self-biasing scheme is used in the circuit[5]. Furthermore, there is enough design margin for the stacked modules. From the post simulation, V-Mid is approximate 1.2 V ($V_{\text{DD}} =$ 1.8 V), which makes the up/bottom modules operate well. The design margin makes sure that the design operates well over the whole frequency band when V-Mid is with +/–15% variation (V-Mid = 1.0–1.4 V). So, all these techniques above are employed to improve its robust operation. Two capacitors C_1 and C_2 are connected to node V-Mid. The capacitors can optimize the phase noise by filtering the second harmonic frequency of the LC-VCO and make node V-Mid more stable. The threshold voltage of the transistors M1 and M2 are the fundamental limitation to the oscillation amplitude. To increase the oscillation amplitude, the forward-body bias (FBB) technique is adopted as shown in Fig. 2. The transistors M1 and M2 are the RFMOS

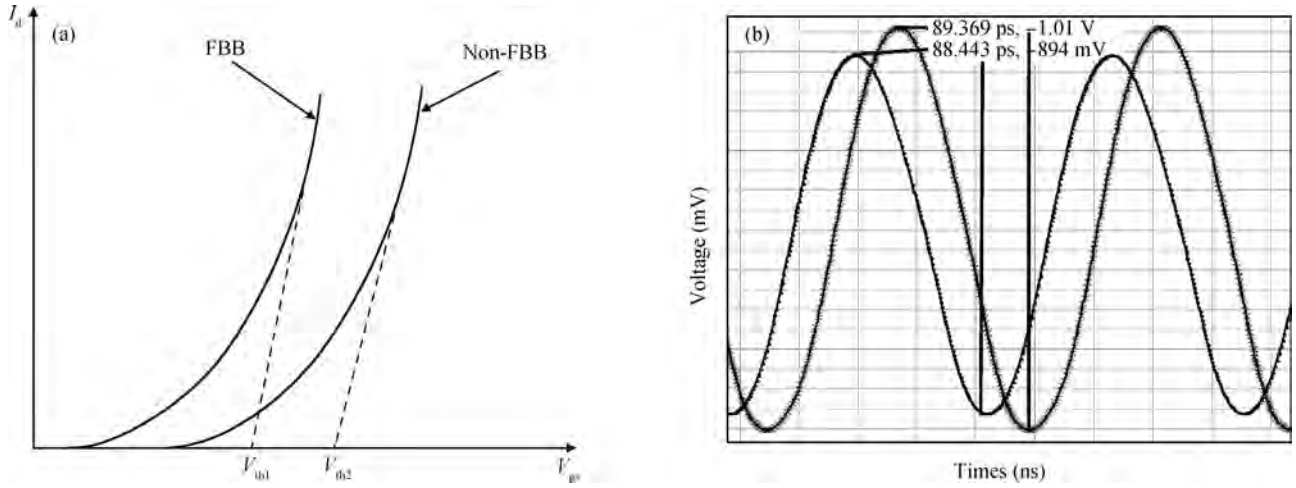

Fig. 3. Effect of FBB technique. (a) RFMOS I–V curve. (b) LC-VCO oscillation amplitude.

transistors, which have a deep N-well to form the separate substrate and prevent the noise interference from ground and supply. For the MOSFET device, the threshold voltage is governed by the body effect as

$$V_{\mathrm{Th}} = V_{\mathrm{Th0}} + \gamma(\sqrt{|2\Phi_{\mathrm{F}} + V_{\mathrm{SB}}|} - \sqrt{|2\Phi_{\mathrm{F}}|}), \qquad (1)$$

where V_{Th0} is the threshold voltage for $V_{\mathrm{SB}} = 0$ V, Φ_{F} is a physical parameter, and γ is body effect coefficient. The forward bias voltage on the deep N-well reduces the threshold voltage while maintaining V_{SB} less than zero. The bulk node of the transistors M1 and M2 is connected to the VCO's supply. The effective threshold voltage is shown in Fig. 3(a). V_{Th} decreases by about 100 mV. LC-VCO oscillation amplitude increases by over 100 mV more than that of without FBB technique in Fig. 3(b). This can improve the phase noise of the LC-VCO.

The divide-by-2 is the current-mode logic (CML) static frequency divider. In order to minimize the number of the stacked transistors between two supply rails, it is built without current source. The quadrature signals generated by the divide-by-2 module have the better phase and amplitude match. The divide-by-3 generates the 50% duty cycle signals, which is suitable for the I/Q signal generation. However, the conventional divide-by-3 circuits cannot generate the I/Q signals. The low power DMP is 32/33 divider that consists of a cascade of four divide-by-2 circuits followed by a divide-by-2/3. The optimized design can make the DMP operate at low voltage and realize the low power consumption. Divide-by-3 and DMP schemes will be discussed in the next part.

3.2. Frequency presetting method and process

Figure 4 shows the presetting module and the LC-VCO circuit. The presetting module is a mixed-signal circuit that consists of six parallel current sources[6]. A 6-bit digital presetting signal C[5 : 0] controls on and off of the current sources. MP3, MP5, …, MP11 and MP13 transistors constitute a series of current sources with different ratios of the currents: 2^n ($n = 0$, 1, 2, 3, 4, 5), respectively. When P[3 : 0] and C[5 : 0] are set to LC-VCO and the frequency presetting module, respectively, LC-VCO will oscillate at a presetting frequency that is very close to the target frequency. Thus the frequency of VCO is accurately preset with small initial frequency error. Then the output voltage V_{a} of the LPF accurately tunes the frequency of LC-VCO by adjusting the current through MP15 transistor. Finally the loop will adjust the voltage of V_{a} to lock the target frequency quickly. This frequency synthesizer can operate in two modes: calibration mode and operation mode, as shown in Fig. 1. In calibration mode, the phase lock loop is opened by switch LS<1 : 0> = 2′b10, and the voltage of V_{a} in the presetting module is biased at 1/2 V_{DD}. Then the digital processor can automatically sample the VCO's frequency and calculate the presetting signals P[3 : 0] and C[5 : 0] by the frequency sampler, linear interpolation and presetting signal generator module, respectively. The presetting signals P and C are stored in NVM memory. In most situations, we need to store several different presetting signals P and C in the NVM, which are related to several different frequencies, so the process described above may be carried out several times. After the several groups of presetting signals P and C are stored in NVM, the calibration mode is finished.

In operation mode, the switch LS<1 : 0> is set 2′b01, and the loop is closed. The digital processor reads out the signals P and C from NVM according to the divide ratio information. Then the presetting signals P and C control the presetting module and the 4-bit SCA in LC-VCO, respectively, and preset the target frequency of LC-VCO. After the presetting operation, the LC-VCO will oscillate at a presetting frequency that is very close to the target frequency. Then the output voltage V_{a} of the LPF precisely tunes the frequency of the LC-VCO by adjusting the current through the MP15 transistor. Therefore the synthesizer can be locked in a very short time. Its settling time almost does not depend on frequency step, process variation, device parasitic effect and chip temperature.

3.3. Auxiliary non-volatile memory

The low power NVM is based on the FN tunneling phenomenon with extremely small current density[7]. It is compatible with the standard CMOS process. It stores the control signals and calibration parameters obtained in calibration mode. This avoids the repetitive calibration process and saves power

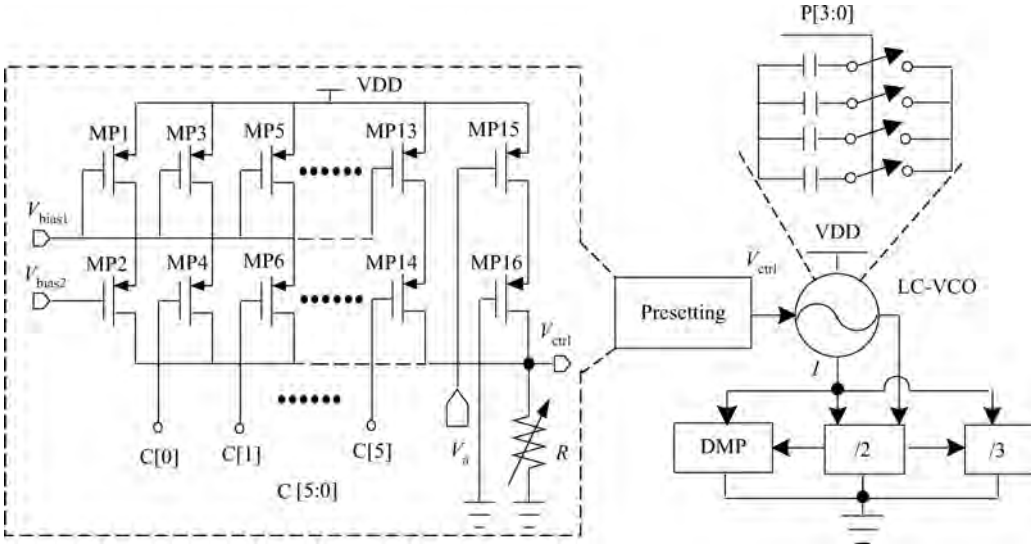

Fig. 4. LC-VCO with presetting module.

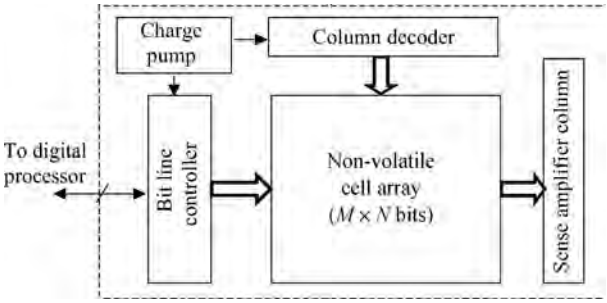

Fig. 5. Architecture of the NVM.

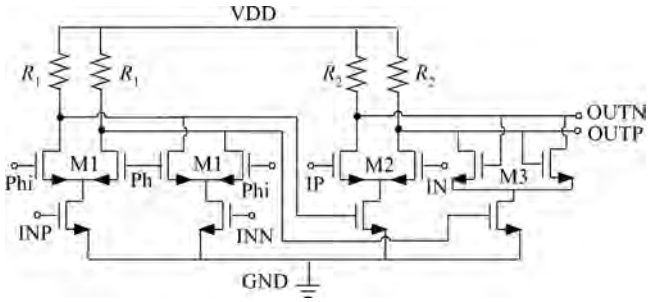

Fig. 7. Phase-switchable level-sensitive (PSLS) latches.

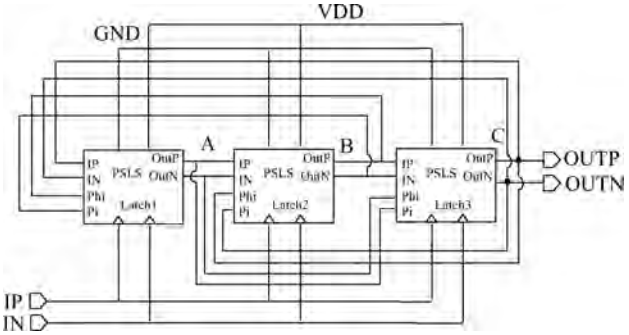

Fig. 6. Topology of the divide-by-3.

consumption in practical applications. The architecture of the NVM is shown in Fig. 5. It consists of a NV cell array, a bit line controller, a column decoder, a sense amplifier column and a charge pump. The controller controls the write/read operation of the NV memory. The column decoder selects the active column. The sense amplifiers detect the outputs of the active-column cells in reading operation. The charge pump generates a high voltage and a medium voltage in writing operation. The implementation method of the circuits is discussed in Ref. [7].

3.4. Divide-by-3 with 50% output duty cycle

To obtain the multi-standard carriers, a divide-by-3 is designed to follow the divide-by-2. However, the primary obstacle with the divide-by-3 is the generation of I/Q signals. The signals at the output of the divide-by-3 should be 50% duty cycle. But it is difficult to realize 50% duty cycle by conventional divide-by-3 circuits[8]. In this section, a divide-by-3 with 50% output duty cycle[9] is addressed. Figure 6 shows the topology of the divider. It consists of three phase-switchable level-sensitive (PSLS) latches. The PSLS latch is shown in Fig. 7. It consists of one standard SCL latch and one double-edge-triggered latch (both positive and negative edge-triggered). The standard latch is driven by the double-edge-triggered latch. If the latch is transparent during either the high or the low level of the clock, the instantaneous value of the phi is transmitted to the standard SCL latch. Figure 8 shows conceptually the timing diagram of the divide-by-3 (signals at nodes A, B and C in Fig. 6.) It has a 50% duty cycle. They are suitable to connect poly-phase filter or divide-by-2 circuit for I/Q quadrature signals generation. The divide-by-3 circuit can also be viewed as a three-stage ring oscillator when the amplitude of the input clock signal is set to zero. We use the small signal analysis method to analyze the operation. The oscillation condition of the circuit is derived as follows, which is the Barkausen criteria for ring oscillation.

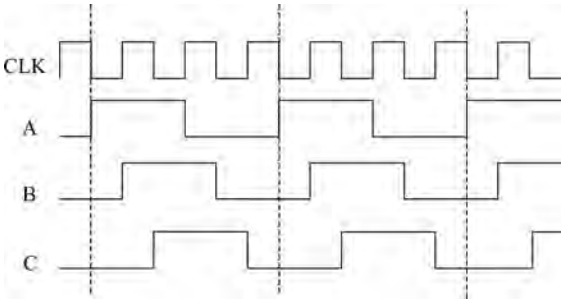

Fig. 8. Divide-by-3 timing diagram.

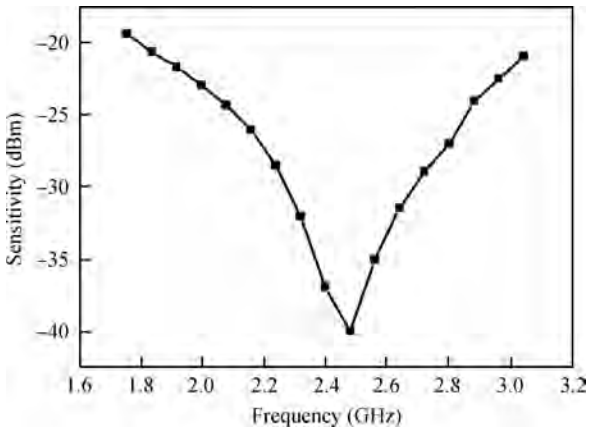

Fig. 9. Sensitivity of the divide-by-3.

$$\angle G^3(\mathrm{j}\varpi_{\mathrm{OSC}}) = n\pi, \quad n = \text{odd}; \quad \left|G^3(\mathrm{j}\varpi_{\mathrm{OSC}})\right| \geqslant 1, \quad (2)$$

where G is the transfer function of each stage of the oscillator, and ϖ_{OSC} is the self-oscillation frequency. The transfer function G can be written as

$$G = \frac{g_{\mathrm{m2}}}{Y_{\mathrm{L2}} - g_{\mathrm{m3}}} \frac{g_{\mathrm{m1}}}{Y_{\mathrm{L1}}}, \quad (3)$$

where $Y_{\mathrm{L1}} = g_1 + SC_1, Y_{\mathrm{L2}} = g_2 + SC_2, C_1$ and C_2 are the load capacitors of the double-edge-triggered latch and standard SCL latch respectively, g_1 and g_2 are the transconductances of the load resistors in the standard and double-edge-triggered latch. g_{m1}, g_{m2}, g_{m3} are the transconductances of the M1, M2, M3 respectively.

From the Barkausen oscillation criteria, we can obtain the relationship between self-oscillation ϖ_{OSC} and the circuit parameters as follows:

$$\varpi_{\mathrm{OSC}} \leqslant \frac{\sqrt{g_{\mathrm{m}}^2 - g_1^2}}{C_1}, \quad (4)$$

where g_{m} is the assumption $g_{\mathrm{m1}} = g_{\mathrm{m2}} = g_{\mathrm{m3}} = g_{\mathrm{m}}$. So Eq. (4) imposes a limiting constraint on the self-oscillation frequency. In fact, the input signal with the frequency $3\varpi_{\mathrm{OSC}}$ has very high input sensitivity for the divide-by-3. Figure 9 shows the input sensitivity of the divide-by-3 at a 1.2 V voltage. Based on Eq. (4), there exists a trade-off among power consumption, operation frequency and load capacitor. So we optimized the power consumption of the circuit to obtain the low power.

3.5. Low power divide-by-32/33 dual mode prescaler (DMP)

In order to reduce the total power of the frequency synthesizer, a low voltage low power divide-by-32/33 DMP is developed. Figure 10 shows the proposed low power DMP scheme, which consists of one divide-by-2/3 circuits and four divide-by-2 stages. Only two flip-flops with NOR gates operate at the highest frequency, which is different from the conventional DMP with three D flip-flops working at highest frequency[10]. Another type of low power DMP is phase switching prescaler[11] which only has one D flip-flop operating at highest frequency. But it may suffer from the switch glitch. Although various significant efforts have been made to remove the glitches[12], it increases the complication and power in circuit design. In our design, in order to further optimize the power consumption of the DMP, different divide-by-2 and NAND gates circuits are adopted according to the different operation frequency. High frequency operation modules Div2(A) and Nand(A) adopt resistance load SCL circuits. They are shown in Figs. 11 (a) and 11(b). Low frequency operation modules Div2(B) and Nand(B) adopt PMOS load SCL circuits. They are shown in Figs. 11(c) and 11(d). These dividers and NAND gates with PMOS load instead of the resistance can reduce the static power consumption. All these modules are implemented in differential circuit topologies that make sure the DMP operate at a low supply voltage. The divide-by-2/3 circuit is composed of a high speed D flip-flop with the function of NOR logic. The divider and NAND gates do not include current source so that it has the merits of high frequency operation, low power consumption and large voltage headroom[13]. The sizes of the transistors in dividers and NAND gates can be properly scaled to achieve high speed and low power consumption. Figure 12 shows the post simulation of DMP module when the input frequency is 2.4 GHz. It indicates that this DMP can work well under the low voltage supply (1.2 V).

3.6. PFD/CP/LPF

Figure 13 shows the schematic of the dead-zone-zero PFD. It utilizes two flip-flops to produce three states (pull-up, pull down and high-impendence)[14]. Four inverters are inserted in the reset path as the delay cell to avoid the dead-zone problem. In order to reduce the skew between the complementary output signals UP and DN, two cross inverters are inserted in the output path. This technique can effectively accelerate the rise and fall speed of the pulse. This is favorable to reduce the mismatch between the up and down current source in charge pump.

Figure 14 shows the schematic of the charge pump (CP) and the 3rd loop filter (LPF). The switches MN1, MN2, MP1and MP2 are put at the sources of the current mirrors to improve the switching speed and avoiding high current spikes at the output[15]. Current reference is formed by MP6, MN6, MN7 and current mirrors MP3, MP4, MN3, MN4. In order to match the current more precisely, three methods are adopted. First, compensation of the low output impedance of source and sink currents is done to make the current variation less sensitive to the output voltage V_{c}. The sink and source currents are mon-

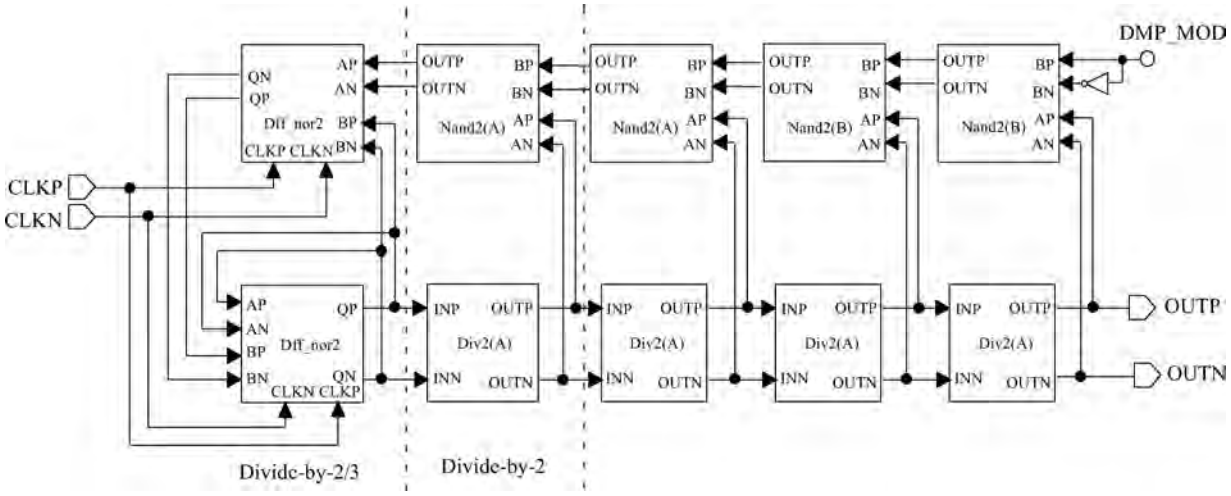

Fig. 10. Low power divide-by-32/33 DMP.

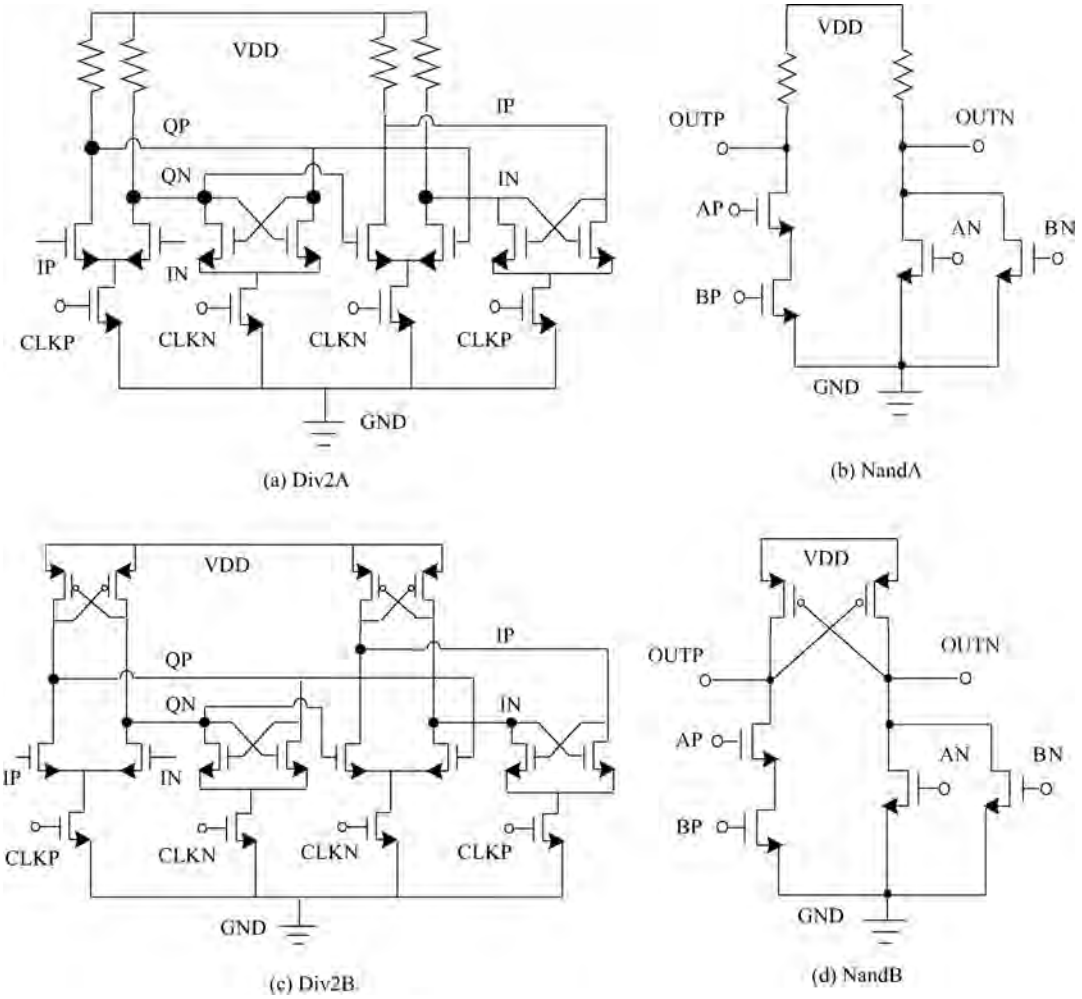

Fig. 11. Different dividers and NAND gates in DMP.

itored in the replica circuit. A negative feedback circuit (made by an OPA) compares the output voltage V_c with the replica circuit voltage V_{rep} to make V_{rep} follow V_c. Second, in order to eliminate the effect of the charge sharing and the current glitch, two switches MN5 and MP5 are used to provide low-impedance discharging paths for removing the charge from nodes A and B when the switches are turned off. Finally, large size transistors for current mirrors are used for better matching in layout design. Two 10-pF bypass capacitors C_{up} and C_{dn} are connected to the gates of MP3 and MN3 to further attenuate the current glitches.

A 3rd on-chip passive loop filter is used as shown in

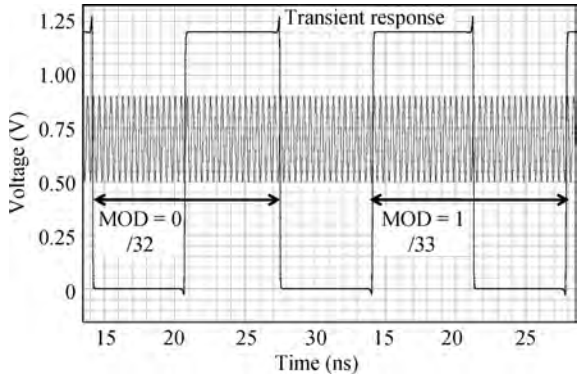

Fig. 12. Transient simulation of the DMP @ 2.4 GHz.

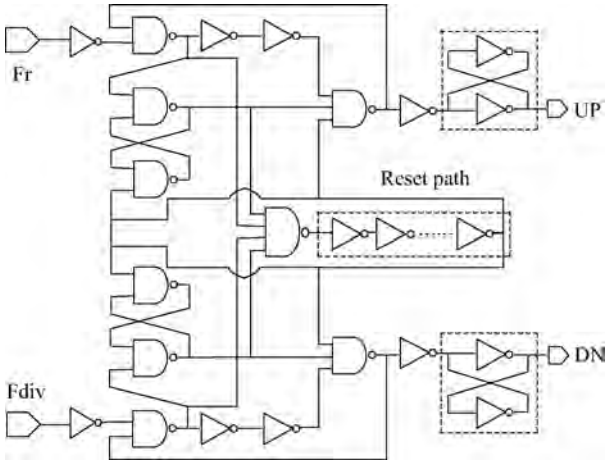

Fig. 13. Schematic of the dead-zone-free PFD.

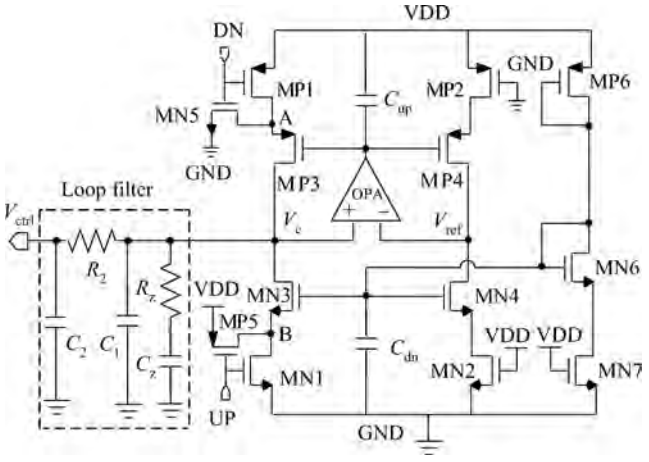

Fig. 14. Schematic of charge pump and LPF.

Fig. 14. The design parameters are optimized by the system level performance specifications such as settling time, phase noise and spur suppression. The parameters are as follows: $C_1 = 26$ pF, $C_2 = 5$ pF, $C_z = 152$ pF, $R_z = 30$ kΩ, $R_2 = 20$ kΩ.

4. Experimental results

The proposed fractional-N frequency synthesizer was implemented in 0.18 μm CMOS process. Figure 15 shows the

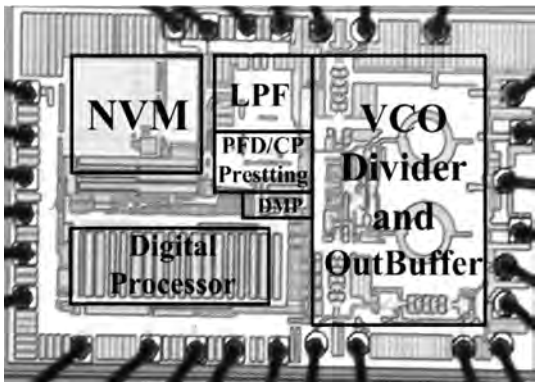

Fig. 15. Microphotograph of the chip.

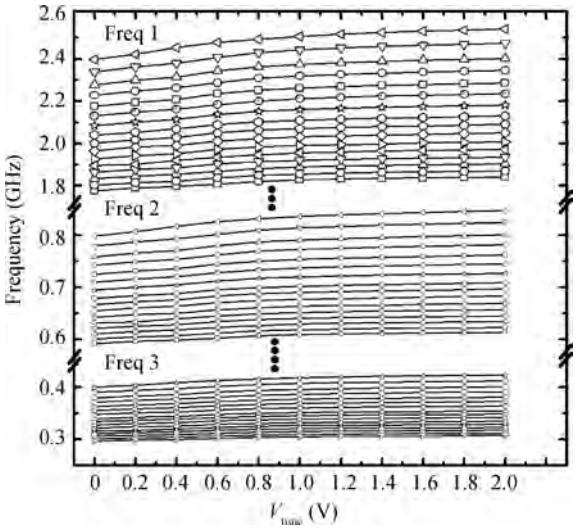

Fig. 16. The measured three frequency bands of the synthesizer.

microphotograph of the chip. The die area is 1×1.6 mm^2 that includes the pads. The whole frequency synthesizer only draws 4.35 mA from a 1.8 V voltage supply. All control signals are supplied through the digital processor, and the reference frequency is 2 MHz (external crystal is 50 MHz).

The LC-VCO oscillated at the double frequency (3.5–5.08 GHz) of the needed frequency. Figure 16 shows the measured three frequency bands of the synthesizer: Freq1, Freq2 and Freq3. Freq1 is the output frequency of the LC-VCO with stacked divide-by-2 and covers a frequency range from 1.75 to 2.54 GHz. The frequency tuning curves are switched by digital word P[3 : 0]. Freq2 (0.58–0.85 GHz) is the output frequency of the divide-by-3, and Freq3 (0.29–0.425 GHz) is obtained from Freq2 by divide-by-2. In addition, Freq1 also can be divided by two with external divider to get the frequency band from 0.875 to 1.27 GHz.

Figure 17 shows the dependence of the LC-VCO presetting frequency on the signals P[3 : 0] and C[5 : 0] when V_a is 0.9 V. The measured result shows a good linear relation between the presetting frequency and the control signal P/C. The better linear relationship between presetting frequency and the signal C, the smaller initial frequency error will be got, which will shorten the settling time. Figure 18 shows the typical frequency hopping characteristic of the frequency synthesizer. The de-

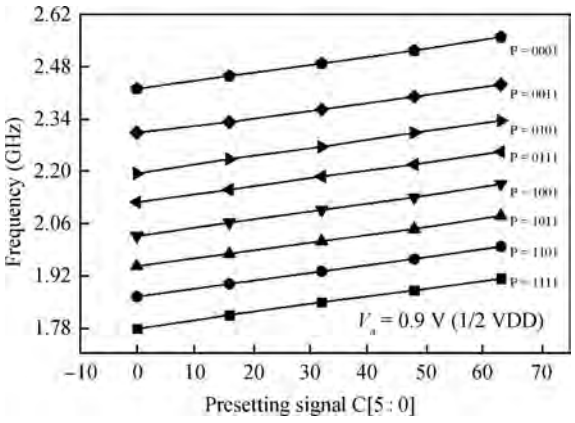

Fig. 17. Frequency versus presetting signal C[5 : 0] with different values P[3 : 0].

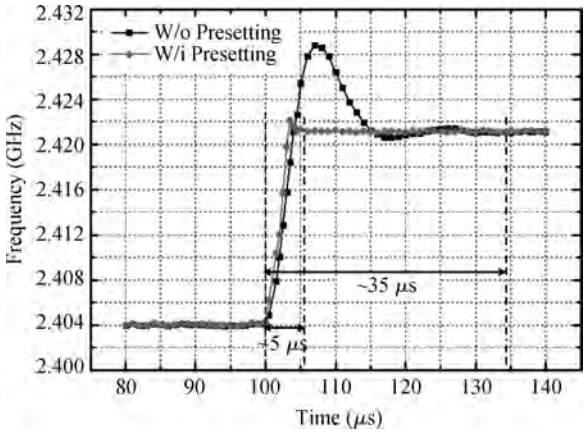

Fig. 18. Typical settling time of the synthesizer.

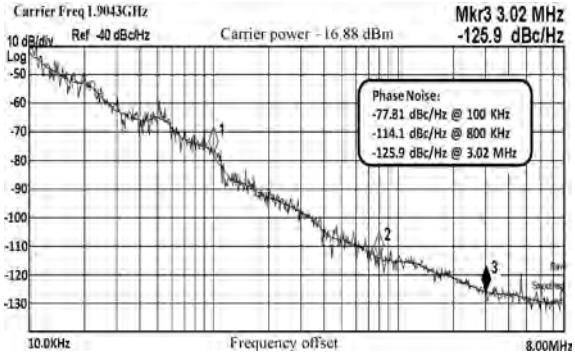

Fig. 19. Phase noise of the Freq1 @ 1.9 GHz.

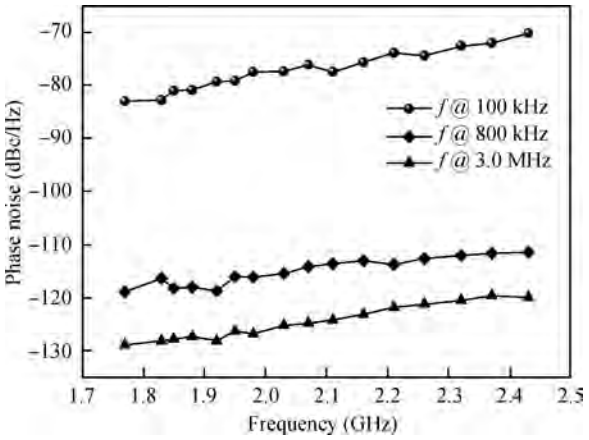

Fig. 20. The measured phase noise of Freq1 (1.75–2.5 GHz).

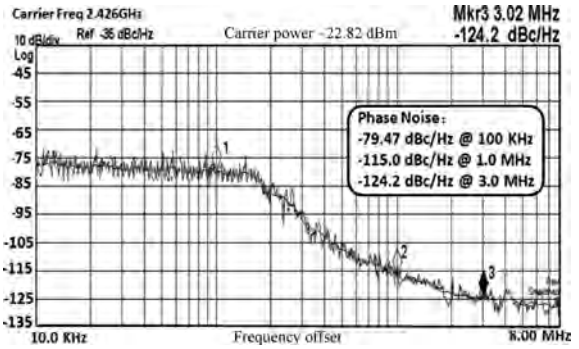

Fig. 21. The measured phase noise of the synthesizer @ 2.426 GHz.

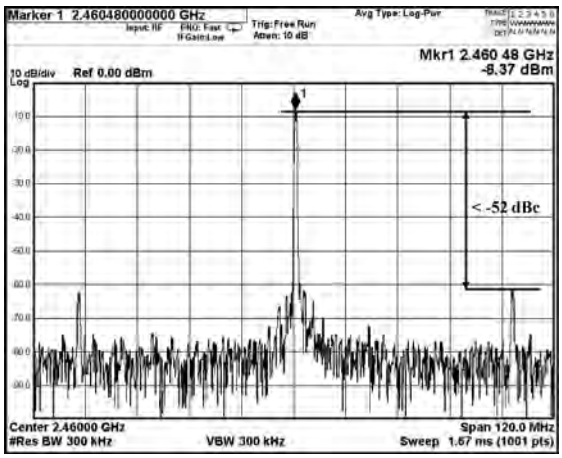

Fig. 22. The measured spectrum of the synthesizer @ 2.460 GHz.

pendence of the frequency on time shows that the frequency hopped rapidly from 2.404 to 2.422 GHz at 100 μs. The settling time is less than 5 μs, which is much shorter than a synthesizer without the frequency presetting function (35 μs).

Figure 19 shows the measured phase noise at 1.9 GHz when the VCO is free running at 3.8 GHz. The current from VCO to stacked divide-by-2 is about 1.2 mA. Figure 20 shows the measured phase noise of the Freq1 (1.75–2.5 GHz) when the LC-VCO is free running.

In order to fairly compare the overall performance of the LC-VCO in this paper with that of state-of-the-art CMOS realizations operating at different frequencies, tuning range and power level, we make use of the following figure of merit (FOM)[16]:

$$\mathrm{FOM} = L(\Delta f) - 20\lg\frac{f_0}{\Delta f} + 10\lg\frac{P}{1\,\mathrm{mW}} - 20\lg\frac{\mathrm{FTR}}{10}, \quad (5)$$

where f_0 is the oscillation frequency, $L(\Delta f)$ is the phase noise measured at an offset Δf from f_0, P is the DC power dissipation in the VCO and FTR is the frequency tuning range in percent. Table 1 shows the comparison of the normalized FOM.

Figure 21 shows the measured phase noise of the PLL

Table 1. Comparison of the normalized FOM.

Reference	Frequency range (GHz)	Tuning range (%)	Power (mW)	Phase noise @ 1 MHz (dBc/Hz)	FOM	Process
Ref. [17]	1.4–1.52	8.20	6.5	–129.8	–183.5	0.18 μm CMOS
Ref. [18]	1.67–1.9	12.8	17.6	–126.1	–180.9	0.18 μm CMOS
Ref. [19]	1.86–2.01	7.8	0.5	–111.0	–177.4	0.18 μm CMOS
Ref. [20]	1.8–2.0	10.5	4.8	–125.0	–178.6	0.18 μm CMOS
Ref. [21]	2.56–2.65	5.8	1.5	–119.2	–180.8	0.18 μm CMOS
Ref. [22]	1.9–2.33	20.3	3.8	–118.2	–183.5	0.18 μm CMOS
Our work	1.75–2.54	36.8	2.0	–118.5	–193.5	0.18 μm CMOS

Table 2. Frequency synthesizer performance comparison.

Parameter	Ref. [23]	Ref. [24]	Ref. [25]	Ref. [26][a]	This work
Process (CMOS)	0.18 μm	0.18 μm	0.18 μm	0.13 μm	0.18 μm
Area (mm^2)	6.25 (with pads)	4.8	2.5 (with pads)	0.04	1.6 (with pads)
Voltage (V)	1.8	1.8	1.8	0.5	1.8
Power (mA)	23	20	12.8	2.5	4.35
Frequency range (GHz)	0.94–1.72, 0.47–0.86, 0.156–0.287	2.4–2.5	1.91–2.79	0.31–0.61	1.75–2.54, 0.87–1.27[b], 0.58–0.85, 0.29–0.425
Loop bandwidth (kHz)	NA	$\sim$ 730	$\sim$ 120	NA	$\sim$ 110
Phase noise (dBc/Hz)	–130 @ 1.45 MHz f = 1.8 GHz	–124 @ 3 MHz f = 2.4 GHz	–101.1 @ 1 MHz f = 2.4 GHz	–95 @ 1 MHz f = 550 MHz	–115.0 @ 1 MHz f = 2.42 GHz
Wave type	I/Q	Differential	Differential	Differential	I/Q
Architecture	Fractional-N	Fractional-N	Fractional-N	Integer-N	Fractional-N

[a] The VCO is 3-stage ring oscillator. [b] This frequency band was obtained by the external divider-by-2 from Freq1 (1.75–2.54 GHz).

locked at 2.426 GHz. The measured phase noise at 1 MHz offset is –115.0 dBc/Hz and the in-band phase noise is about –80 dBc/Hz. The loop bandwidth is approximately 110 kHz. Figure 22 shows the measured spectrum of the PLL locked at 2.46 GHz. The reference spur is less than –52 dBc.

Table 2 shows a comparative study between the proposed low power multi-standard frequency synthesizer and some recently published ones. The power consumption is very low compared with other reports while achieving a larger frequency range.

5. Conclusion

We developed a low power fast settling multi-standard fractional-N frequency synthesizer. The multi-module current reusing, frequency presetting and NVM techniques are adopted to achieve the low power design and fast settling of the synthesizer. The synthesizer was implemented in a 0.18-μm CMOS process. All components in the frequency synthesizer are integrated on the chip and the area is about 1.6×1 mm^2 (including test pads). The measurement results show that its frequency range is from 0.3 to 2.54 GHz and the total current is about 4.35 mA @ 1.8 V supply voltage. The power is very low compared with other recently published examples. The LC-VCO exhibits an excellent FOM of –193.5 with the low power and large frequency range. The typical settling time is less than 5 μs over the entire frequency range.

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