A 700 V BCD technology platform for high voltage applications*

Qiao Ming(乔明)†, Jiang Lingli(蒋苓利), Zhang Bo(张波), and Li Zhaoji(李肇基)

State Key Laboratory of Electronic Thin Films and Integrated Devices, University of Electronic Science and Technology of China, Chengdu 610054, China

Abstract: A 700 V BCD technology platform is presented for high voltage applications. An important feature is that all the devices have been realized by using a fully implanted technology in a p-type single crystal without an epitaxial or a buried layer. An economical manufacturing process, requiring only 10 masking steps, yields a broad range of MOS and bipolar components integrated on a common substrate, including 700 V nLDMOS, 200 V nLDMOS, 80 V nLDMOS, 60 V nLDMOS, 40 V nLDMOS, 700 V nJFET, and low voltage devices. A robust double RESURF nLDMOS with a breakdown voltage of 800 V and specific on-resistance of 206.2 mΩ·cm^2 is successfully optimized and realized. The results of this technology are low fabrication cost, simple process and small chip area for PIC products.

Key words: BCD technology; fully implanted technology; double RESURF; LDMOS

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1. Introduction

Power ICs have been considered for such applications as switch mode power supplies, motor drives, automotive load switching, printers, displays, telecommunication switching, and others in which the operating voltages are in the range of 50 to 1200 V[1−7]. The continuous drive toward cost-effective integration of power and control functions on the same chip has provided improved performance, increased functionality, enhanced reliability and compact solutions in silicon utilization[7−11]. A SPIC (smart power IC) process with a wide range of devices up to 700 V has been reported[12, 13]. However, this process is complex and costly due to the formation of triple-well structures, and the specific on-resistance of the high voltage double RESURF (reduced surface field) LDMOS (lateral double-diffused MOSFET) is large due to the low n-well dose.

In this paper, an economical fully implanted BCD (bipolar CMOS DMOS) manufacturing process which requires less masking steps is developed by optimizing the integrated 700 V double RESURF nLDMOS (n-channel lateral double-diffused MOSFET) and 700 V nJFET (n-channel junction field effect transistor). This paper reports the structures, the fabrication process and the characteristics of the high voltage and low voltage devices. The major features of this 700 V BCD technology platform for high voltage applications have been clearly demonstrated.

2. Device structures and process

The design of the 700 V BCD technology is based on 2 μm CMOS production technology. A schematic cross-sectional view, showing the available BCD devices on a typical CMOS technology platform, is given in Fig. 1. An N-well is used to form the drift region of LDMOS, the n-type well of low voltage PMOS, and the collector region of NPN bipolar transistor. A P-well is adopted for forming the base region of NPN bipolar transistor, the p-type well of low voltage NMOS and high voltage LDMOS, and the p-type top layer of 700–200 V LDMOS. A broad range of MOS and bipolar components, including 700 V nLDMOS, 200 V nLDMOS, 80 V nLDMOS, 60 V nLDMOS, 40 V nLDMOS, 700 V nJFET, and low voltage devices, are compatible on a common p-type substrate. The highly compatible high voltage and low voltage devices result in the developed 700 V BCD technology platform having low fabrication cost, small chip area and simple process without epitaxial or buried layers.

Table 1 shows the comparison of the process flow for the developed 700 V BCD technology and the conventional SPIC process in Ref. [12]. Table 2 summarizes the electrical parameters for high voltage LDMOS, low voltage CMOS, BJT and poly resistor. In previous work, all the devices were realized by using a fully implanted triple-well technology in a p-type single crystal. Boron implantations are used three times to form P-base, P-well and p-type rings, respectively. In this work, conforming P-well technology for P-base, P-well and p-type rings is adopted for forming the base region of NPN bipolar transistor, the p-type well of low voltage NMOS and high voltage LDMOS, and the p-type top layer of 700–200 V LDMOS, simultaneously. So, two masking steps for the p-type regions are saved.

The 700 V BCD technology starts on p-type silicon with resistivity of 80–130 Ω·cm. At the beginning of the fabrication process, the wafer undergoes an implantation of phosphorous ions for the N-well. The choice of the N-well dose is based on the doping of the drift regions for high voltage LDMOS and high voltage JFET. N-well with depth of 5–9 μm is formed after the drive-in step at 1180 ℃. The higher dose for the N-well is helpful for realizing low specific on-resistance for high voltage LDMOS. After N-well implantation and drive-in, conforming P-well technology for P-base, P-well and p-type rings is adopted for forming the base region of the NPN bipolar tran-

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† Corresponding author. Email: qiaoming@uestc.edu.cn

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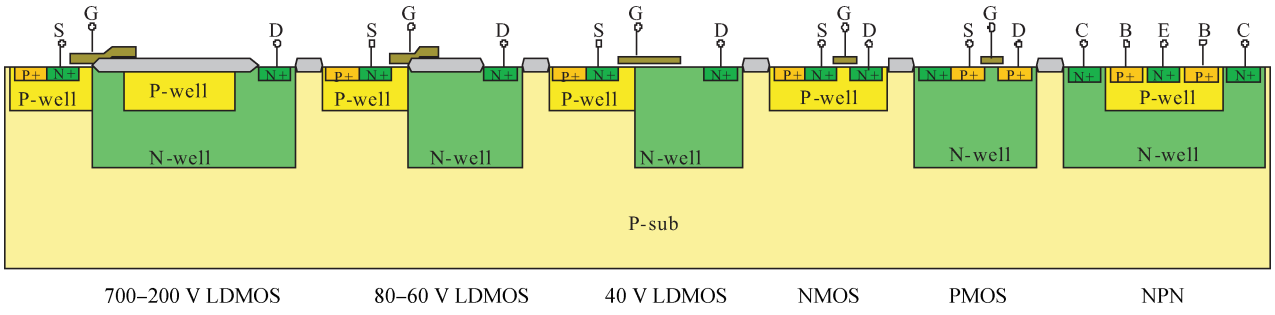

Fig. 1. Schematic cross-sectional view of 700 V BCD technology.

Table 1. Outline of process flow.

Previous process	Present process
P-substrate	P-substrate
N-well formation	N-well formation
P-base formation	Conforming P-well
P-well formation	technology for P-base,
P-type rings formation	P-well and p-type rings
Channel doping	Channel doping
Gate formation	Gate formation
Source and drain formation	Source and drain formation
Contact and metallization	Contact and metallization

Table 2. Electrical parameters for LDMOS, CMOS, bipolar and poly resistor.

LDMOS	BV_{dss} (V)	R_{sp} (mΩ·cm^2)
700 V LDMOS	800	206.2
200 V LDMOS	215	15.1
60–80 V LDMOS	98	5.0
40 V LDMOS	66	4.0
CMOS	V_T (V)	BV_{dss} (V)
NMOS	0.77	13.1
PMOS	–0.98	–15.0
Bipolar	BV_{CEO} (V)	BV_{CBO} (V)
BJT	20.7	33.0
Resistor	Res (Ω/□)	
Poly	26	

sistor, the p-type well of low voltage NMOS and high voltage LDMOS, and the p-type top layer of 700–200 V LDMOS. The depth of the P-well is about 1–2 μm. Local oxidation of silicon (LOCOS) technology is used to form the active region, and the thickness of the field oxide layer is about 0.6–0.7 μm. Then 30–50 nm gate oxide is grown, and polysilicon is deposited, doped and patterned. This is followed by masked implantation of n-type S/D and p-type S/D. Subsequently, a PMD (pre-metal dielectric) is deposited, in which contact windows are defined. Finally, Al–Si–Cu is deposited and patterned, and a passivation layer is applied.

3. Experimental results and discussion

3.1. High voltage LDMOS

RESURF technology is used for the design of high voltage LDMOS structures. Compared with the LDMOS with the breakdown voltage of less than 100 V, a p-type top layer is added for forming 700–200 V double RESURF LDMOS structures.

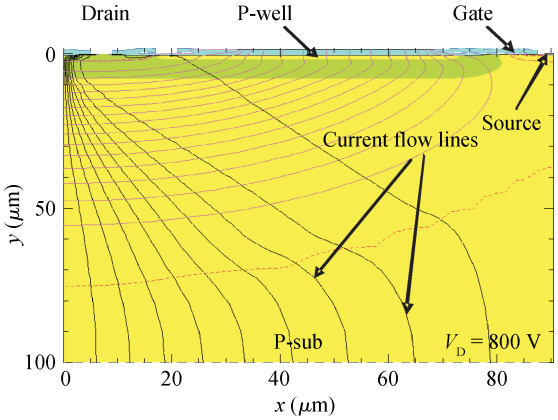

Fig. 2. The simulated potential contours of 700 V double RESURF LDMOS.

The 700 V double RESURF LDMOS shown in Fig. 1 is realized using 700 V BCD technology in TSUPREM4 and then imported into MEDICI for device simulations. Figure 2 shows the potential contours of the 700 V double RESURF LDMOS. The applied voltage to the drain electrode is 800 V, and the potential difference between two lines equals 50 V. In this structure, the p-type top layer formed by the conforming P-well technology is inserted in the top of the N-well drift region. The desired trade-off between breakdown voltage and the specific on-resistance are obtained by varying the dose of the N-well drift region and the p-type top layer. Figure 3 shows the simulated off-state breakdown voltage as a function of P-top dose with different N-well dose for 700 V double RESURF LDMOS. For the LDMOS with the breakdown voltage of over 700 V, there is a relevant P-top dose range with different N-well dose. The N-well dose can be chosen properly by the P-top dose, which is an important parameter for low voltage NMOS and NPN. Figure 4 shows the off-state breakdown voltage and the specific on-resistance as a function of N-well dose with P-well dope of 3×10^{12} cm^{-2} for 700 V double RESURF LDMOS. The breakdown voltage of the double RESURF LDMOS is dependent on the N-well dose in the drift region. The N-well dose has an optimum for a fixed P-well dose. The specific on-resistance is decreased with increasing the N-well dose. The experimental results, which are coincident with the simulated results, are also shown in Fig. 4. The measured breakdown voltage and specific on-resistance of the high voltage double

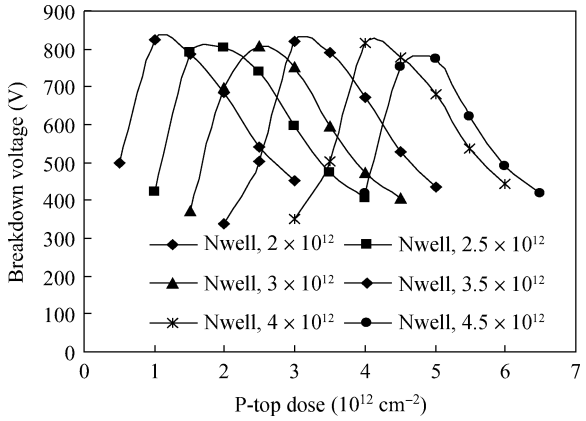

Fig. 3. The simulated off-state breakdown voltage as a function of P-top dose with different N-well dose for 700 V double RESURF LDMOS.

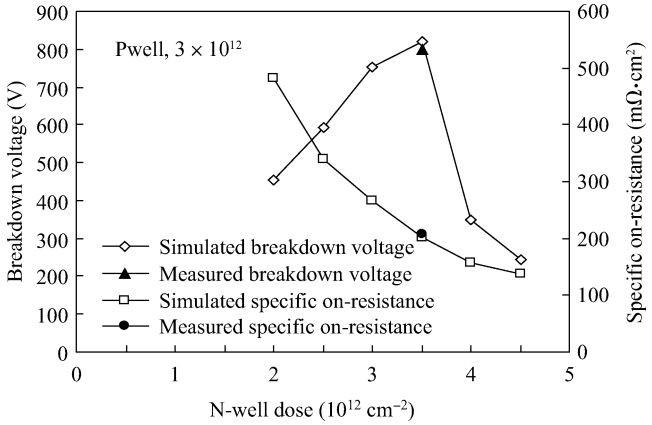

Fig. 4. Off-state breakdown voltage and specific on-resistance as a function of N-well dose with P-well dope of 3 × 10^{12} cm^{-2} for 700 V double RESURF LDMOS.

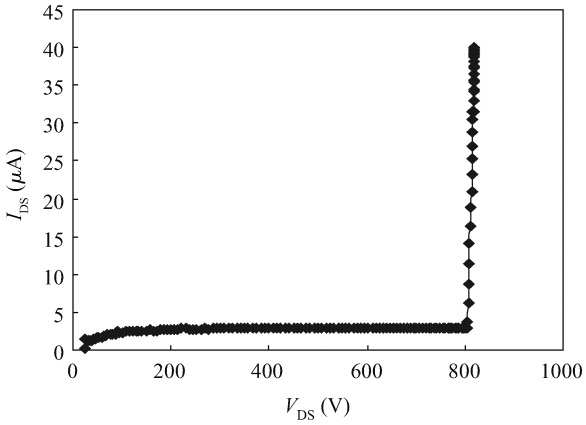

Fig. 5. The measured off-state breakdown characteristics of 700 V double RESURF LDMOS.

RESURF LDMOS are 800 V and 206.2 mΩ·cm^2, respectively. Figure 5 shows the measured off-state breakdown characteristics of the 700 V double RESURF LDMOS.

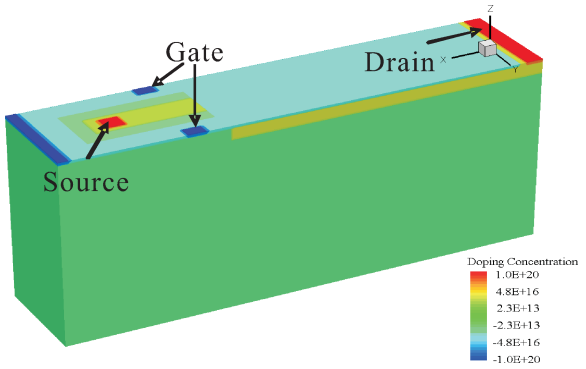

Fig. 6. The simulated structure for 700 V nJFET by ISE.

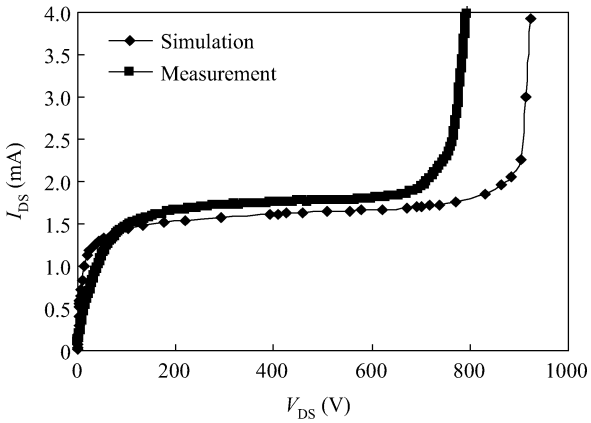

Fig. 7. Drain current characteristics for 700 V nJFET.

3.2. High voltage JFET

A versatile 700 V nJFET device can be used as internal power supply and current detector for SPIC. The nJFET device has similar structure as the double RESURF LDMOS for sustaining the breakdown voltage of over 700 V. So the nJFET can be parallel with the high voltage LDMOS. Figure 6 shows simulated structure for 700 V nJFET by ISE. Despite the voltage of the JFET device being up to 700 V at the drain electrode, the JFET conduction channel pinches off and keeps the voltage at the source electrode from 10 to100 V. When the power MOSFET is in the on state, the JFET device can be used to sense the drain current. It can be used as the detector for protecting the power MOSFET. Figure 7 shows simulated and measured drain current characteristics for 700 V nJFET.

3.3. Low voltage CMOS

The cross-sectional views of the low voltage NMOS and PMOS are also shown in Fig. 1. The low voltage PMOS is realized in the N-well, which is simultaneous with drift regions of high voltage LDMOS and JFET formed by phosphorous implantation and drive-in. The low voltage NMOS is fabricated in the P-well, which is simultaneous with the P-well region of high voltage LDMOS formed by boron implantation and drive-in. The measured drain current characteristics for the low voltage NMOS and PMOS are shown in Fig. 8. The threshold voltages of the NMOS are 0.77 V for NMOS and –0.98 V for PMOS, respectively. The breakdown voltages of the low

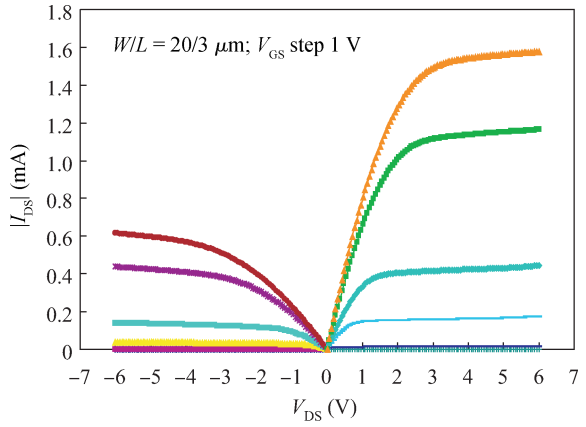

Fig. 8. Drain current characteristics for low voltage CMOS.

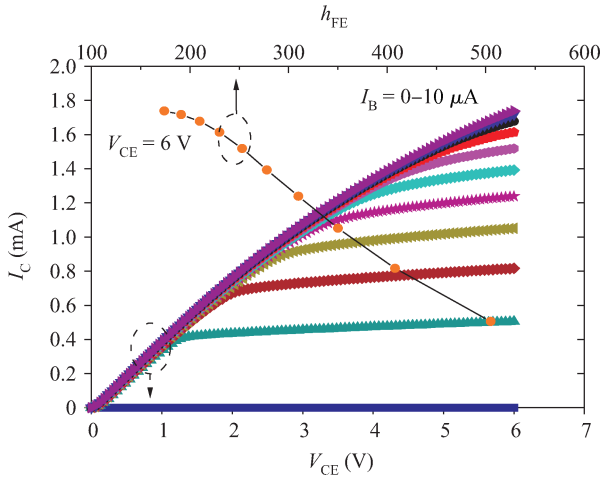

Fig. 9. I_C–V_{CE} and h_{FE}–I_C characteristics for NPN.

voltage CMOS devices are 13.1 V for NMOS and –15.0 V for PMOS, respectively.

3.4. Low voltage BJT

A NPN type BJT is also fabricated using this technology. Figure 9 shows the measured collector current (I_C) versus V_{CE} and current gain (h_{FE}) versus I_C for NPN. The doping and the junction depth of p-well region will affect the current gain and breakdown voltage of the NPN. The emitter and collector regions are realized using the implantation of n-type S/D.

4. Conclusion

A fully implanted 700 V BCD technology platform without epitaxial or buried layers is developed for high voltage applications. Conforming P-well technology for the P-base, P-well and p-type rings is adopted for forming the base region of an NPN bipolar transistor, the p-type well of low voltage NMOS and high voltage LDMOS, and the p-type top layer of 700–200 V LDMOS simultaneously without additional mask and process. A robust 700 V double RESURF nLDMOS and a 700 V nJFET are successfully optimized and realized. The measured breakdown voltage and specific on-resistance of the high voltage double RESURF LDMOS are 800 V and 206.2 mΩ·cm^2 respectively. This fully implanted 700 V BCD technology is expected to make significant impact on the highly demanded PIC market.

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