# A constant loop bandwidth fractional-*N* frequency synthesizer for GNSS receivers

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**Abstract:** A constant loop bandwidth fractional-*N* frequency synthesizer for portable civilian global navigation satellite system (GNSS) receivers implemented in a 130 nm 1P6M CMOS process is introduced. Via discrete working regions, the LC-VCO obtains a wide tuning range with a simple structure and small VCO gain. Spur suppression technology is proposed to minimize the phase offset introduced by PFD and charge pumps. The optimized bandwidth is maintained by an auto loop calibration module to adjust the charge pump current when the PLL output frequency changes or the temperature varies. Measurement results show that this synthesizer attains an in-band phase noise lower than –93 dBc at a 10 kHz offset and a spur less than –70 dBc; the bandwidth varies by ± 3% for all the GNSS signals. The whole synthesizer consumes 4.5 mA current from a 1 V supply, and its area (without the LO tested buffer) is 0.5 $mm^2$.

**Key words:** constant loop bandwidth; GNSS; frequency synthesizer; VCO
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## 1. Introduction

GNSS (global navigation satellite system) is a wireless navigation system. The GPS and GLONASS systems provide civil navigational services, and Galileo and Compass-II are being built with expeditious speed. Before long, future GNSSs will be multiple systems and achieve shared services through compatible and interoperable collaboration. Moreover, the portable equipment requires lower power, more integration and costs less for the RF front-end[1, 2]. Consequently, it is necessary to design a low-power, high-performance, wide-band frequency synthesizer.

Loop bandwidth affects the parameters of the PLL frequency synthesizer, which are phase noise, reference spur and settling time[3]. If loop bandwidth is unreasonable, it will reduce the capability of GNSS receivers. Hence, loop bandwidth should be optimized under idiographic instances. However, when output frequency changes to a new frequency or the process, temperature and supply voltage (PVT) bring an offset in a wide-band PLL, the bandwidth will fall into a sub-optimized situation. Until now, the most popular solutions to get an optimized loop bandwidth in a wide-band PLL have been to adopt adaptive[4] and constant[5] loop bandwidth. Adaptive bandwidth is a wide bandwidth that is set before lock, and the bandwidth is then optimized after the PLL is locked. Nevertheless, it is difficult to get an optimized bandwidth when the loop parameters are changed, a method only seen in ring oscillator PLLs. Constant bandwidth retains an optimal performance when the output frequency and PVT change. However, the present schemes ground on the analog split-tuned VCO, which needs a dual-loop PLL or a complicated charge pump.

To resolve the above problems, a constant loop bandwidth in a wide-band digital split-tuned LC-VCO-based PLL frequency synthesizer is proposed in this paper. The loop filter parameters in the GNSS receiver are analyzed and constant bandwidth PLL architecture is proposed. The circuit design of the key PLL modules is elaborated.

## 2. Analysis of the constant loop bandwidth in a wide-band frequency synthesizer

### 2.1. Analysis of the third-order loop filter characteristics in the GNSS receiver

Owing to the factual received GNSS signals are quite small, especially in urban, canyon and forest areas, a low phase noise frequency synthesizer is needed for good sensitivity. The bandwidth of closed-loop PLLs is critical, and affects the phase noise of the frequency synthesizer. The in-band phase noise is contributed by PFDs, dividers, reference TCXOs and loop filters; VCOs, reference spurs and sigma–delta quantization noise decide the phase noise out of band. Moreover, the PLL setting time is affected by the bandwidth. A 120 kHz bandwidth is chosen as the optimal value, and has the advantage of good phase noise in band. The reference spur and modulator quantization noise were rejected well.

GPS, GLONASS, Compass-II and Galileo are the four representative navigation systems; the frequency distribution of GNSS signals is listed in Table 1. A third-order loop filter is designed with 100 kHz bandwidth and 60° phase margin on 1176.45 MHz, and VCO gain $K_{VCO}$ are normalized. Transformation of the loop parameters is achieved with a variation in signal frequency and PVT, as shown in Fig. 1. When the signal frequency varies from 1176.45 to 1605.375 MHz, the bandwidth changes from 100 to 191 kHz, and the phase margin shifts from 39.5 to 60.6°.The bandwidth and phase margin

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Table 1. The frequency distribution of the GNSS signals.

| | GPS | | | GLONASS | | Galileo | | | Compass-II[6] | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Band | L1 | L2 | L5 | L1 | L2 | E5a | E5b | E2-L1-E1 | B1 | B2 | B3 |
| Frequency (MHz) | 1575.42 | 1227.6 | 1176.45 | 1598.0625 — 1605.375 | 1242.9375 — 1248.625 | 1176.45 | 1207.14 | 1575.42 | 1559.052 — 1591.788 | 1166.22 — 1217.37 | 1250.618 — 1286.423 |

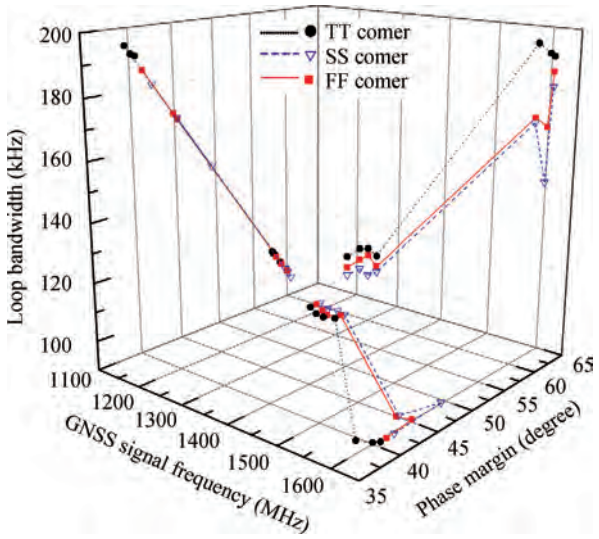


Fig. 1. Effect of frequency and PVT variation on the loop filter.

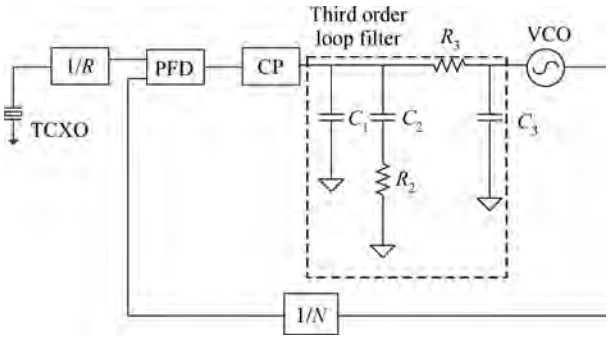


Fig. 2. Block diagram of a simplified PLL.

have a visible movement when the PVT is altered. The phase noise in the closed-loop PLL isn't an optimal value, and the loop will drop into the instable state at some signal frequencies. Consequently, it is necessary to keep a constant bandwidth at an optimal value over different GNSS signals and variations of PVT.

Figure 2 shows a simplified type-II PLL block diagram. The loop gain $G(s)$ equals

$$G(s) = \frac{I_{CP}}{2\pi}\frac{K_{VCO}}{S}\frac{R}{N}Z(s), \tag{1}$$

where $I_{CP}$ is the charge pump (CP) current, $K_{VCO}$ is the VCO gain of control voltage to oscillation frequency, $R$ is the reference divider ratio, $N$ is the main divider ratio, and $Z(s)$ is the impedance of the loop filter. The loop bandwidth and phase margin can be calculated, based on Banerjee's maximal phase margin method[7]:

$$\omega_C \approx \frac{RI_{CP}K_{VCO}}{N}\frac{R_2C_2}{C_1+C_2+C_3}, \tag{2}$$

$$\begin{aligned}\phi &= 180^\circ + \tan^{-1}(\omega_c T_2) - \tan^{-1}(\omega_c T_1) - \tan^{-1}(\omega_c T_{31}) \\ &= 180^\circ + \tan^{-1}(\omega_c R_2 C_2) - \tan^{-1}\left(\omega_c \frac{R_2C_1C_2}{C_1+C_2}\right) \\ &\quad - \tan^{-1}\left(\omega_c \frac{R_3C_3(C_1+C_2+C_3)}{R_2C_1C_2}\right),\end{aligned} \tag{3}$$

where $\omega_C$ is the bandwidth and $\phi$ is the phase margin. The bandwidth is affected by the variation in $I_{CP}$, $K_{VCO}$, $R$ and $N$ from Eq. (2) if a passive loop filter is selected out of chip. The $K_{VCO}$ in an LC-VCO can be obtained as

$$K_{VCO} = \frac{df_{VCO}}{dV_{ctrl}} = \frac{df_{VCO}}{dC_{var\_eff}}\frac{dC_{var\_eff}}{dV_{ctrl}}, \tag{4}$$

where $f_{VCO}$ is the VCO oscillation frequency, $V_{ctrl}$ is the VCO control voltage, and $C_{var\_eff}$ is the VCO effective varactor. Thereby, if $I_{CP}$ satisfies the following relation:

$$I_{CP} \propto \frac{N}{R}\frac{1}{K_{VCO}} \propto \frac{N}{R}\frac{1}{dC_{var\_eff}/dV_{ctrl}}, \tag{5}$$

from Eqs. (2), (4) and (5), a constant loop bandwidth can be maintained in spite of the PLL output frequency changing or the variation in PVT. Then the phase margin also remains the same from Eqs. (3) and (5).

### 2.2. PLL architecture

Condition (5) is necessary in order to get a constant loop bandwidth, the $R$ can be omitted if the same $R$ chose all the GNSS signals. Therefore, the fractional-$N$ frequency synthesizer is selected for the uniform $R$, which can gain better phase noise in-band and shorter lock time. Figure 3 shows the architecture of the proposed synthesizer for a universal portable GNSS receiver. A wide-band VCO works on discrete regions, with tuning curve linearization ensuring a wide tuning range and constant $K_{VCO}$. An improved PFD/CP minimizes the sink and source current mismatch and timing mismatch. A TSPC multi-modulus divider based on the pulse swallow is implemented for low power. Adaptive frequency calibration (AFC) is used to find the correct tuning curve when the chip powers on or the signal frequency is changed. Auto loop calibration (ALC) makes a wide bandwidth before PLL lock and maintains constant bandwidth when PLL is locked. At the same time it rectifies the VCO current to get an optimal performance of phase noise and power.

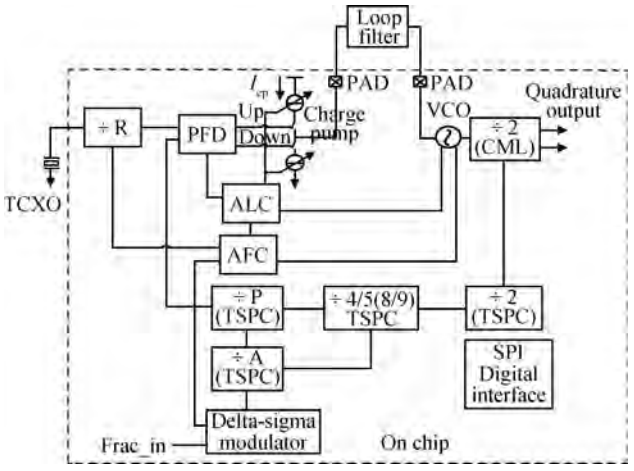


Fig. 3. Block diagram of the proposed frequency synthesizer.

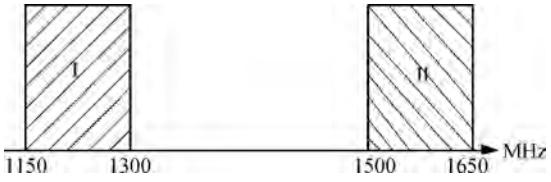


Fig. 4. GNSS signal frequency regions.

## 3. Circuit design

### 3.1. Discrete working regions of the LC-VCO

GNSS signal frequency is centralized in region I (1150 to 1300 MHz) and region II (1500 to 1650 MHz), as shown in Fig. 4, and there is an ineffective 400 MHz district in the VCO tuning range. Hence, we need to design an LC-VCO with discrete working regions that optimize regions I and II separately and conserve the area.

If $K_{\rm VCO}$ is constant in the whole VCO tuning range, then the $I_{\rm CP}$ satisfying condition (5) is easier than in conventional VCO because the parameter $K_{\rm VCO}$ can be omitted. A linear tuning curve technique[8] is adopted to keep $K_{\rm VCO}$ constant in every single tuning curve, and then condition (5) is translated to

$$I_{\rm CP} \propto \frac{N}{R}\frac{1}{\alpha}, \quad \alpha = \frac{K_{\rm VCO}}{K_{\rm VCOmax}}, \tag{6}$$

where $K_{\rm VCOmax}$ is the VCO gain of the maximal frequency corresponding tuning curve and $K_{\rm VCO}$ is the VCO gain on the other tuning curves. Discrete LC-VCO working regions with tuning curve linearization are proposed to keep a constant $K_{\rm VCO}$ in the same $C$–$V$ curve and cover all the GNSS signal frequencies, as shown in Fig. 5. A PMOS-only VCO-core topology with a current source to supply is selected for lower phase noise since PMOS transistors have less flicker noise. MP1 and MP2 are the cross-coupled pair that generate negative resistance to compensate the equivalent resistance of the LC tank. MP3 and MP4 are the current source. $R_1$ and MP5 compose low-pass filters to filter the $1/f$ noise from the current source, which deteriorates the phase noise through up-conversion to the LC tank. The VCO power can be calculated by the energy conservation theorem:

$$P_{\rm c} = \frac{R_{\rm s}I_{\rm p}^2}{2} = \frac{R_{\rm s}CV_{\rm p}^2}{2L}, \tag{7}$$

where $R_{\rm s}$ is the tank inductor series resistance, $I_{\rm p}$ is the peak amplitude current through the inductor, $V_{\rm p}$ is the peak amplitude voltage of the VCO sine wave output, $C$ is the total tank capacitor, and $L$ is the tank inductor. It should therefore maximize $L$ and minimize $R_{\rm s}$ for low power; $C$ and $V_{\rm p}$ were optimized previously based on the frequency tuning range and phase noise. $R_{\rm s}$ is minimized by choosing top metal as the inductor. $I_{\rm REF}$ is adjustable to get an optimal tradeoff between power and phase noise.

A switched capacitor array is controlled by a three bits band-code, as shown in the right part of Fig. 5. MSD B2 switches the working region between I and II, and B1, B0 control the capacitors for covering the range of the region and the offset produced by PVT variation. $C$ are switched capacitors and MN11 is a switch, which should have a large size for good phase noise. MN12 and MN13 supply a DC bias voltage to avoid a float state for $C$ when MN11 is on, similarly MP12 and MP13 supply a DC bias voltage when MN11 is off. MN12, MN13, MP12 and MP13 choose the unit size for reducing the parasitical capacitor and saving area. B2 controlled $C$ capacitors should choose carefully to locate the LO frequency in regions I and II, when the MN11 switch is on and off. The configuration of the control capacitor bank controlled by B1, B0 is similar to B2, whereas the capacitors and switches are binary weighted.

The varactor is compensated for linearization in the effective $V_{\rm ctrl}$, and the configuration is illustrated in the bottom-left part of Fig. 5. Two series connected A-MOSs $C_{\rm var1}$, $C_{\rm var2}$ with offset DC bias voltage $V_{\rm B1}$ and $V_{\rm B2}$, similar connection in the other hand for differential symmetry. $V_{\rm ctrl}$, through resistor R, connects the gate of two A-MOSs. When $V_{\rm ctrl}$ changes from 0 to 1 V, the gate-bulk voltage of $C_{\rm var1}$ is changed from $-V_{\rm B1}$ to $(1 - V_{\rm B1})$ V, while that of $C_{\rm var2}$ is biased from $-V_{\rm B2}$ to $(1 - V_{\rm B2})$V. The offset bias voltage is equal to $V_{\rm B1} - V_{\rm B2}$. The $C$–$V$ curve of equivalent varactor $C_{\rm var\_eq}$ between $C_{\rm var1}$, $C_{\rm var2}$ is moved by $V_{\rm B1} - V_{\rm B2}$. The voltage of $V_{\rm B1}$ is zero in our design. $C_{\rm var\_eq}$ can be calculated as:

$$\begin{aligned} C_{\rm var\_eq}(V_{\rm ctrl}) &= \frac{C_{\rm var1}(V_{\rm ctrl} - V_{\rm B1})C_{\rm var2}(V_{\rm ctrl} - V_{\rm B2})}{C_{\rm var1}(V_{\rm ctrl} - V_{\rm B1}) + C_{\rm var2}(V_{\rm ctrl} - V_{\rm B2})} \\ &= \frac{C_{\rm var1}V_{\rm ctrl}C_{\rm var2}(V_{\rm ctrl} - V_{\rm B2})}{C_{\rm var1}V_{\rm ctrl} + C_{\rm var2}(V_{\rm ctrl} - V_{\rm B2})}. \end{aligned} \tag{8}$$

### 3.2. Phase frequency detector and configurable charge pump

Reference spurs are spurious tones that appear at multiples of $f_{\rm REF}$ from $f_{\rm LO}$, and result mainly from periodic disturbances of the loop filter voltage ($V_{\rm ctrl}$) introduced by the chare pump. The amount of reference spur in the PLL[9] is approximately calculated by

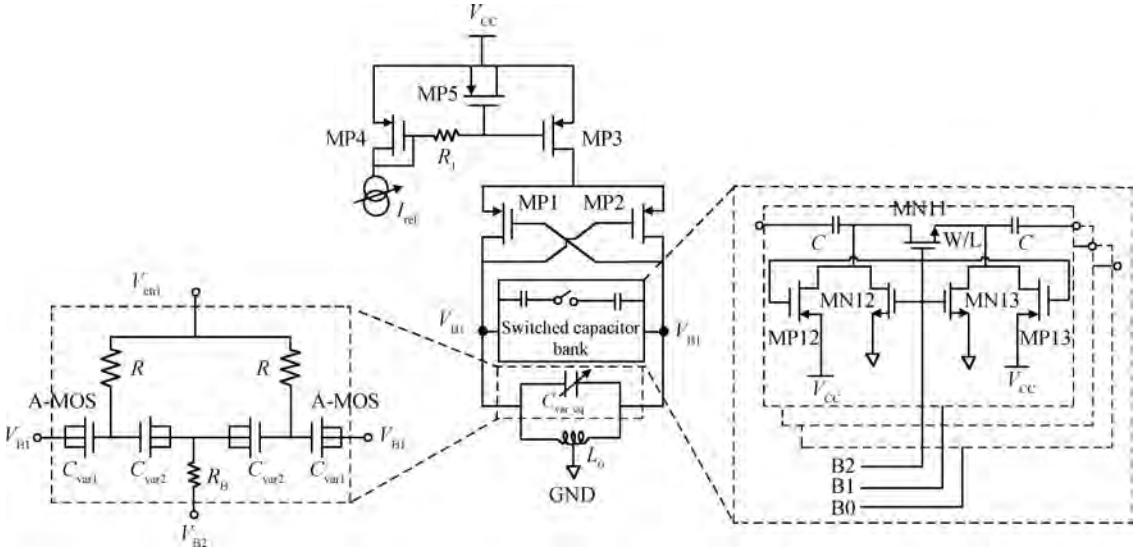


Fig. 5. Schematic of the proposed LC-VCO.

$$
\begin{aligned}
P_{\mathrm{r}} &= 20\lg\left(\frac{1}{\sqrt{2}}\frac{\omega_{\mathrm{c}}}{\omega_{\mathrm{ref}}}N\varphi\right) - 20\lg\frac{\omega_{\mathrm{ref}}}{\omega_{\mathrm{p1}}},\\
\varphi &= \varphi_{\mathrm{l}} + \varphi_{\mathrm{cm}} + \varphi_{\mathrm{tm}},\\
\varphi_{\mathrm{l}} &= 2\pi\frac{\Delta I_{\mathrm{leak}}}{I_{\mathrm{cp}}},\\
\varphi_{\mathrm{cm}} &= 2\pi\frac{\Delta T_{\mathrm{on}}}{T_{\mathrm{ref}}}\frac{\Delta I_{\mathrm{mismatch}}}{I_{\mathrm{cp}}},\\
\varphi_{\mathrm{tm}} &= \frac{\Delta T_{\mathrm{on}}}{T_{\mathrm{ref}}}\frac{\Delta T_{\mathrm{mismatch}}}{T_{\mathrm{ref}}},
\end{aligned}
\tag{9}
$$

where $\omega_{\mathrm{p1}}$ is the first pole of the loop filter, $\varphi$ is the phase offset introduced by the leakage current, the mismatch of the charge pump current and the timing mismatch of the PFD and charge pump, $\Delta I_{\mathrm{leak}}$ is the leak current, $\Delta I_{\mathrm{mismatch}}$ is the mismatch of the charge pump sink and source current, $\Delta T_{\mathrm{on}}$ is the turn on time when PLL is locked, and $\Delta T_{\mathrm{mismatch}}$ is the timing mismatch of the PMOS charge pump and NMOS switches. The phase offset ($\varphi$) should be minimized to get a low reference spur and ensure optimized loop bandwidth and PLL settle time. The leakage current is almost eliminated by making a loop filter out of a chip and a VCO varactor in the N well with a guard ring. The mismatch from the current and delay is minimized by the proposed PFD and charge pump.

A PFD with equivalent differential delay output is shown in Fig. 6(a), which cooperates with a charge pump with complementary switches as shown in Fig. 6(b) to avoid a time mismatch. A configurable capacitor is introduced to eliminate the dead zone problem and minimize the turn on time ($\Delta T_{\mathrm{on}}$). The lock detector outputs the LD signal as the lock indication. The charge pump with drain switching adapts to low supply voltage applications, and has a fast switching-speed and low power at the cost of charge share. Charge share in switched capacitor circuits is discussed[10]. The sink and source current are mirrored from the same current source to decrease current mismatch. MP4 and MN7 are complementary switches, MP6 and MN6 are complementary dummy devices used to remove charge injection and clock feedback from MP4 and MN7, and the size of MP6 and MN6 is half that of MP4 and MN7. The topology is complementary in the pull-down circuit. A subtle configurable current source is also introduced, and the unit of the programmable current is 1 $\mu$A.

### 3.3. Adaptive frequency and auto loop calibration

A digital split-tuned wide-band VCO should have an AFC module to find the right tuning curve when the divider ratio $N$ changes or the chip is powered on. The open-loop method[11] doesn't suit our design due to the VCO working region not being consecutive. An AFC with improved calibration time, which is based on the closed-loop method[12], is illustrated in Fig. 7(a). A large current is chosen before PLL lock, which brings a fast charge, discharge and wide loop bandwidth. This method not only profits PLL lock, but also AFC calibration. A finite state machine (FSM) adopts the arithmetic of a dimidiate search, which runs an at most three times iterative search to complete the calibration. The programmable clock of the FSM is divided from the referenced frequency $f_{\mathrm{REF}}$, and a trade-off is made between fast and normal work.

An ALC is proposed to keep $I_{\mathrm{CP}}$ satisfying Eq. (6) for a constant loop bandwidth when PVT varies or the GNSS signal changes, and a block diagram is shown in Fig. 7(b). The $\alpha$ in Eq. (6) on a different process corner is obtained by post-simulation and embodied in the decoder. The enabled control unit detects the state of AFC_OK and LD, and if only one of them is low, the <S8:S0> is set high to obtain a wide bandwidth for a fast PLL lock and AFC calibration, and the <K3:K0> is set low to ensure reliable VCO oscillation. When AFC_OK and LD are high, the decoder is enabled. The first step configures $I_{\mathrm{CP}}$ scaled with the main divider ration $N$, then adjusts $I_{\mathrm{CP}}$ based on the VCO band-code<B2:B0>, which corresponds to the $\alpha$. In the last step, the decoder regulates the $I_{\mathrm{CP}}$ to achieve Eq. (5) grounded on <St1:St0>. The <St1:St0> is configured when the measured parameters of the chip is near the process corner, and the <K3:K0> is adjusted to an optimal value based on <B2:B0> and <St1:St0> for low power and good phase noise.

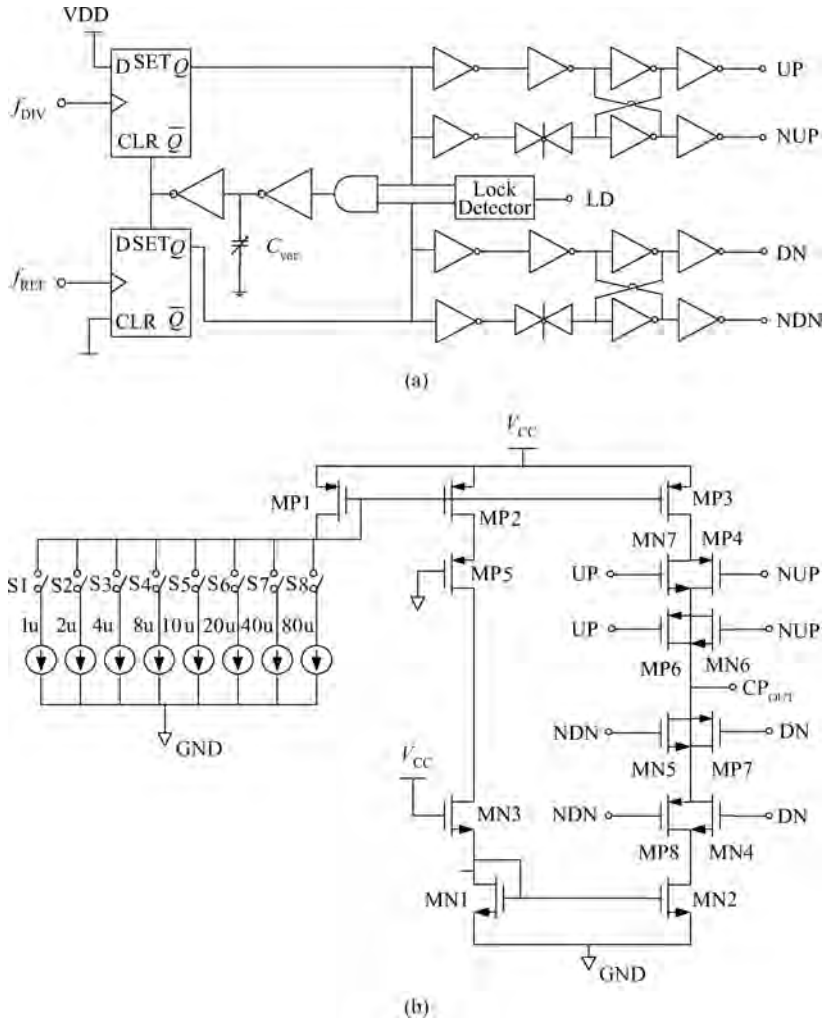


Fig. 6. (a) A simplified schematic of the PFD, and (b) schematic of the proposed charge pump.

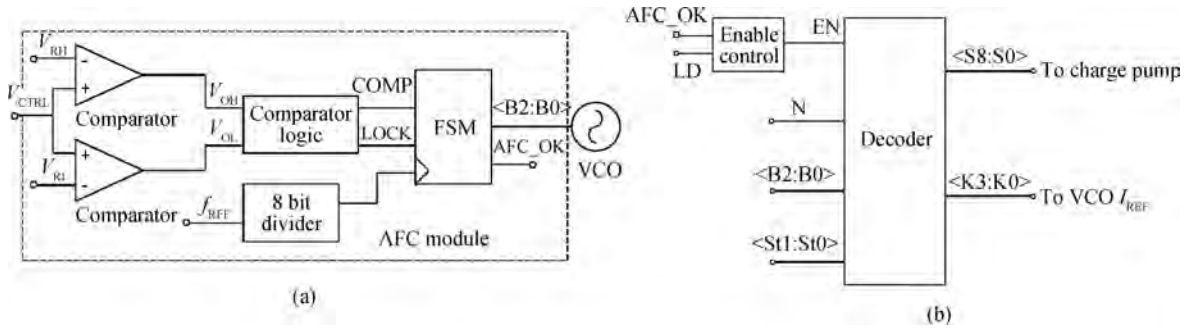


Fig. 7. Block diagrams of (a) the AFC and (b) the ALC.

## 4. Measurement results

The proposed fractional-$N$ frequency synthesizer as a key module of the GNSS receiver has been manufactured in a standard 0.13 $\mu$m 1P6M CMOS process, and is shown in Fig. 8. The whole frequency synthesizer occupies 0.5 mm$^2$ (without LO tested buffer), and consumes 4.5 mA with a 1 V power supply excluding the LO tested buffer. The most power-hungry blocks in PLL are VCO and the CML 2:1 frequency divider, and they consume 3 mA current in total. The frequency tuning curve ($F$–$V$) of the proposed PLL is measured at the LO tested buffer by fixing the feedback divider's ratio and changing the input reference frequency under PLL in a closed loop. The $F$–$V$ curve is shown in Fig. 9. The LO signal frequency changes from 1290 to 1110 MHz in region I, and from 1840 to 1440 MHz in region II. The frequency covers all the GNSS signals and process deviations, while the $V_{ctrl}$ varies from 0 to 1 V. It is evident that the FV curve is almost linear in the charge pump effective output range between 0.1 and 0.9 V.

The phase noise of the proposed frequency synthesizer is measured at the LO tested buffer. Figure 10 shows the measured LO signal power spectrum, and the corresponding phase

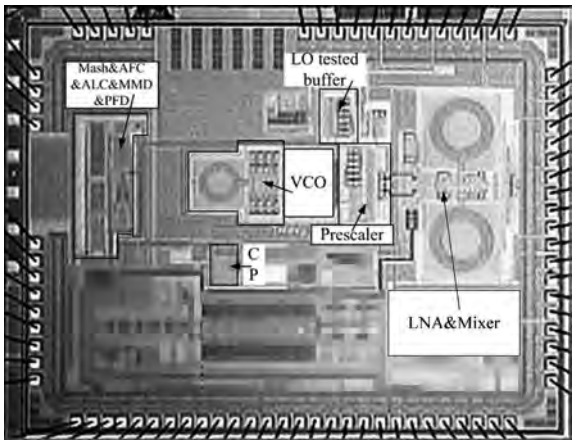


Fig. 8. Die micrograph.

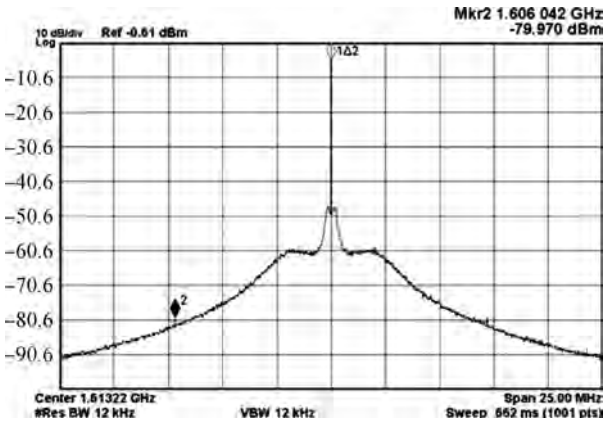


Fig. 11. LO signal in region II with a 25 MHz span.

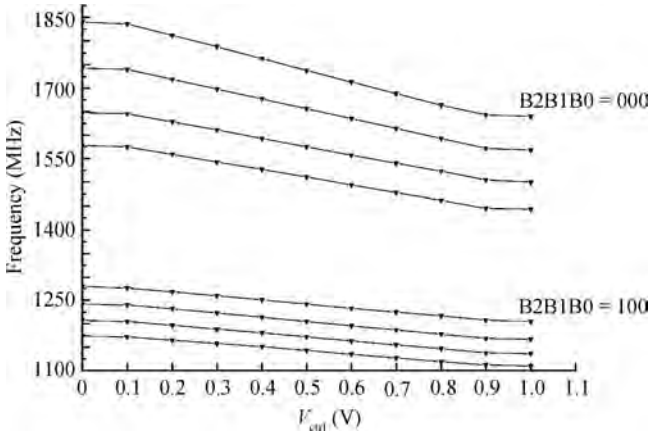


Fig. 9. The measured LO $F-V$ curve.

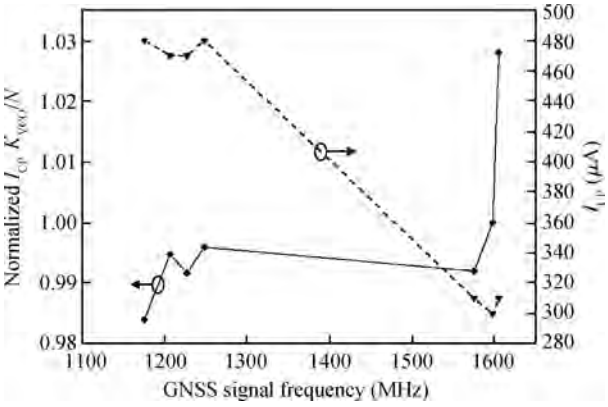


Fig. 12. Normalized $I_{CP}K_{VCO}/N$ and $I_{CP}$ on signal frequency.

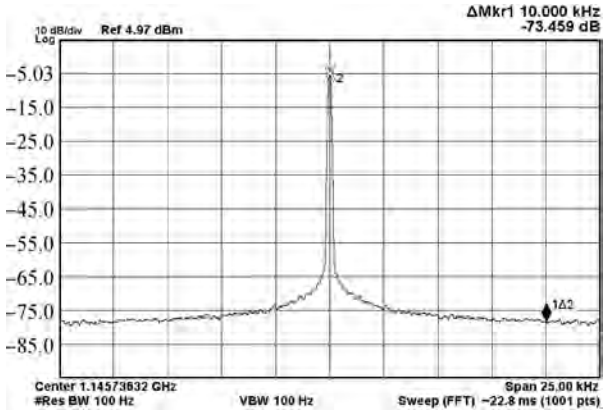


Fig. 10. LO signal in region I with a 25 kHz span.

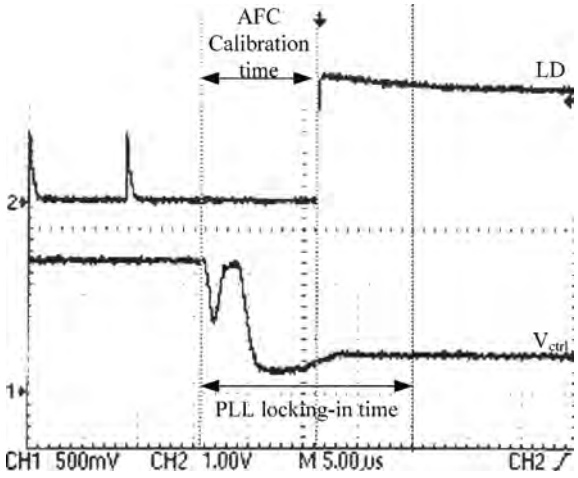


Fig. 13. The measured locking-in time.

noise of the proposed fractional-$N$ frequency synthesizer is better than –93 dBc at 10 kHz offset. The reference spur is less than –70 dBc, as shown in Fig. 11.

$K_{VCO}$ is calculated from the measured LO $F-V$ curve, $f_{REF}$ is chosen as 8.184 MHz, $K_{VCO}$ varies more than twice in the GNSS signals and $N$ changes from 143.7 to 196.2. ALC adjusts the $I_{CP}$ when PLL is locked for a 120 kHz optimal bandwidth, the variation of $I_{CP}K_{VCO}/N$, which is equivalent to a change in bandwidth, as shown in Fig. 12. It is limited to ±3% for any GNSS signals. The measured locking-in time of the proposed PLL is less than 20 $\mu$s, as shown in Fig. 13, which contains the AFC calibration time of about 10 $\mu$s. The performance comparison of the proposed PLL with other related frequency synthesizers is listed in Table 2.

Table 2. Performance comparison of the published frequency synthesizers.

| Parameter | This work | Ref. [5] | Ref. [13] | Ref. [14] |
|---|---|---|---|---|
| Technology | CMOS 130 nm | CMOS 130 nm | CMOS 130 nm | CMOS 130 nm |
| Center frequency (GHz) | 1.48 | 3.5 | 1.58 | 1.48 |
| Tuning range (%) | 50 | 22.8 | 25 | 32.4 |
| Phase noise (dBc/Hz) | –93 @ 10 kHz<br>–118 @ 1 MHz | –82.2 @ 10 kHz<br>–116 @ 1 MHz | –70 @ 100 kHz<br>–110 @ 1 MHz | –82 @ 1 MHz<br>–99 @ 10 MHz |
| Reference spur (dBc) | –70 | N/A | –65 | –47 |
| Power (mW) | 4.5 | 48 | 1.2 | 5.8 |

## 5. Conclusion

A constant loop bandwidth fractional-$N$ frequency synthesizer for GNSS receivers is proposed in this paper, and was designed and implemented in a 0.13 $\mu$m CMOS process. A constant loop bandwidth wide-band PLL is analyzed at length, and the wide-band LC-VCO has a linear tuning curve and a discrete working region. A low-power configurable charge pump with charge share cancellation reduces spurs. The ALC module configures the $I_{CP}$ to the maximum before PLL lock, and maintains constant bandwidth regardless of the variation in LO frequency and PVT when the PLL locked. The proposed fractional frequency synthesizer has been successfully applied to portable civilian GNSS receivers.

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