The realization of an SVGA OLED-on-silicon microdisplay driving circuit*

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Abstract: An 800 × 600 pixel organic light-emitting diode-on-silicon (OLEDoS) driving circuit is proposed. The pixel cell circuit utilizes a subthreshold-voltage-scaling structure which can modulate the pixel current between 170 pA and 11.4 nA. In order to keep the voltage of the column bus at a relatively high level, the sample-and-hold circuits adopt a ping–pong operation. The driving circuit is fabricated in a commercially available 0.35 μm two-poly four-metal 3.3 V mixed-signal CMOS process. The pixel cell area is 15 × 15 μm^2 and the total chip occupies 15.5 × 12.3 mm^2. Experimental results show that the chip can work properly at a frame frequency of 60 Hz and has a 64 grayscale (monochrome) display. The total power consumption of the chip is about 85 mW with a 3.3V supply voltage.

Key words: microdisplay; OLED-on-silicon; pixel; SVGA; 64 grayscale; buffer
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1. Introduction

Microdisplays have attracted much attention in recent years, and organic light-emitting diode-on-silicon (OLEDoS) is one of the new microdisplay technologies. OLEDoS has been widely studied in the past decade and has a number of attributes that make it uniquely suitable for microdisplay applications[1]. It has advantages such as self-emittance with a wider viewing angle, high contrast, fast response and a broad temperature range at low power consumption[2], and when combined with mature standard CMOS technology costs could be greatly reduced. With such superior performance, OLEDoS is considered as one of the most promising next-generation microdisplay technologies.

In this paper, as the OLEDoS pixel cell area is 15 × 15 μm^2, pixel currents between hundreds of picoamperes (pA) and tens of nanoamperes (nA) are required. In order to modulate pixel current at such a low level, three circuit structures are often used. The first is a current-mirror circuit[3], whose function is to convert the input signal into a current signal and then copy it onto the OLEDoS pixel cell. Due to a large interconnect parasitic capacitor, it is difficult to transform extremely small currents to a pixel cell at a high update rate (if the frame frequency is 60 Hz, sampling signals will be at tens of MegaHertz). The second structure is the three-transistor voltage-programmed pixel driver, which means that a third MOS transistor is made parallel with an OLED device to bypass the driving current and make the OLED current small enough[4, 5]. Unfortunately, the current flowing to the third MOS transistor is useless, so its power consumption is large. The third structure is the subthreshold-voltage-scaling OLED pixel driver topology[6], and its main principle is to make the pixel current transistor work at the subthreshold region. This structure has a relatively low power consumption and can work at a high sampling signal rate at the same time. The third structure is employed in this paper to satisfy the driving circuit specification requirements.

2. The design of the OLED-on-silicon driving circuit

2.1. OLED-on-silicon driving-circuit system architecture

The system-architecture diagram of the chip is shown in Fig. 1. It mainly consists of five parts: a 6 bit DAC, a buffer, a row and column scan driver circuit, a sample and hold circuit, and 800 × 600 pixel arrays. The 6 bit DAC converts the input 6 bit digital signals into analog current signals. Because of the large parasitic capacitor, a buffer is needed when the voltage signal is transferred from the DAC to the sample and hold circuit. By controlling the "TOP" and "BTM" switches on and off, we can realize two sample and hold circuits (on the top and bottom of the chip) to work alternately. The row scan driver coordinates with the column scan driver to send the signal to the pixel arrays. The layout of the entire microdisplay system is shown in Fig. 2, and the chip size is 15.5 × 12.3 mm^2.

2.2. The general working principle of the driving circuit

For the purpose of explaining the working principle of the driving circuit clearly, the 800 × 600 pixel cell arrays are simplified into a single pixel cell, and the timing requirements will be reduced at the same time. As shown in Fig. 3, a working schematic of a single pixel cell is divided into three parts (labeled by the dotted line boxes): DAC and buffer, sample-and-hold circuit, and pixel circuit. The working principle is: a 6 bit DAC converts a digital signal to current I_1; the current I (= I_1 + I_2) flowing into N1 (diode-connected) produces voltage V_1;

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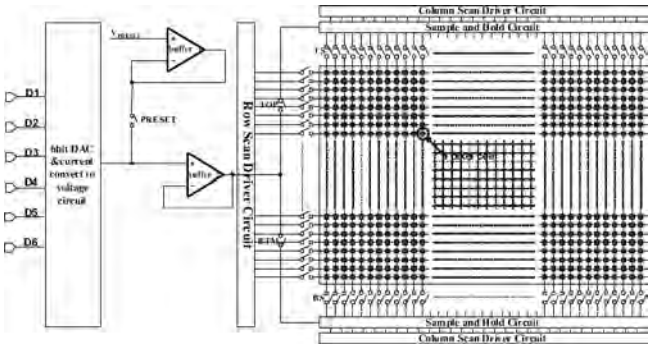

Fig. 1. Driving-circuit system architecture.

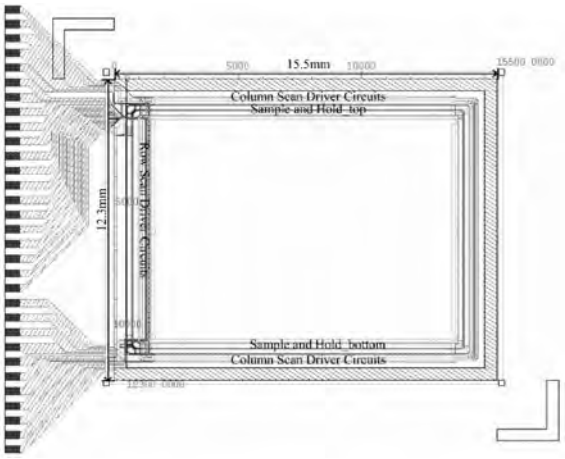

Fig. 2. The OLEDoS driving-circuit layout.

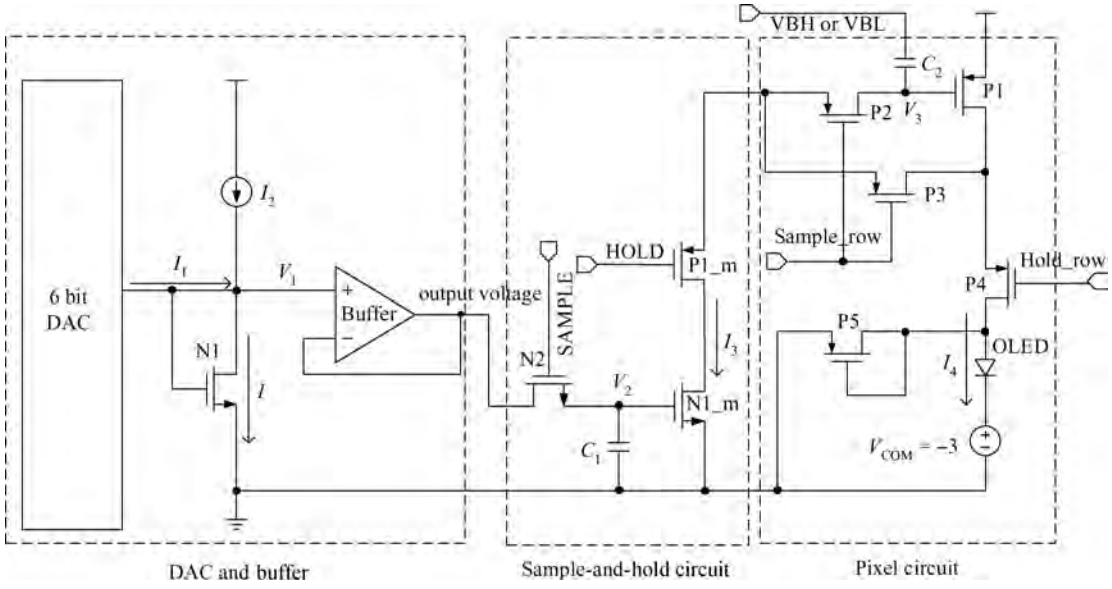

Fig. 3. A working schematic of driving a single pixel cell.

through the buffer, the voltage V_1 is sampled onto the capacitor C_1 when SAMPLE is high; with HOLD and sample_row turning to low level (hold_row is high), the current I_3 which is controlled by V_2 flow from P1 to N1_m and the corresponding voltage V_3 is stored on the capacitor C_2; as hold_row is low (sample_row is high), the voltage V_3 controls the current of P1, that is, the current I_4 flow into the OLED.

The detailed working principle, complete circuit diagrams and the parameter of the critical component will be described in the next three sections.

2.3. DAC and buffer

The DAC and buffer circuit is shown in Fig. 4. Typical binary weighted current scaling architecture is adopted by the 6 bit DAC, and a two-stage miller operation amplifier is used in the buffers. The output current of the 6 bit DAC is from 0 to 320 μA, and adds the current that flows from P1, so the total current (I_{total}) range is between 2 and 322 μA. The diode-connected MOS N1 produces a voltage according to I_{total}.

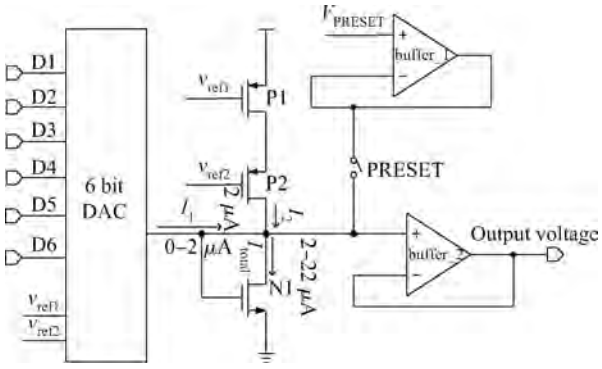

Fig. 4. A DAC and buffer circuit.

Because the aspect ratio of N1 is large (500 μm/2 μm), the parasitic capacitor will also be large. When I_{total} is at low current levels, the gate voltage of N1 cannot reach the final value within the time period given by the video sample signal

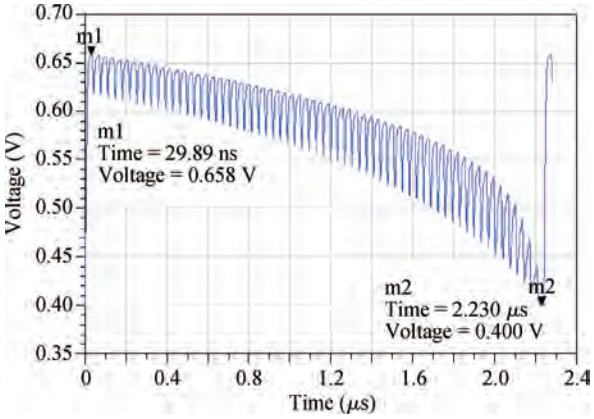

Fig. 5. Simulation result of the output of buffer_2.

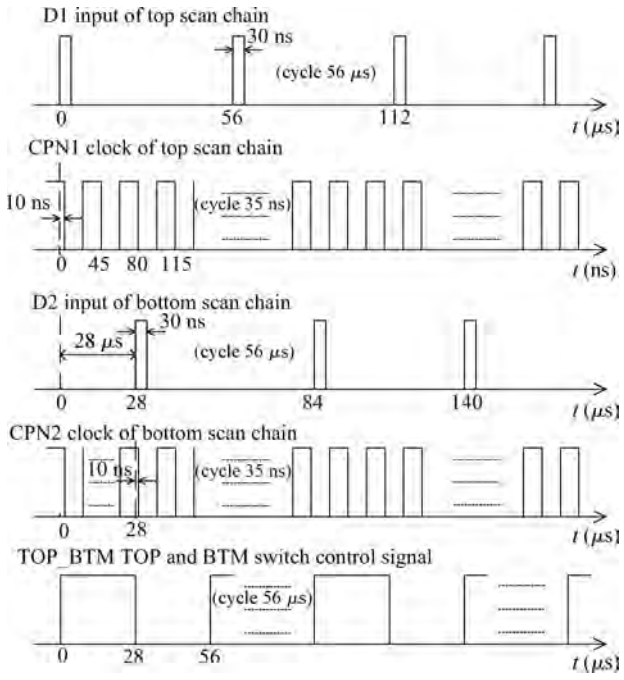

Fig. 6. Timing diagram for the sample-and-hold circuit.

(~ 35 ns, frame frequency 60 Hz). In order to settle this problem, the N1 gate is pre-charged to a voltage near the low current level by buffer_1. Buffer_2 isolates the capacitor seen at the N1 gate from the capacitor of the sample and hold circuit, and is also used to drive the sample and hold circuit. The simulation result of the output voltage of buffer_2 is shown in Fig. 5.

In addition, two off-chip precision resistors for the bandgap are used to generate two reference voltages (v_{ref1}, v_{ref2}) for the DAC's cascode current source.

2.4. The sample-and-hold circuit and the row, column scan drive circuit

The scan drive circuit is composed of the head and tail connected D flip-flop, which is a standard cell in a 0.35 μm CMOS mixed-signal process. The D flip-flop is negative edge triggered with active-low clear. The pixel cell in the sample phase or hold phase is controlled by a scan drive circuit.

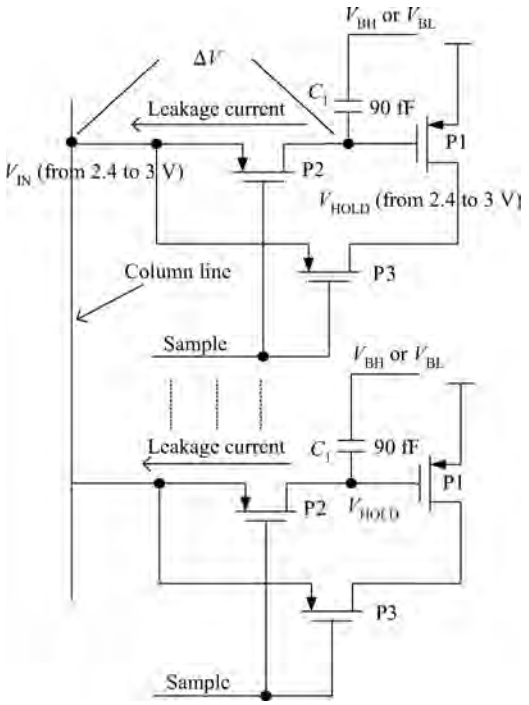

Fig. 7. Leakage current from C_1.

There are two sample-and-hold circuits along the top and the bottom of the pixel array (Fig. 1). During a line period, when switch TOP is on (TS off), the top sample-and-hold circuit will sample the voltage from buffer_2; at the same time, switch BTM is off (BS on), and the bottom sample-and-hold will write their data, which are sampling at the previous line period to the one row of the pixel array. At the next line period the operation is opposite. The timing diagram is shown in Fig. 6.

This ping–pong scan operation can keep the column line's voltage from dropping to the ground. Consequently, even though the storage capacitor in the pixel cell is small (90 fF), the voltage on the storage capacitor can have a long hold time. This situation can be simplified as in Fig. 7. When P2 is off, the less the ΔV ($|V_{\mathrm{IN}} - V_{\mathrm{HOLD}}|$) is, the less the leakage current from C_1 is. The simulation result is shown in Fig. 8. We can conclude that with the ping–pong operation, the voltage holding on C_1 only dropped 30 mV in a frame period in the worst case; without ping–pong operation (only one sample-and-hold circuit), V_{IN} may be 0 in the worst case and the voltage holding on C_1 dropped 412 mV. There is a difference of about 10 times between the two simulations.

The sample-and-hold circuit[6] is shown in Fig. 9. VIN is the output of buffer_2 (Fig. 4); signal SAMPLE, another output, controls N2 to be on or be off; in order to hold the voltage on the C_1 storage capacitor, C_1 should be relatively large (600 fF); N3 can reduce the clock feedthrough effect which is caused by the capacitive coupling between the N2 gate and the A node; N1_m with N1 (in Fig. 4) forms a current mirror structure, and the aspect ratio of N1_m is 5 μm/2 μm, with $(W/L)_{\mathrm{N1}}$ = 500 μm/2 μm. N1_m's output current, shown in Fig. 10, is from 3.365 μA to 21.69 nA. Compared to the output current of the DAC, N1_m's current decreases about 100 times.

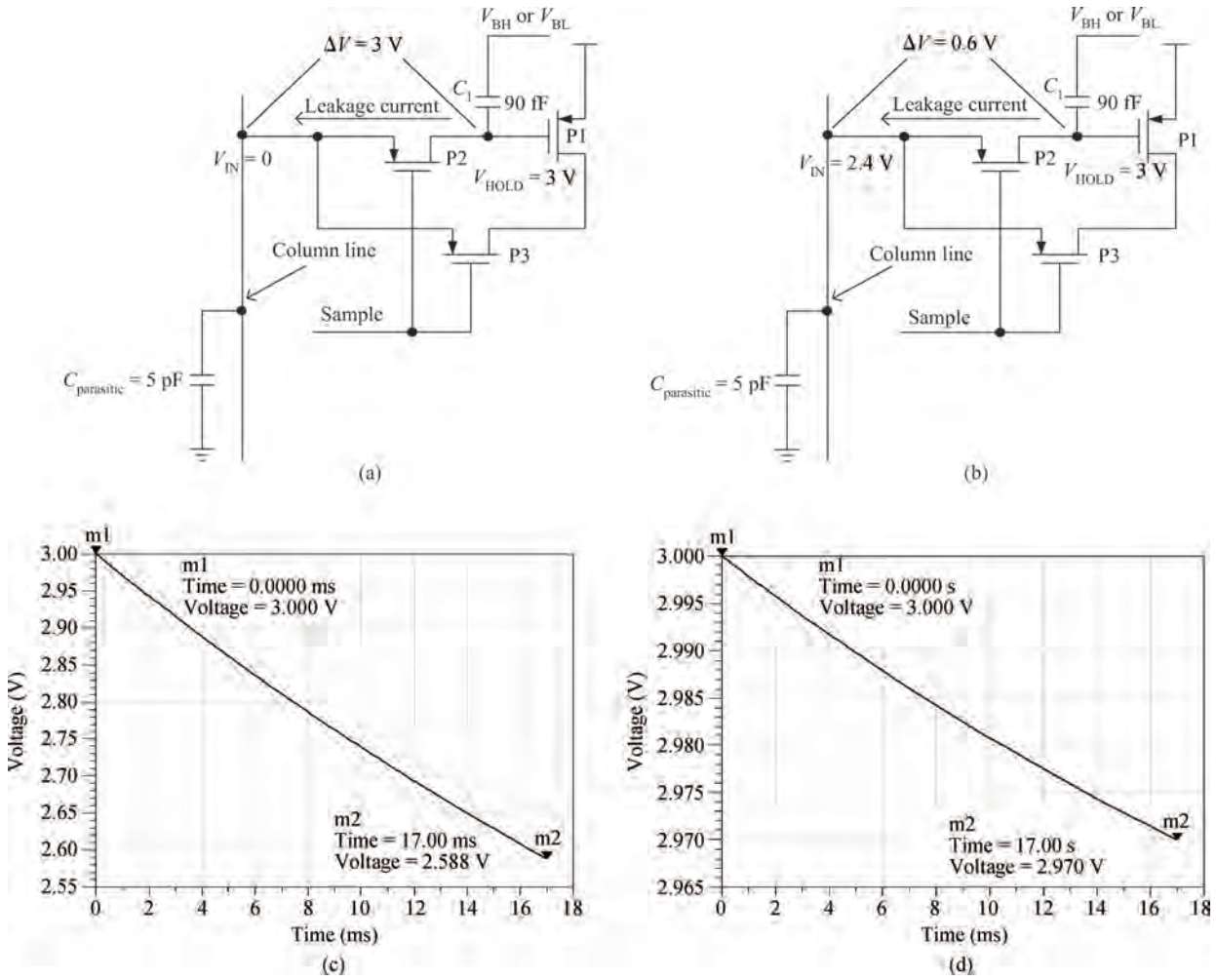

Fig. 8. Voltage between C_1 and $C_{\text{parasitic}}$ in difference value and simulation results. (a) $\Delta V = 3$ V. (b) $\Delta V = 0.6$ V. (c) Simulation result of $\Delta V = 3$ V. (d) Simulation result of $\Delta V = 0.6$ V.

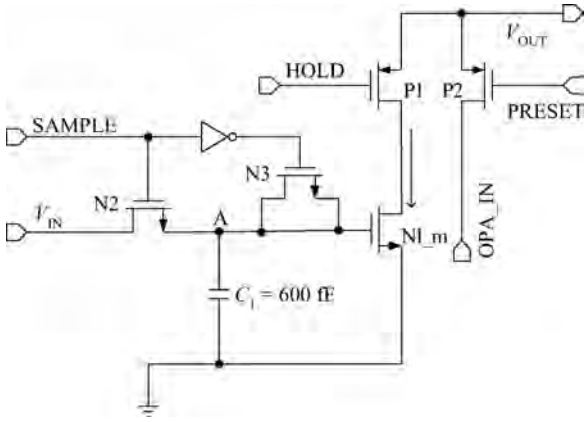

Fig. 9. Top and bottom sample-and-hold circuits.

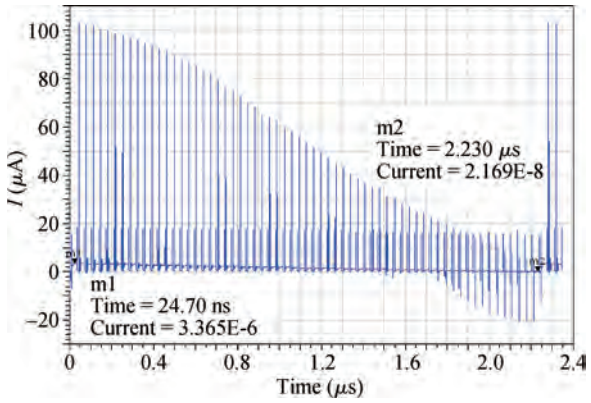

Fig. 10. The output current of N1_m.

2.5. The pixel circuit

As shown in Fig. 11, the pixel cell circuit consists of five PMOS[6]. P1 is the driving current source transistor; P2, P3 and P4 are minimum-sized switch transistors; and P5 clamps the drain voltage of P4, preventing it from being below ground too much. The width-to-length (W/L) ratio of P1 is 6 μm/0.35 μm. The value of the storage capacitor C_1 is 90 fF, and this is used to hold the pixel data between two frames.

The pixel circuit's current is from 21.69 nA to 3.365 μA (a result from Fig. 10) in the sample phase, but the OLED (15 $\times$ 15 μm^2) working current is from about 200 pA to 30 nA. So we can change one terminal voltage of C_1's voltage from VBL (in Fig. 11) in the sample phase to VBH (in Fig. 11) in the hold

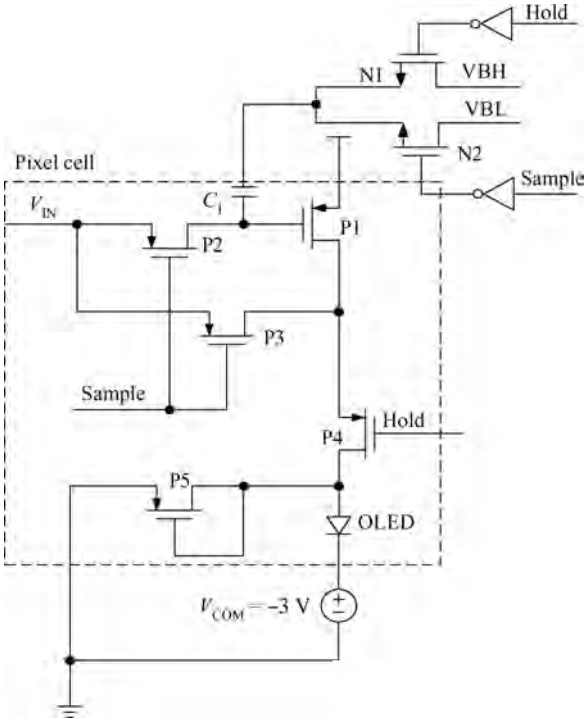

Fig. 11. The pixel circuit.

phase to realize the drain–source current of P1 being between 200 pA and 30 nA in the hold phase. The principle is as shown below.

(1) In the sample phase, P2, P3 and N2 are on, P4 and N1 are off, and one terminal voltage of C_1 is V_{BL} (Fig. 11). The P1 transistor is operating in the subthreshold region, so the current of P1 is:

$$I_{1P1} \cong I_0(W/L)_{P1} \exp[(V_{SG1} - |V_{th}|)/(nkT/q)], \quad (1)$$

where V_{th} is the threshold voltage of P1, and I_0 and n are empirical parameters, with $n \geqslant 1$, and typically ranging around 1.5.

(2) In the hold phase, P4 and N1 are on, P2, P3 and N2 are off, and one terminal voltage of C_1 is changed from V_{BL} to V_{BH}. So the gate voltage of P1 is changed from V_{SG1} (in the sample phase's voltage) to $V_{SG2} = V_{SG1} - (V_{BH} - V_{BL})$, and now the current of P1 is:

$$I_{2P1} \cong I_0(W/L)_{P1} \exp[(V_{SG2} - |V_{th}|)/(nkT/q)]. \quad (2)$$

Combine Eqs. (1) and (2), and we find that:

$$\frac{I_{1P1}}{I_{2P1}} = \exp\left[(V_{SG1} - V_{SG2})/(\eta kT/q)\right]. \quad (3)$$

If $I_{1P1}/I_{2P1} = 100$, Equation (3) is rewritten as:

$$V_{SG1} - V_{SG2} = nkT/q \cdot \ln(100). \quad (4)$$

In fact, we can write:

$$V_{BH} - V_{BL} = nkT/q \cdot \ln(100). \quad (5)$$

So as long as the value of V_{BH} and V_{BL} satisfies Eq. (5), we can change the drain–source current of P1 by 100 times.

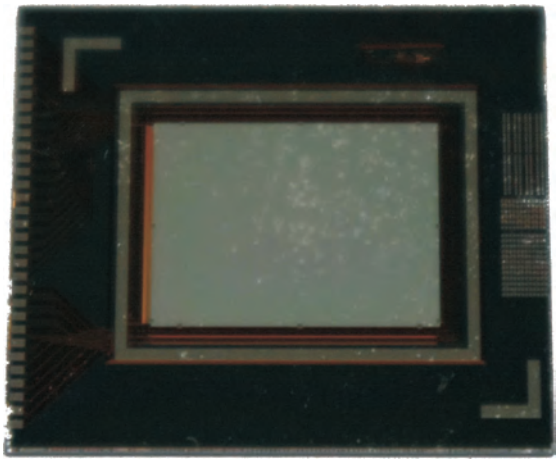

Fig. 12. A microdisplay die micrograph.

Table 1. Measurement summary.

Parameter	Value
Gray scales	64 (monochrome)
Pixel current	170 pA to 11.4 nA
Resolution	800 × 600
Pixel area	15 × 15 μm^2
Chip area	15.5 × 12.3 mm^2
Frame frequency	60 Hz
Technology	0.35 μm CMOS
Supply voltage	3.3 V
Consumption	85 mW

3. Measurement results

The system architecture described in this paper is implemented using the 0.35 μm two-poly four-metal (2P4M) 3.3 V mixed-signal CMOS process. A die scribed from a wafer is shown in Fig. 12. Then it will be with the PCB package, and an OLEDoS device has been grown on it (the thickness of the OLEDoS device is about 100 nm).

For the purpose of testing the OLEDoS display effect, three kinds of test signal are added to the chip. The first one is a black and white square pattern (Fig. 13(a)), the second is a 16 grayscale pattern (Fig. 13(b)) and the third is a 64 grayscale pattern (Fig. 13(c)). As shown in Fig. 13, OLEDoS has a good display effect and we can distinguish 64 gray scales. When the input of the 6 bit DAC was 00000 (darkest), the brightness was 24.3 cd/m^2; and when the input was 111111 (brightest), the brightness was 2108 cd/m^2. The brightness experimental results were measured by the Spectra Scan 650 device. According to the pixel cell area, it can be predicted that the pixel cell current ranged from 170 pA to 11.4 nA. The total power consumption of the chip was about 85 mW (black and white square pattern). Table 1 gives a measurement results overview of the overall chip.

4. Conclusion

In this paper, we proposed the system architecture of an OLEDoS driving circuit, which was implemented in a 0.35 μm 2P4M mixed-signal CMOS process. The output current of the 6 bit DAC was decreased by two steps: the first in a sample-

Fig. 13. Test patterns. (a) Black and white square pattern. (b) 16 gray scales pattern. (c) 64 gray scales pattern.

and-hold circuit, where the current was decreased by about 100 times; and the second in a pixel cell circuit in the hold phase, where the current was also decreased by about 100 times. The pixel cell working current was therefore modulated between hundreds of picoamperes and tens of nanoamperes. From the final display test result, it achieved a good display effect and realized 64 gray scales.

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