Analysis and implementation of derivative superposition for a power amplifier driver*

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Abstract: A new expression is proposed to analyze the linearization effectiveness of derivative superposition (DS) with large and small signal inputs, and different optimization methods of DS are found for different input magnitudes. A power amplifier driver (PAD) with large-signal optimized DS was implemented in 0.13 μm technology within a reconfigurable RF transmitter. The PAD is compatible with the GSM band at 900 MHz and the WCDMA band at 1.95 GHz, and it has a gain range of 44 dB with a step of 2 dB. Measurement results show that the overall OIP3 of the transmitter is better than 19 dBm, and the output referred 1-dB compression point is better than 7.5 dBm.

Key words: amplifier; linearity; derivative superposition

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1. Introduction

With the development of CMOS technology, system-on-chip (SoC) has become more and more popular. However, today it is still hard for an on-chip CMOS power amplifier (PA) to output large power with enough linearity to meet the stringent specifications of third-generation protocols such as WCDMA. Thus, power amplifier drivers (PADs) are still necessary for most RF transmitters as the output stage to drive off-chip PA.

In order to meet the strict requirement of protocols, linearity is the most important specification for a PAD. Many approaches have been proposed to improve the linearity of PADs (or PAs), including digital predistortion[1] and analog techniques[2]. Among those techniques, derivative superstition (also called the "multiple-gated transistor technique")[3] is a strong candidate because of its good linearization effect and power efficiency. In addition, the derivative superposition (DS) technique is also commonly used in low noise amplifiers (LNAs) with small signal inputs[4]. However, no detailed analysis of the comparison of DS with large and small signal inputs is available, and whether the optimization method of DS for large and small signals is different remains questionable.

In this work, we try to solve this question with our new uniform expression for non-linearity analysis. In addition, a PAD with derivative superposition linearization technique for reconfigurable RF application is proposed to verify our analysis. The PAD is programmable and compatible with GSM, EDGE and WCDMA.

2. Analysis of derivative superposition

2.1. Derivative superposition with small signal input

Derivative superposition, as shown in Fig. 1(a), was originally proposed to improve the small-signal linearity performance of amplifiers. MOSFET Ma is biased in the strong-inversion region, while Mb is biased in the subthreshold region. It defines the first, second and third order transconductance to be the first, second and third order derivative of the drain current regarding gate–source voltage:

$$g_{\mathrm{m1}}(V_{\mathrm{GS}}) = \left.\frac{\partial i_{\mathrm{DS}}}{\partial V_{\mathrm{GS}}}\right|_{V_{\mathrm{GS}}}, \quad g_{\mathrm{m2}}(V_{\mathrm{GS}}) = \left.\frac{\partial^2 i_{\mathrm{DS}}}{\partial V_{\mathrm{GS}}^2}\right|_{V_{\mathrm{GS}}},$$

$$g_{\mathrm{m3}}(V_{\mathrm{GS}}) = \left.\frac{\partial^3 i_{\mathrm{DS}}}{\partial V_{\mathrm{GS}}^3}\right|_{V_{\mathrm{GS}}}, \tag{1}$$

thus with input signal V_{in}, the Taylor series of total signal current i can be expressed as:

$$\begin{aligned} i &= g_{\mathrm{m1}}(V_{\mathrm{GS}})V_{\mathrm{in}} + \frac{1}{2}g_{\mathrm{m2}}(V_{\mathrm{GS}})V_{\mathrm{in}}^2 \\ &\quad + \frac{1}{2}\int_0^{V_{\mathrm{in}}} (V_{\mathrm{in}} - x)^2 g_{\mathrm{m3}}(x + V_{\mathrm{GS}})\,\mathrm{d}x \\ &= \left[g_{\mathrm{m1a}}(V_{\mathrm{GS}}) + g_{\mathrm{m1b}}(V_{\mathrm{GS}})\right] V_{\mathrm{in}} \\ &\quad + \frac{1}{2}\left[g_{\mathrm{m2a}}(V_{\mathrm{GS}}) + g_{\mathrm{m2b}}(V_{\mathrm{GS}})\right] V_{\mathrm{in}}^2 \\ &\quad + \frac{1}{2}\int_0^{V_{\mathrm{in}}} (V_{\mathrm{in}} - x)^2 \left[g_{\mathrm{m3a}}(x + V_{\mathrm{GS}})\right. \\ &\quad \left. + g_{\mathrm{m3b}}(x + V_{\mathrm{GS}})\right]\mathrm{d}x. \end{aligned} \tag{2}$$

Since an MOSFET has negative g_{m3} in a strong-inversion region and positive g_{m3} in a subthreshold region[4], the g_{m3} of Ma and Mb can cancel each other out (shown in Fig. 1(b)), making $g_{\mathrm{m3a}} + g_{\mathrm{m3b}}$ equal (or close) to zero within the compensation window. As a result, the last term in Eq. (2) is close to zero, thus the third-order nonlinearity is reduced. Consequently, the optimization goal of DS for small signals is to

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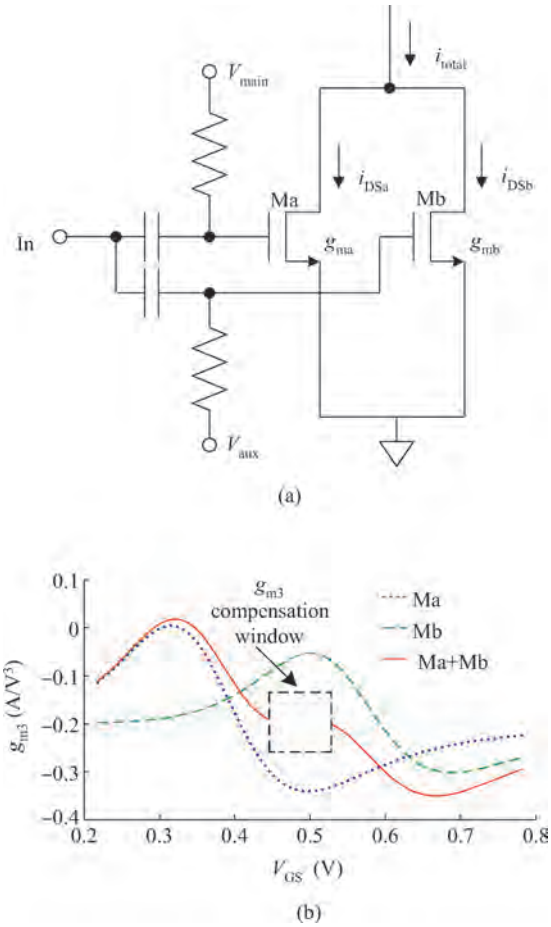

Fig. 1. (a) Concept of derivative superposition. (b) Third order transconductance.

obtain a compensation window with a range as large as possible to accommodate input signal swing. The range of the compensation window is usually around 100 mV, enough to handle a small signal input, but far from enough for a large signal input. On the other hand, g_{m3} outside the compensation window grows rapidly, making the third-order nonlinearity of DS with small signal optimization similar to an uncompensated one when the input signal is large. Thus, the optimization goal of small signal DS is not suitable for large inputs. In addition, the third-order term is expressed by an integral term in Eq. (2) so it is hard to quantitatively calculate third-order nonlinearity with Eq. (2).

2.2. Derivative superposition with large signal input

For a large signal, an analytical method was proposed in Ref. [5]. The circuit of an amplifier for large signal analysis of DS is shown in Fig. 2. The circuit is in a pseudo-differential configuration to reduce the impact of second-order nonlinearity. The main amplifying MOSFETs (M1 and M2) are biased in the strong-inversion region, while auxiliary amplifying MOSFETs (M1aux and M2aux) are biased in the subthreshold region. The first-order differential transconductance of the main, auxiliary and total amplifying MOSFETs are shown in Fig. 3(a). With complementary transconductance of main amplifying MOSFETs and auxiliary amplifying MOSFETs, the total transconductance of the main and auxiliary amplifying

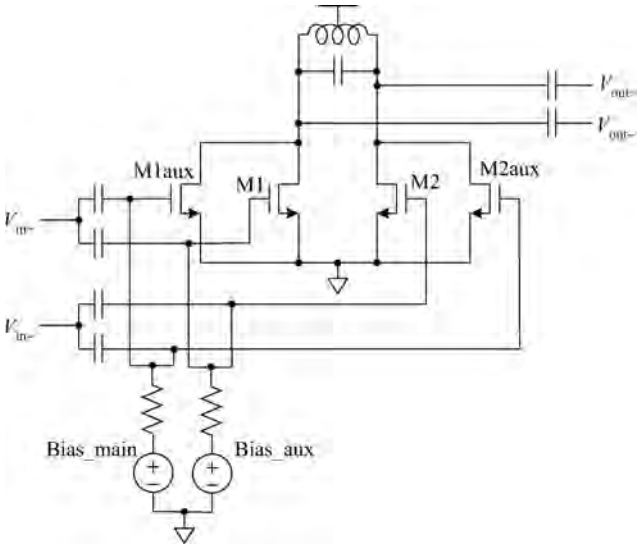

Fig. 2. Circuit of amplifier for large signal analysis of DS.

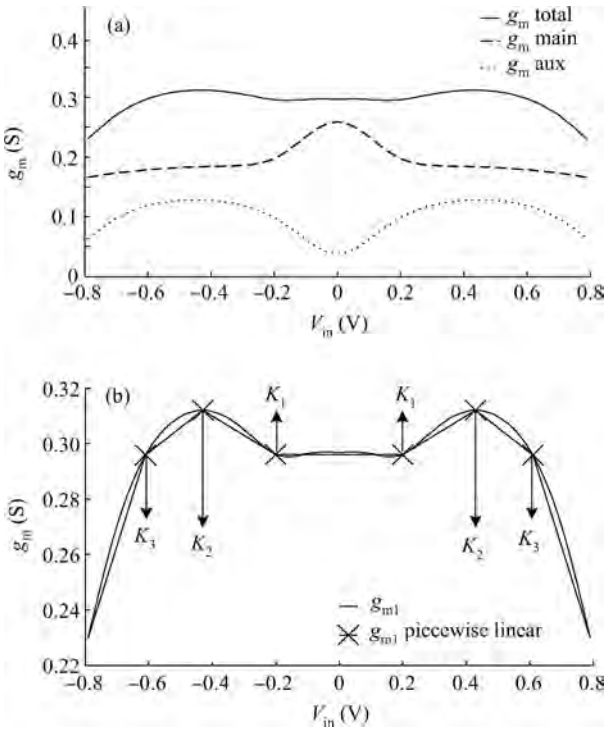

Fig. 3. (a) Differential transconductance of main, auxiliary and total amplifying MOSFETs. (b) Piecewise linear approximation of differential transconductance.

MOSFETs is flat over a large range. Next, we use piecewise-linear curve to approximate the total transconductance curve (Fig. 3(b)). Since g_{m3} is the second-order derivative of g_{m1}, g_{m3} is now approximated by the Dirac-delta pulses at the points where the slope of g_{m1} changes (kneels in Fig. 3(b)), and can be expressed as:

$$g_{m3} = \sum_{i=1}^{N} K_i \delta(V_{in} - V_i), \tag{3}$$

where V_{in} is the magnitude of input signal. To consider the third-order non-linearity of Eq. (3), we calculate its Fourier series. Suppose the input is a sinusoid with magnitude V_{in} at frequency ω, then the third-order component is[5]:

$$\begin{aligned} I_{\text{ds3,large signal}} &= \frac{\omega}{2\pi}\int_{-\pi}^{\pi}\int_{0}^{V_{\text{in}}\cos\omega t}\frac{1}{2}\left(V_{\text{in}}\cos\omega t - x\right)^2 \\ &\quad \times g_{\text{m3}}\left(V_{\text{GS}}+x\right)\cos 3\omega t\,\text{d}x\,\text{d}t \\ &= \frac{4}{15\pi}\text{Re}\left\{\sum_{i=1}^{N}\frac{K_i\left(V_{\text{in}}^2 - V_i^2\right)^{\frac{5}{2}}}{V_{\text{in}}^3}\right\}, \end{aligned} \tag{4}$$

where K_i is the magnitude of i-th Dirac pulse, which is the change of the slope of g_{m1} at the corresponding input signal magnitude, V_i. When the magnitude of input signal is smaller than V_i, $\text{Re}\{(V_{\text{in}}{}^2 - V_i{}^2)^{2.5}\}$ is zero, so the i-th Dirac pulse does not influence I_{ds3} until the input magnitude is larger than V_i.

2.3. Uniform analytical expression for large and small signal input

Equation (4) mainly describes the strong nonlinearity caused by kneels in transconductance, and is suitable for a large signal. When the input signal magnitude is smaller than all V_i, I_{ds3} predicted by Eq. (4) is zero, which is not consistent with real conditions. Actually, with a small signal input, I_{ds3} is mainly decided by g_{m3} at the bias point; when the input magnitude is moderate, which is the case of PAD, the third-order non-linearity is decided by the nonlinearity of both g_{m3} at bias point and transconductance kneels. To combine small signal conditions and large signal conditions into one expression, we can modify Eq. (4) by adding the contribution of small signal third-order transconductance. When the signal is very small, Equation (2) can be approximated as:

$$i \approx g_{\text{m1}}\left(V_{\text{GS}}\right)V_{\text{in}} + \frac{1}{2}g_{\text{m2}}\left(V_{\text{GS}}\right)V_{\text{in}}^2 + \frac{1}{6}g_{\text{m3}}\left(V_{\text{GS}}\right)V_{\text{in}}^3, \tag{5}$$

and its third-order component is (for simplicity, we write $g_{\text{m3}}(V_{\text{GS}})$ as g_{m3} here):

$$\begin{aligned} I_{\text{ds3,small signal}} &= \frac{\omega}{2\pi}\int_{-\pi}^{\pi}\frac{1}{6}g_{\text{m3}}V_{\text{in}}^3\cos^3\omega t\cos 3\omega t\,\text{d}t \\ &= \frac{g_{\text{m3}}V_{\text{in}}^3}{48}. \end{aligned} \tag{6}$$

However, the contribution of Eq. (6) should be small when the input signal is large (when $V_{\text{in}} > V_1$, where V_1 is the voltage position of the first Dirac-delta pulse K_1). In order to reflect this effect, we add a damping factor to Eq. (6), and it becomes:

$$I_{\text{ds3,small signal}} = \frac{g_{\text{m3}}}{48}\frac{V_{\text{in}}^3}{1+\left(\dfrac{V_{\text{in}}}{V_1}\right)^{\beta}}, \tag{7}$$

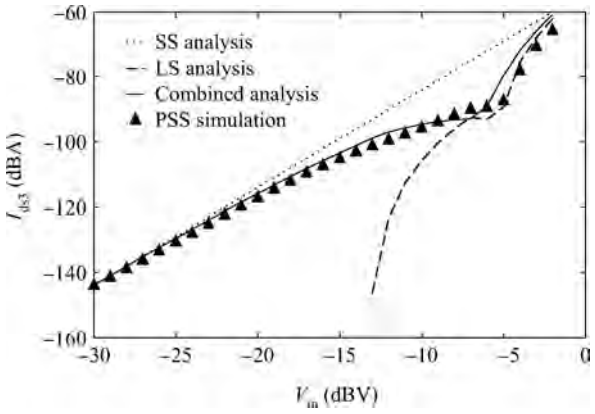

Fig. 4. Third-order component predicted by SS, LS, combined analysis and PSS simulation.

where β is a fitting factor and $\beta > 1$. Combining Eq. (4) and Eq. (7), we have:

$$\begin{aligned} I_{\text{ds3\_combined}} &= \frac{4}{15\pi}\text{Re}\left\{\sum_{i=1}^{N}\frac{K_i\left(V_{\text{in}}^2 - V_i^2\right)^{\frac{5}{2}}}{V_{\text{in}}^3}\right\} \\ &\quad + \frac{g_{\text{m3}}}{48}\frac{V_{\text{in}}^3}{1+\left(\dfrac{V_{\text{in}}}{V_1}\right)^{\beta}}, \end{aligned} \tag{8}$$

when the input signal is small, the first term in Eq. (8) is zero, and $V_{\text{in}}/V_1 \approx 0$, and Equation (8) becomes the case of Eq. (6). When the input signal is large, the contribution of the last term in Eq. (8) is damped by $[1+(V_{\text{in}}/V_1)^{\beta}]$, so Equation (8) is dominated by the first term. The results of small-signal (SS) analysis (Eq. (6)), large-signal (LS) analysis (Eq. (4)), combined analysis (Eq. (7)) and periodic steady-state (PSS) simulation are shown in Fig. 4. With a small input, the SS analysis and simulation results fit well; when the input signal is large, LS analysis has better consistency with the simulation. In addition, our combined analysis fits well with the simulation both in small and large signal conditions, which justifies the effectiveness of our analysis.

With Eq. (8), we can analysis nonlinearity in DS with both large and small input signals. One important inference of Eq. (8) is that a small ripple in g_{m1} curve will not degrade the third-order nonlinearity, since the rising edge and falling edge of the ripple correspond to Dirac-delta pulses with different signs and they can cancel each other out (K_1 and K_2 in Fig. 3(b)); in addition, the first edge of ripple can cancel the third-order nonlinearity caused by small signal transconductance g_{m3} as long as K_1 has the different sign with g_{m3} at bias point. Thus, the goal of optimization of DS for moderate and large signals is to achieve a large range of relatively flat (small ripple is acceptable) g_{m1} to accommodate input swing. Indeed, the third-order component here is directly related to third-order distortion (HD3) instead of third-order intermodulation (IM3), but with the empirical relationship between HD3 and IM3, IM3 can be inferred from HD3[5].

To verify the effectiveness of our analysis on IM3, we compare the linearity of amplifiers with large-signal optimized DS, with small-signal optimized DS and without DS. The g_{m1}

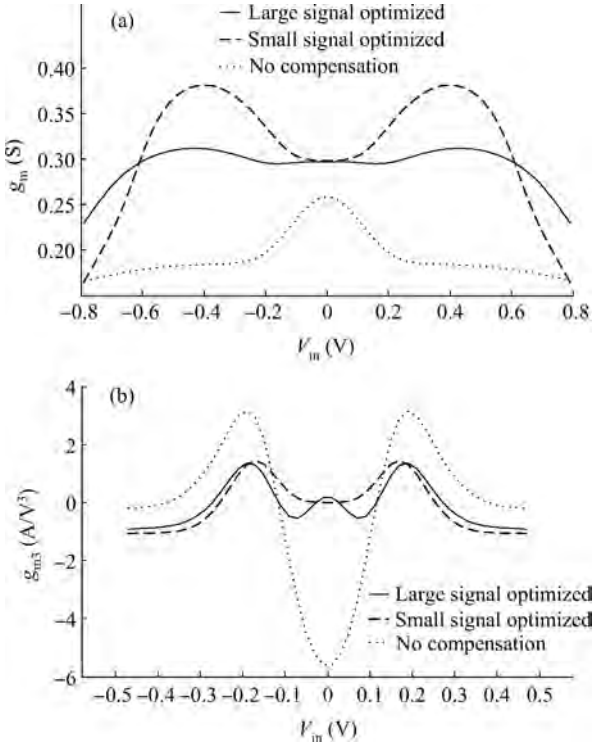

Fig. 5. (a) g_m and (b) g_{m3} of large signal optimized, small signal optimized DS and without DS.

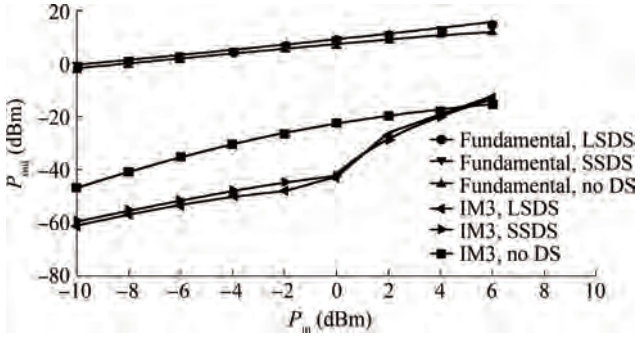

Fig. 6. Simulated IM3 of large signal optimized, small signal optimized DS and without DS.

and g_{m3} of three circuits are plotted in Figs. 5 (a) and 5(b). The small-signal optimized derivative superposition (SSDS) has the largest compensation window of g_{m3}, and the flat region of g_{m1} is small; outside the flat region, g_{m1} changes dramatically. On the other hand, the large-signal optimized derivative superposition (LSDS) has a large region of relatively flat g_{m1}, and there is a small ripple to cancel the small signal g_{m3}. We used PSS simulation to compare the IM3 of three amplifiers (shown in Fig. 6 below). With moderate input (–10 to –2 dBm) and output power (–1 to +7 dBm), the LSDS has the best IM3 (4 dB better than SSDS and 20 dB better than uncompensated one), this is because of the cancellation effect of the first ripple. After the first ripple ($\sim$ 0 dBm input), an auxiliary amplifying MOSFETs can enter into strong-inversion region and dominate the change of g_{m1}, causing the rapid rise of IM3 of both LSDS and SSDS, and finally the three amplifiers have similar IM3 with larger input (> 4 dBm input). The best compensation point

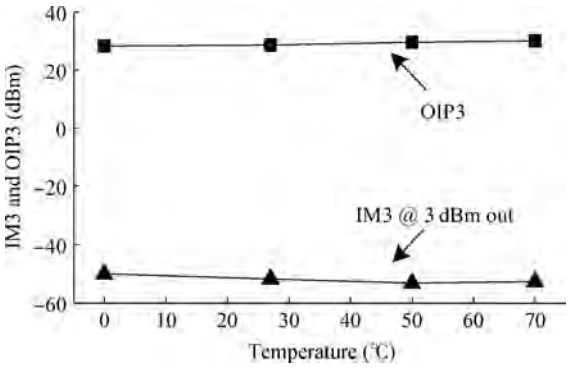

Fig. 7. Simulated IM3 and OIP3 change with temperature.

can vary when environment (PVT) changes; for example, when temperature changes, the threshold voltage of MOSFETs also change, making the compensation window shift. However, the effect of such shift on linearity is moderate; simulation shows that with different temperature, the IM3 with moderate output power (3 dBm) with the large-signal optimized DS varies between –50 and –53.22 dBm, while its OIP3 varies between 28.34 and 30.07 dBm, as shown in Fig. 7. From both analysis and simulation, we can conclude that DS can work effectively with moderate input, while the optimization goal of DS can be different when dealing with large or small signals.

3. Circuit design

The proposed PAD has a two-stage configuration. Since PAD delivers relatively large power, the size of power amplifying transistors, and thus parasitic capacitance is large. In order to reduce the loading effect of input capacitance on the previous stage (usually a mixer), a buffer stage is inserted as the first stage. As a building block in a reconfigurable RF transmitter, the PAD can work under two frequency bands (900 MHz for GSM/EDGE band and 1.95 GHz for WCDMA band) and cover a wide gain range of 44 dB.

3.1. First stage

The first stage of the PAD is shown in Fig. 8. Since the output swing of the first stage is relatively low, the power supply voltage of the first stage is 1.2 V. The first stage uses a pseudo-differential structure with an LC tank load. A switchable capacitor is inserted into the LC tank to tune the resonating frequency of the LC tank when the work band of PAD changes. In addition, a parallel resistor is added into the LC tank to decrease the Q factor of the LC tank and thus increase the 3-dB bandwidth of the PAD. In addition to working as buffer stage, the first stage also provides a large range of gain control and fine tuning step (32 dB gain range and 2 dB/step). The gain control is realized by switching on/off cascode transistors (s1–s16), and switching on different cascode transistors corresponds to different gain. One concern here is systematic gain accuracy. The gain step (2 dB, or $10^{0.1}$) is not a rational number, so we need to use a rational number to approximate it. All transistors in the first stage have the same channel length and finger width to increase matching. Suppose the effective number of fingers (the number of fingers of transistors whose corresponding cascode

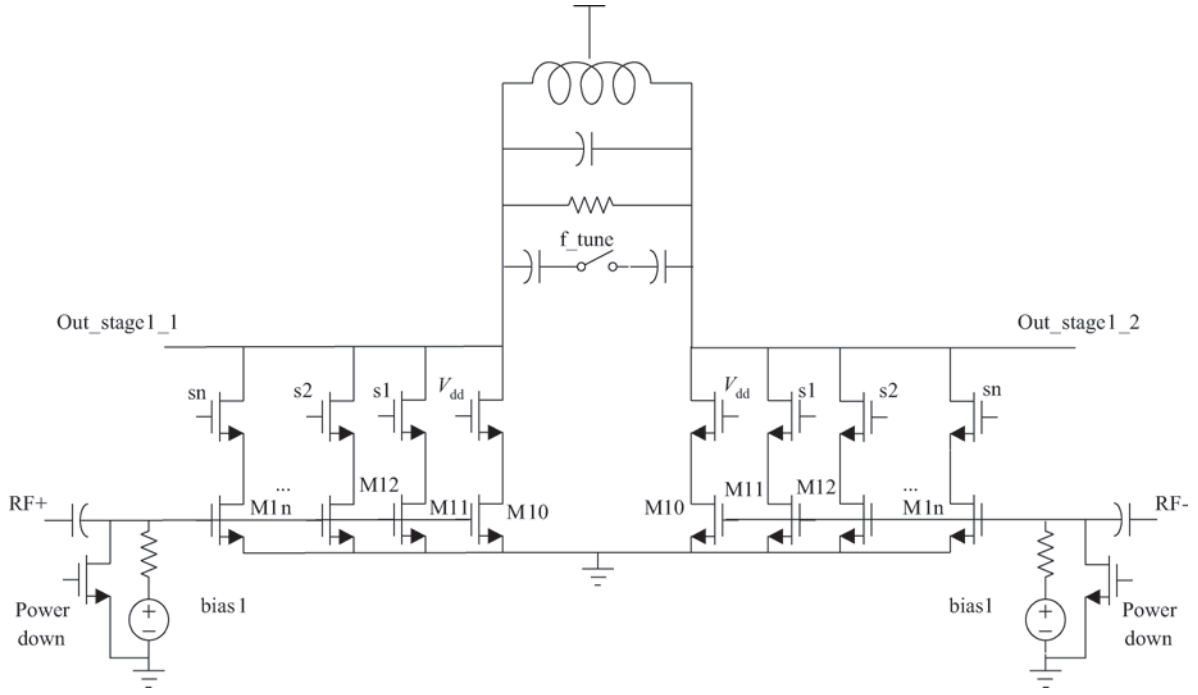

Fig. 8. Schematic of the first stage of the PAD.

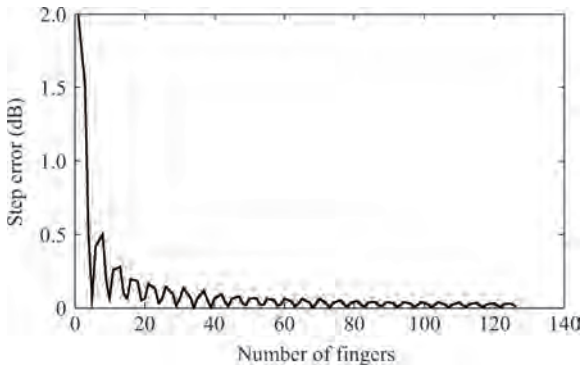

Fig. 9. Gain error versus number of fingers.

transistors are switched on) of one gain set is p, then we must find an integer q as the effective number of fingers for the next gain step which minimizes error ε, where

$$\varepsilon = \frac{q/p}{10^{0.1}}. \tag{9}$$

A direct observation is that with larger p, it is more likely to find a better q to reduce ε. The curve of step error versus p is shown in Fig. 9. From Fig. 9, we can see that the gain error generally decreases as effective number of fingers increases, though the curve is not monotonic. Thus, we can conclude that the largest systematic gain step error occurs at step with small gain set. To decrease step error, we should choose a large number of fingers, but this can increase parasitic capacitance. To obtain a balance between parasitic and step error, we choose the effective number of fingers of M10, which corresponds to the smallest gain, to be 6, and it can ensure that the systematic gain error of the first stage is smaller than 0.5 dB.

3.2. Second stage

The second stage is shown in Fig. 10. The power supply voltage of the second stage is 2.5 V for a large power output, and can be reduced to 1.8 V when outputting moderate power. In order to reduce the risk of breakdown, cascode transistors in the second stage are thick-oxide MOSFETs. The second stage uses the DS technique to improve the linearity. According the analysis in Section 2, our optimization goal is a flat g_{m1} curve in large input voltage region instead of a large g_{m3} compensation window. The gain of the second stage can vary by switching cascode transistors, and it has a gain range of 12 dB and a gain step of 6 dB. The sizes ratios of transistors M21 : M22 : M23 and M21aux : M22aux : M23aux are 1 : 1 : 2 to fulfill 6 dB gain step. Since the PAD needs to drive two off-chip PAs corresponding to different frequency bands, the second stage has two branches of cascode transistors to work as RF switches (controlled by GSM/WCDMA enable signal). When working with a selected frequency band and gain set, cascode transistors corresponding to the frequency band and gain set are turned on, while other cascode transistors are turned off. The load of the second stage is the LC tank. Two LC tanks, resonating around 900 MHz and 1.95 GHz, correspond to two frequency bands. The resonating impedance of the LC tanks is adjusted to near 50 Ω to facilitate output matching. The simulated output third-order interception point (OIP3) of the two-stage driver is 24.14 dBm for 1.95 GHz high-band and 22.91 dBm for 900 MHz low band. The difference between high-band and low-band OIP3 may be attributed to the different load of driver amplifier, when the LC tank resonates at different frequencies.

4. Implementation and measurement results

The PAD is implemented in SMIC 0.13 μm CMOS technology, as a part of a reconfigurable RF transmitter. The chip

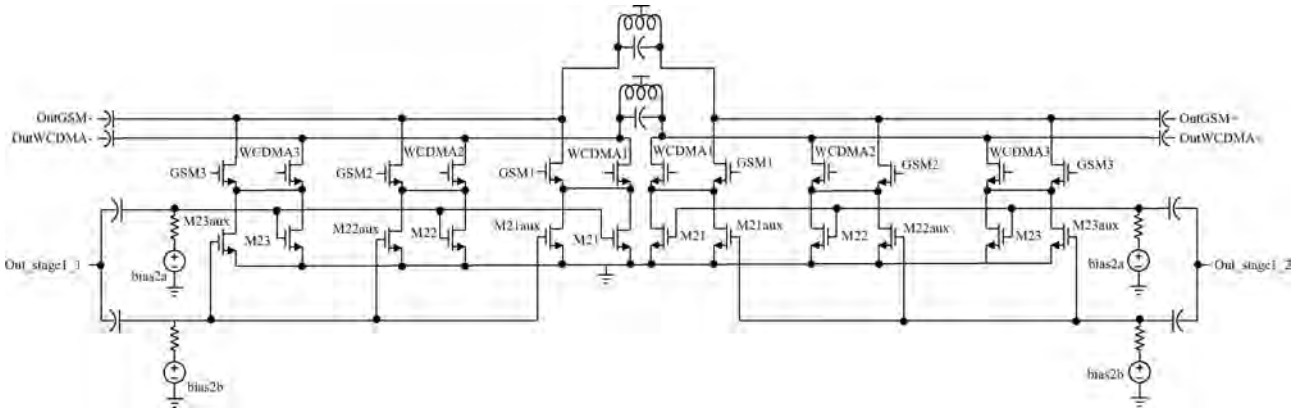

Fig. 10. Schematic of the second stage of PAD.

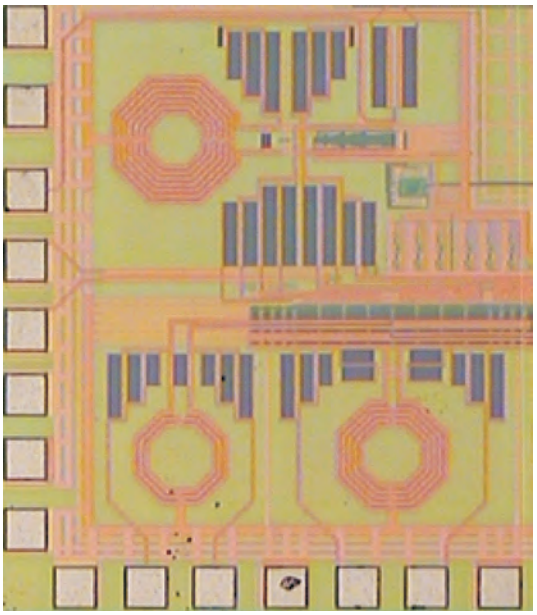

Fig. 11. Chip micrograph of the PAD.

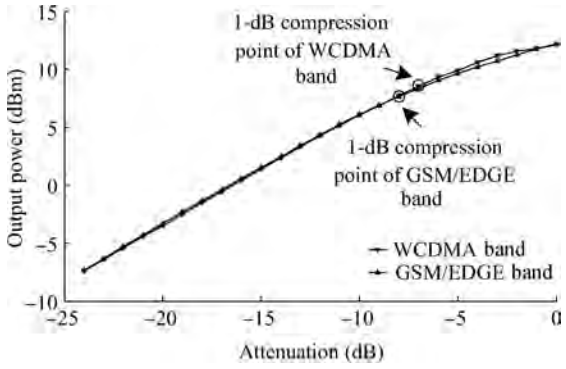

Fig. 12. Output power curve.

micrograph of the PAD is shown in Fig. 11. The area of the PAD is $860 \times 720\ \mu m^2$.

The PAD was tested inside the transmitter chain. The currents of the first stage and second stage are 12 and 42 mA, respectively. The exact gain of the PAD cannot be directly measured, and the simulated maximum gain is 15 dB. The curve

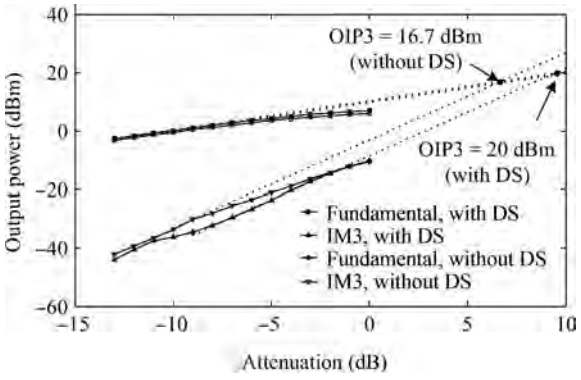

Fig. 13. IM3 curve at 1.95 GHz output.

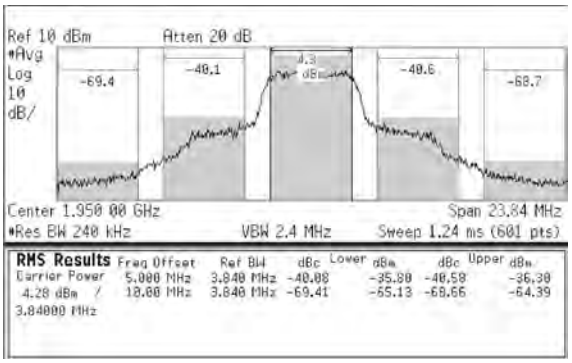

Fig. 14. ACLR measurement result of a WCDMA signal with 2.5 V power supply.

of output power versus input attenuation at maximum gain set is shown in Fig. 12. The output 1-dB compression points for WCDMA band and GSM/EDGE band are 8.3 and 7.5 dBm, respectively.

In order to investigate the effectiveness of DS for a large signal, a two-tone baseband signal with frequency spacing of 1 MHz is inputted ($f_1 = 1.95$ GHz and $f_2 = 1.951$ GHz), and output IM3 curve of PAD with DS enabled/disabled is shown in Fig. 13. The input signal magnitude is adjusted by the attenuator inside a vector signal generator. At the maximum gain set, the auxiliary amplifying MOSFETs consume 5 mA current. The gain of the PAD when DS is enabled is about 0.5 dB

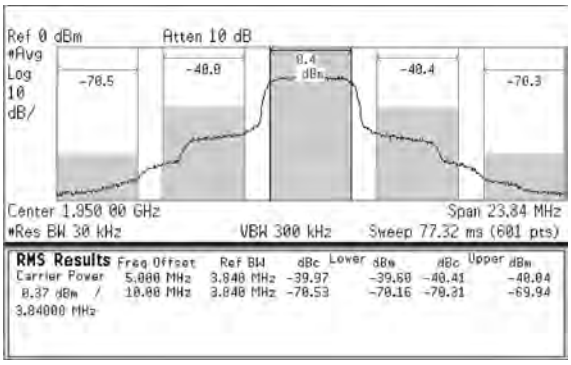

Fig. 15. ACLR measurement result of a WCDMA signal with 1.8 V power supply.

higher than when DS is disabled, since auxiliary amplifying MOSFETs also provide gain. The overall OIP3 of the transmitter with DS enabled at WCDMA band is 20 dBm, while OIP3 drops to 16.7 dBm when DS is disabled. At moderate output power (3 dBm), the IM3 of the transmitter with DS is 4 dB better than without DS. The overall OIP3 and improvement of OIP3 are less than in the simulation result, which can be explained by the fact that the simulation only considers the nonlinearity of the PAD while in measurement nonlinearities induced by other blocks in the transmitter, such as the mixer and the filter, can also contribute to the overall nonlinearity and degrade the improvement. For GSM/EDGE bands, the OIP3 curve is similar, and the measured OIP3 is 19.1 dBm with DS.

The adjacent channel leakage ratio (ACLR) of the PAD when working with a WCDMA input signal at maximum gain is shown in Fig. 14. With 4.3 dBm output power, the ACLRs at 5 MHz and 10 MHz frequency offset are −40.1 dBc and −68.7 dBc, respectively, leaving more than 5 dB margin for an off-chip PA. When outputting moderate power, the power supply voltage of the second stage can be reduced to 1.8 V to save power. An ACLR with a power supply voltage of the second stage equal to 1.8 V is shown in Fig. 15. The channel power is 0 dBm with 40 dBc and 70 dBc ACLR for 5 MHz and 10 MHz frequency offset. Actually, when the gain set is small, the power consumption of the PAD can be further reduced. For example, with 6 dB gain reduction, the power consumption of the second stage decreases by 50%. Thus, the power consumption of the PAD can be adaptively adjusted with different output powers and it can be more power-efficient than PADs without power control.

The error vector magnitudes (EVM) for 900 MHz GSM and EDGE at 5 dBm output power are shown in Figs. 16(a) and 16(b). For GSM, the phase error is less than one degree; for EDGE, the EVM is less than 2.3%. These results show that the PAD has negligible AM-PM distortion with moderate output power.

The S_{22} of the PAD at GSM/EDGE bands and WCDMA band is shown in Fig. 17. The simulated impedance of the LC tank of the second stage at resonating frequency is near 50 Ω, but with PVT variation and parasites on a test PCB board, the resonating frequency of the LC tank deviates from the expected value, which makes off-chip matching network necessary. With an off-chip matching network, the S_{22} at GSM, EDGE and WCDMA working band can be lower can –8 dB.

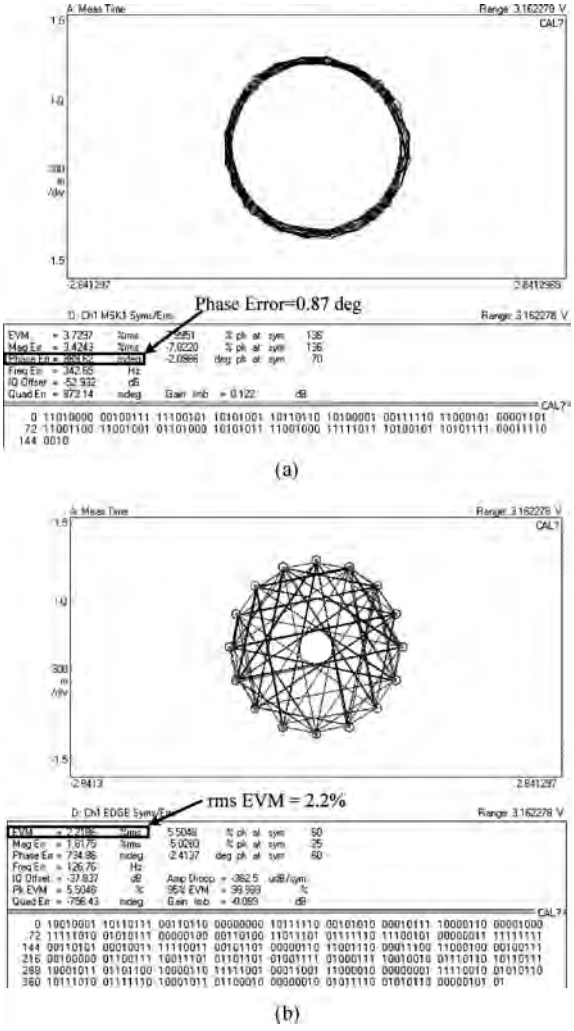

Fig. 16. EVM of (a) GSM and (b) EDGE output at 900 MHz.

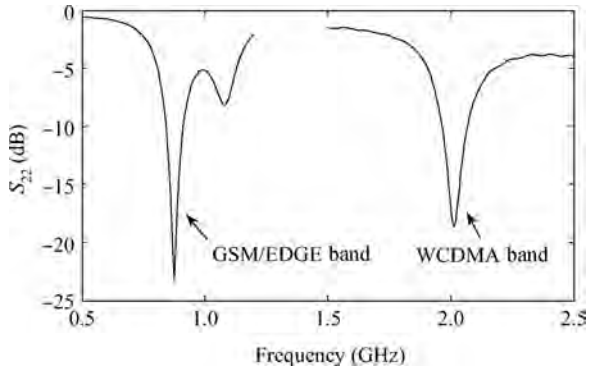

Fig. 17. S_{22} of PAD output.

The step-gain error of the PAD is shown in Fig. 18, and the gain error is less than 0.5 dB. The simulation results are slightly deviated from the measurement results at large gain because of the length of diffusion (LOD) effect, which is not considered in simulation. On the other hand, transistors corresponding to small gain have many dummy transistors surrounding them, which significantly reduce the impact of LOD effect on gain.

The performance of the PAD is summarized in Table 1. When compared with other multiple-band transmitters, the

Table 1. Summary of measured performance and comparisons.

Parameter	Ref. [6]				Ref. [7]		Ref. [8]	This work	
CMOS technology	0.18 μm				0.13 μm		0.18 μm	0.13 μm	
Supply voltage (V)	1.8				1.2		1.8	1.2 (1st stage), 2.5 (2nd stage)	
Current (mA)	50				51		N/A	16 (1st stage), 42 (2nd stage)	
Frequency (GHz)	0.9	1.8	2.4	5.2	2.45	4.9	0.05–0.862	0.9	1.95
P_{1dB} (dBm)	2.4	2.4	1.6	0.6	5.8	1	6.4	7.5	8.3
OIP3 (dBm)	13.5	12.2	12.1	8.3	15.5	12	15.9	19.1	20
PAE @ P_{1dB} (%)	1.73	1.73	1.6	1.28	N/A	N/A	N/A	4.35	5.23
Power gain (dB)	10	11	11.1	7.8	N/A		N/A	15* (max.)	
Gain range (dB)	N/A				43		N/A	44	
Gain step (dB)	N/A				2		N/A	2	
Sizes (mm^2)	0.307				N/A		N/A	0.619	

*: Simulation result.

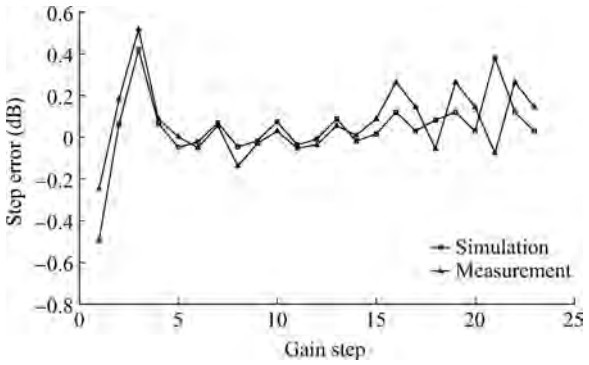

Fig. 18. Gain step error of PAD.

transmitter with the proposed PAD has the best OIP3, output 1-dB compression point and PAE, while the current consumption of our PAD are comparable to other PADs in references.

5. Conclusion

A uniform expression effective for both small and large signal conditions is proposed for non-linear behavior analysis. With the expression, we analyze and compare the derivative superposition with small and large signal inputs. Through analysis, we find that the optimization goals of derivative superposition are different for large signal input and small signal input: one is to compensate g_{m1}, and the other is to compensate g_{m3}. A PAD with large-signal optimized derivative superposition was implemented, and experimental results show that that the large-signal optimized derivative superposition can improve the overall OIP3 of transmitter by over 3 dB, and IM3 by over 4 dB at moderate output power.

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