Holding-voltage drift of a silicon-controlled rectifier with different film thicknesses in silicon-on-insulator technology*

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Abstract: This paper presents a new phenomenon, where the holding-voltage of a silicon-controlled rectifier acts as an electrostatic-discharge protection drift in diverse film thicknesses in silicon-on-insulator (SOI) technology. The phenomenon was demonstrated through fabricated chips in 0.18 μm SOI technology. The drift of the holding voltage was then simulated, and its mechanism is discussed comprehensively through ISE TCAD simulations.

Key words: holding-voltage drift; electrostatic discharge; silicon-on-insulator; silicon-controlled rectifier

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1. Introduction

The continuing scale of high-density and high-performance technology in advanced microelectronic processes, short channel effects, hot electrons, and so on, provides many challenges for device engineers. In comparison to bulk-Si, silicon-on-insulator (SOI) has excellent speed and power consumption features[1]. However, electrostatic-discharge (ESD) is a major challenge for advanced SOI technology due to the inherent properties of SOI devices. This is due to film current conduction properties and potential heat trapping in the film on top of the oxide, which is a poor heat conductor. The SOI buried oxide (BOX) and thin silicon film regions are perceived as impediments to providing good ESD protection for SOI chips. Since SOI is expected to be a key technology in future deep-submicron IC's, ESD protection will be a major issue in the manufacture of SOI devices[2, 3].

This work presents a new phenomenon, that of the holding-voltage drift of a silicon-controlled rectifier (SCR) in different film thicknesses in SOI technology. An SCR formed by lateral PNPN structures could prevent device damage from ESD. The experimental results in 0.18 μm SOI technology measured through the transmission line pulse test system demonstrated the holding-voltage drift in different film thicknesses. To investigate the mechanism, ISE TCAD simulations were used, followed by comprehensive discussions.

Due to the thin silicon film and thermal insulating properties of the buried oxide, ESD devices in SOI have significantly low performance. SCRs have been widely used in industry for on-chip ESD protection due to their excellent current shunting capabilities[4], and have become one of the most efficient structures in terms of ESD protection. Figure 1 shows a cross-section of an SCR formed by lateral PNPN structures in SOI technology. On the buried oxide BOX, a parasitic PNPN structure was formed in silicon. The adjacent N+ and P+ contacts in the N-well were connected to the anode terminal. A vertical PNP bipolar transistor, Q1, was formed with the P-substrate as the collector, the N-well as the base and the P+ contact as the emitter. The N+ contact in the P-substrate was connected to the ground and formed the emitter of the lateral NPN bipolar transistor Q2. The base of the NPN was formed by the P-substrate and the collector was the N-well and the N+ contact. There were shunt resistors, R_1 and R_2, between the anode/cathode and the Q1/Q2 base. R_{s1} and R_{s2} were the parasitic resistors in the N-well and the P-substrate, respectively.

The experimental results in the 0.18 μm SOI technology are summarized in Table 1, where the holding-voltage drift, V_{hold}, is apparent between the thinner and thicker SCR film thicknesses. L is the lateral space, as shown in Fig. 1. In the same L, the V_{hold} of the thinner film SCR increased impressively compared with the thicker one. For instance, there was remarkable drift (approximately 0.29 V) in the holding voltage when the film thickness varied in the L_2 device.

As we know, the holding-voltage directly decides the latch up immunity capability of ESD protection devices. To prevent from latch up, the holding voltage of ESD protections should exceed the operation voltage of the protected device. Thus the new phenomenon that holding-voltage of SCR that is drifted with diverse thickness of the films in SOI process should be taken into consideration by ESD protection designers. Therefore, simulations aiming to verify the new phenomenon and comprehensive discussions were processed through ISE TCAD in the next section.

2. Simulations and discussions

The holding-voltage drift phenomenon was also apparent in the simulated results, as shown in Fig. 2. The aforementioned

Table 1. Experimental results in the 0.18 μm SOI technology.

L	V_{hold} (V) (Thinner film)	V_{hold} (V) (Thicker film)
L_1 (Shortest)	1.14	0.97
L_2 (Middle)	1.33	1.04
L_3 (Longest)	1.58	1.1

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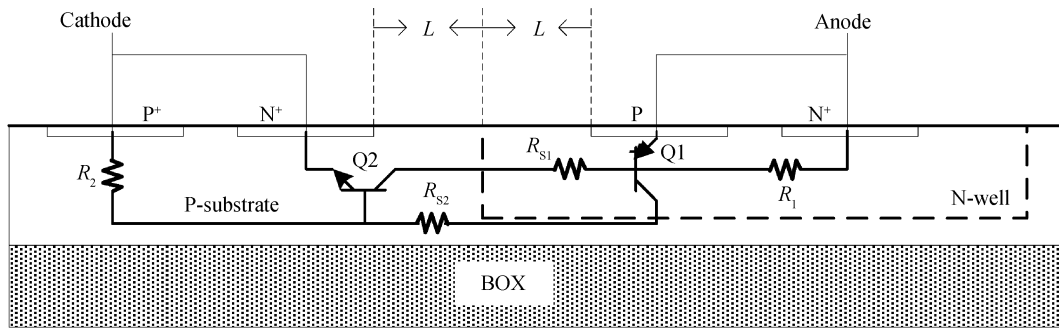

Fig. 1. An SCR formed by lateral PNPN structures in SOI technology.

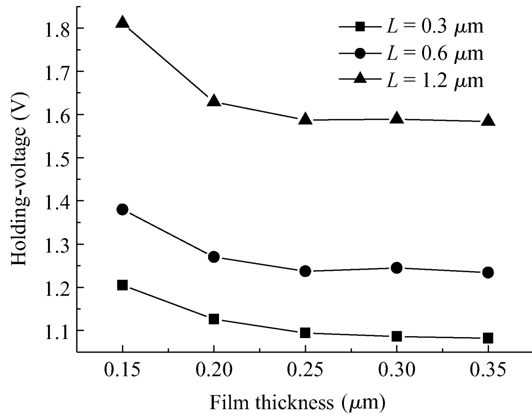

Fig. 2. Holding-voltage drift phenomenon in simulated results.

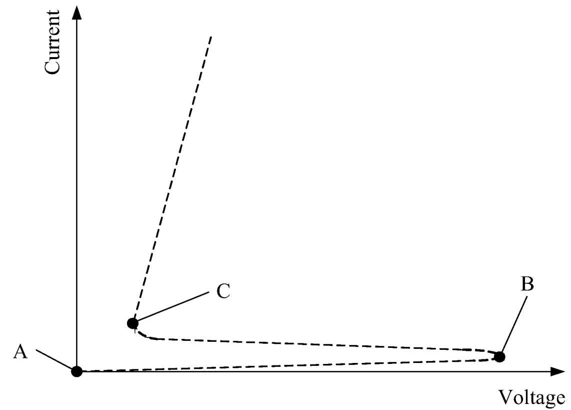

Fig. 4. I–V characteristics of the SCR with deep snapback.

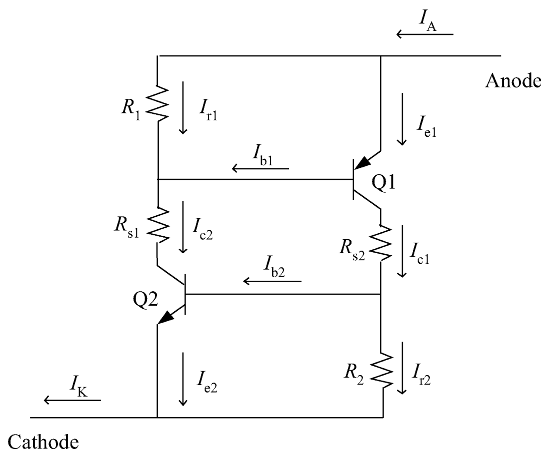

Fig. 3. Equivalent circuit of the SCR.

parasitic PNPN structure formed a parasitic SCR with different values of L, including 0.3, 0.6 and 1.2 μm. The film thickness varied from 0.15 to 0.35 μm. In the condition where L $=$ 0.3 μm, the holding-voltage dropped from 1.205 to 1.086 V when the film thickness varied from 0.15 to 0.35 μm. Similarly, the $V_{\rm hold}$ reduced from 1.380 to 1.244 V in the L $=$ 0.6 μm device. With $L = 1.2$ μm, the holding-voltage dropped from 1.811 to 1.618 V. In order to discuss the holding-voltage drift with diverse film thicknesses in SOI technology, the operation principle of SCRs is presented in the next section.

Figure 3 shows the equivalent circuit of the SCR, where the parasitic SCR consists of a pair of parasitic lateral bipolar transistors, PNP Q1, and vertical NPN bipolar transistors, Q2. R_1 and R_2 are the N-well and substrate shunt resistors, respectively. Between the base and the collector of Q1 and Q2 were parasitic resistors defined as $R_{\rm s1}$ and $R_{\rm s2}$, respectively. During an ESD stressed over anode and with the SCR turned on, a low impedance feature, which dramatically reduced the power dissipation, emerged[5]. Because of regenerative feedback and low impedance during the operation of Q1 and Q2, this had deep snapback I–V characteristics, which enabled it to handle large transient currents.

Figure 4 displays the SCR's I–V characteristics with deep snapback. Point A depicts the initial state of the parasitic SCR, where no voltage stress is applied.

At point B, the SCR was triggered and turned on. To get the appropriate triggering voltage that the various applications need, the SCR triggering technique has made great progress in recent years with, for example, integrated GGMOS (gate-grounded MOS) triggering, integrated GCMOS (gate-coupled MOS) triggering and substrate triggering[6, 7]. For the basic lateral PNPN structure mentioned above, the triggering voltage was given by SCR forward breakdown, almost the breakdown voltage of the P-substrate/N-well junction. The impact ionization that the high electric field induced was concentrated around the P-substrate/N-well junction. Once the applied voltage increased over the breakdown voltage, avalanche breakdown took place and avalanche breakdown current turned the device on.

While the SOI SCR operated, the lateral PNPN structure could be equivalent as a cross-coupled PNP and NPN bipo-

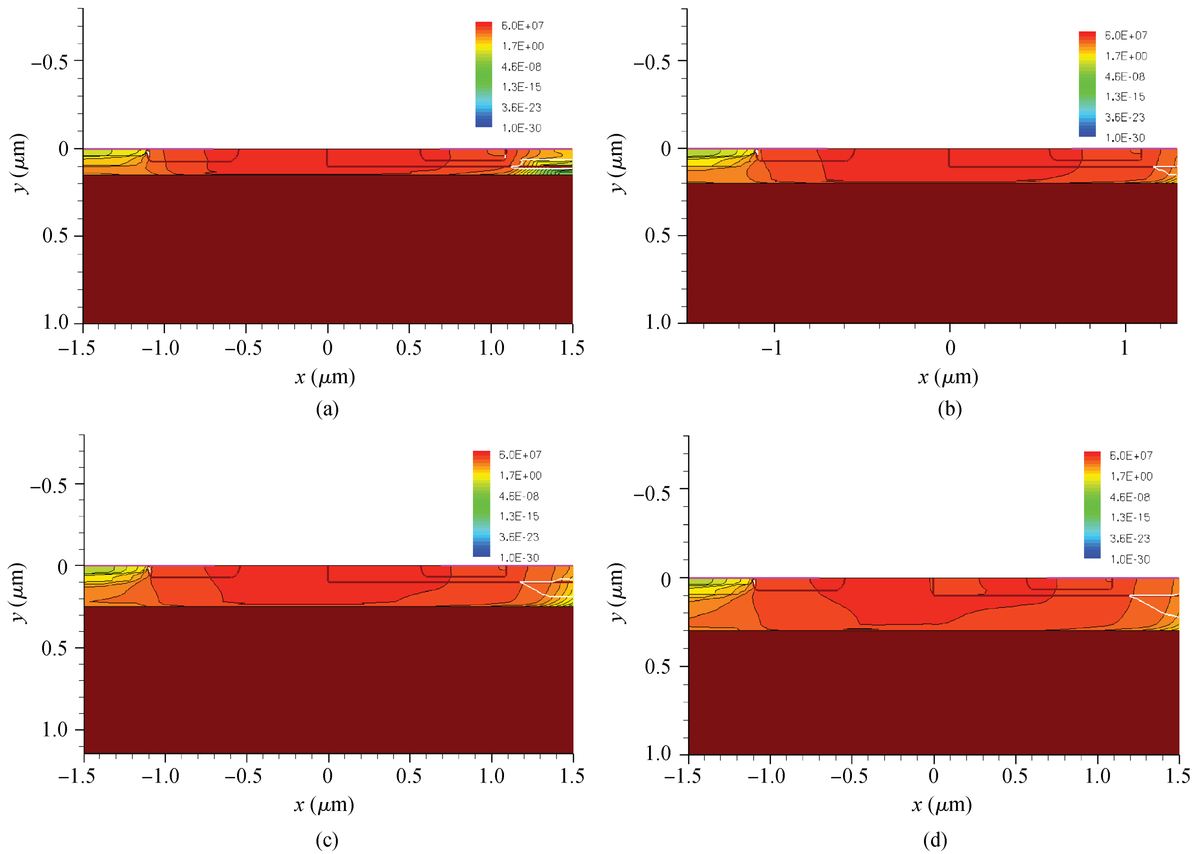

Fig. 5. Current density distribution in SOI SCR devices with film thicknesses of (a) 0.15, (b) 0.2, (c) 0.25 and (d) 0.3 μm, respectively.

lar transistor. At point C, this PNP–NPN coupling established regenerative feedback, leading to the I–V characteristic with snapback phenomenon and causing electrical instability. To analyze the critical condition of SCR operation, the Ebers-Moll transistor model and Kirchhoff's current law were used to get:

$$I = I_{\mathrm{A}} = I_{\mathrm{K}} = I_{\mathrm{e1}} + I_{\mathrm{r1}} = I_{\mathrm{e2}} + I_{\mathrm{r2}} = I_{\mathrm{c1}} + I_{\mathrm{c2}}, \quad (1)$$

$$I_{\mathrm{c1}} = \alpha_1 I_{\mathrm{e1}} + I_{\mathrm{co1}}, \quad (2)$$

$$I_{\mathrm{c2}} = \alpha_2 I_{\mathrm{e2}} + I_{\mathrm{co2}}, \quad (3)$$

$$I = \alpha_1 I_{\mathrm{e1}} + I_{\mathrm{co1}} + \alpha_2 I_{\mathrm{e2}} + I_{\mathrm{co2}}. \quad (4)$$

Hence, one gets

$$I = \frac{I_{\mathrm{co1}} + I_{\mathrm{co2}} - \alpha_1 I_{\mathrm{r1}} - \alpha_2 I_{\mathrm{r2}}}{1 - \alpha_1 - \alpha_2}, \quad (5)$$

where α_1 and α_2 are the transport factors of the PNP and NPN bipolar transistors, respectively, and I_{co1} and I_{co2} are the reverse leakage currents of the PNP and NPN bipolar transistors, respectively. I_{e1}, I_{c1}, I_{e2}, I_{c2}, I_{r1} and I_{r2} are illustrated in Fig. 3. We assume that the leakage current was significantly less than the anode or cathode current, $\frac{I_{\mathrm{co1}}+I_{\mathrm{co2}}}{I} \approx 0$. Based on the formulas above, the critical regeneration condition for the parasitic lateral SCR can be expressed as:

$$\alpha_1 + \alpha_2 = 1 + \alpha_1 \frac{I_{\mathrm{r1}}}{I} + \alpha_2 \frac{I_{\mathrm{r2}}}{I}. \quad (6)$$

At point C, both the parasitic PNP and NPN bipolar transistors operated and the potential difference between anode to cathode clamped to holding-voltage. The holding-voltage, V_{hold}, was the voltage across the PNPN structure after the structure switched from its blocking condition to its operating state. At this moment, the current through the Q1 flowed into the P-substrate and forward-biased the emitter–base junction of the Q2 NPN parasitic transistor. The voltage at the anode was no longer needed to provide bias for Q1, and decreased. The value of V_{hold} was determined by the amount of current that was needed to forward-bias the Q1 and Q2. As an approximation, V_{hold} was equal to the sum of the voltage drops across the forward active transistors, Q1, Q2, the parasitic resistors in N-well and the P-substrate[8].

$$V_{\mathrm{hold}} = V_{\mathrm{ec1}} + V_{\mathrm{be2}}\left(1 + \frac{R_{\mathrm{s2}}}{R_2}\right) = V_{\mathrm{eb1}}\left(1 + \frac{R_{\mathrm{s1}}}{R_1}\right) + V_{\mathrm{ce2}}, \quad (7)$$

where V_{ce1} and V_{be2} are the collector–emitter voltage drops of Q1 and the base–emitter, respectively. According to

$$\alpha_1 = \frac{\beta_1}{\beta_1 + 1}, \quad (8)$$

$$\alpha_2 = \frac{\beta_2}{\beta_2 + 1}. \quad (9)$$

During device operation, substituting the bipolar transistor current gain β term for Eq. (6), one gets:

$$\beta_1 \beta_2 = 1 + \frac{I_{\mathrm{r1}}}{I}\beta_1(\beta_2 + 1) + \frac{I_{\mathrm{r2}}}{I}\beta_2(\beta_1 + 1) > 1. \quad (10)$$

Conceptually, the coupling of the PNP and NPN bipolar formed a positive feedback circuit, whose feedback factor was greater than 1[9]. Hence in device operation both of the bipolar transistors, Q1 and Q2, turned on completely and worked in saturation state. Hence in Eq. (7), V_{ec1} and V_{ce2} are approximate to 0.3 V. Besides, $V_{be2} = V_{eb1} = 0.7$ V. Apparently, the parasitic resistances R_{s1} or R_{s2} played a significant role in the PNPN holding-voltage V_{hold}.

Consequently, understanding the holding-voltage drifts in different film thicknesses becomes conceivable. Figure 5 displays the current density distribution in the SOI SCR device which worked at point C in Fig. 4. When the film thickness dropped from 0.3 to 0.15 μm, the current that flowed in the N-well and P-substrate was compressed significantly. For the parasitic resistance R_{s2},

$$R_{s2} = \frac{l}{\delta_{si} A}, \tag{11}$$

where δ_{si} is the conductivity of the P-substrate that approximated to be a constant, and l and A are the length and cross-sectional area of the current channel, respectively. The narrowing of the current channel was equivalent to the reduction of parasitic resistance R_{s2}. Considering Eq. (7) and according to the experimental and simulated results, the holding-voltage would drift while the SOI film thickness became thinner to induce narrowing of current channel. Furthermore, theoretically, continuous increase of the film thickness could not reduce the holding-voltage continuously when the current channel was wide enough, as the 0.3 μm devices above indicate in simulated results.

3. Conclusion

In designing SCR-type ESD protection structures, the device is susceptible to latch-up danger during normal circuit operation. Such potential latch-up risk often leads to IC function failure or even destruction. In this paper a new phenomenon, that the holding-voltage of an SCR in SOI technology would drift in different film thicknesses, has been presented through both experimental and simulated results. With TCAD simulations and discussion, a drift mechanism was eventually suggested. It was found that the narrowing of the current channel is the material cause of holding-voltage drift with diverse films. Considering and understanding holding-voltage drift is certainly beneficial in achieving latch-up immunity in SCRs designed in SOI technology.

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