An optimized analog to digital converter for WLAN analog front end*

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Abstract: A 10 bit 80 MSPS analog to digital converter optimized for WLAN analog front end is presented. In contrast to conventional 1.5 bit pipeline architecture, four optimized multi-bit multiply digital to analog converter stages are implemented. An on-chip low-noise reference buffer is proposed for SoC integration purposes, and a wide-bandwidth wide swing sample and hold amplifier is also presented for achieving a good dynamic range. The converter was fabricated in 0.18 μm 1P6M CMOS technology, and the core area occupies approximately 0.85 mm^2. Measured results show that with an 11 MHz input signal, it provides a 9.4 bit effective number of bits and a 72 dBc spurious frequency dynamic range when sampled at 80 MHz.

Key words: WLAN; analog to digital converter; multi-bit MDAC; reference buffer; SHA

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1. Introduction

The rapid growth of wideband wireless LAN towards higher data rates and greater system capacity places higher requirements on the base-band analog front end components, such as analog to digital converters[1, 2]. For example, the 802.11a protocol supports multiple 20 MHz channels, so for this application the base-band IQ ADCs must sample at least 40 MHz. The oversampling relative to signal bandwidth simplifies the design of the anti-aliasing filter and allows the filtering of adjacent channel blockers to be done primarily in the digital domain[1]. From the system perspective, the SNR of ADCs needs to be above a certain level so as not to deteriorate the EVM of the whole system. A 10 bit 80 MSPS ADC therefore has the full potential to satisfy all the requirements for wideband wireless LAN applications. Integration of the base-band analog front end, and even the radio-frequency front end with the digital base-band to provide a complete solution for WLAN applications, is another current trend for its cost advantages and system implementation flexibility[1−4]. This drives the design of ADCs into deep sub-micro nodes, where corresponding issues such as reduced supply voltage and lower intrinsic gain of the transistor need to be addressed. Traditionally, the pipeline ADC has been the most appropriate realization choice in wireless communication, because of its good trade-off between power, speed and area. Many power saving techniques can also be included in pipeline ADCs, such as amplifier time sharing and dynamic bias[5−8]. However, in more advanced processes, SAR and the sigma delta modulator have been embedded in the pipeline[9,10] ADC or even completely implemented[1] for wireless applications.

This paper describes a switched capacitor pipeline architecture that is compatible with low voltage in 0.18 μm technology. With the consideration of power and speed trade-off, a 2.5 bit per stage MADC is adopted. SHA is necessary for a good dynamic range and on-chip reference generation, and the distribution networks are also included for integration purposes.

2. Architecture and circuit implementation

2.1. Architecture

Traditionally, 1.5 bit stages have been seen to be power efficient for pipeline ADC design for sampling frequencies of several megahertz. Actually, for each extra bit increase in MDAC stages, the sample capacitors of the later stage can be reduced more dramatically. For analysis, the input referred noise due to second stage MDAC sample switches is given by

$$\sigma_{\mathrm{s2\_i}} = \sqrt{\frac{KT}{C_{\mathrm{L}}}}/G, \tag{1}$$

where G and C_{L} are the gain and capacitive loading of the first stage. C_{L} comprises the total sample capacitances of the second stage, the parasitic capacitances and the serial connected feedback and sample capacitance of the first stage. For each extra bit quantized in the first stage, gain G increases by a factor of two. Assuming C_{L} is dominated by the sample capacitance of the second stage, for the same noise budget, C_{L} can be reduced quadruply.

$$\mathrm{BW} = \beta\frac{g_{\mathrm{m}}}{C_{\mathrm{L}}} \approx \frac{1}{G}\frac{g_{\mathrm{m}}}{C_{\mathrm{L}}}. \tag{2}$$

From the above expression, the effective transconductance (g_{m}) can be reduced by two without deteriorating the bandwidth (BW) of the OTA. This leads to the fact that power savings can be achieved until the capacitance of the sub-ADC and interconnect become the dominant load, although the feedback factor of the corresponding stage decreases[11, 12].

On the other hand, in deep sub-micro technology, a two stage amplifier is often the only choice for the conflicting requirement of high gain and wide swing in deep sub-micro processes. In this situation, the bias current of the second stage takes the large portion of the whole amplifier current consumption[13]. Therefore, multi-bit stages probably achieve a higher power saving for the relaxed phase margin requirement and reduced number of amplifiers[15]. Figure 1 shows the architec-

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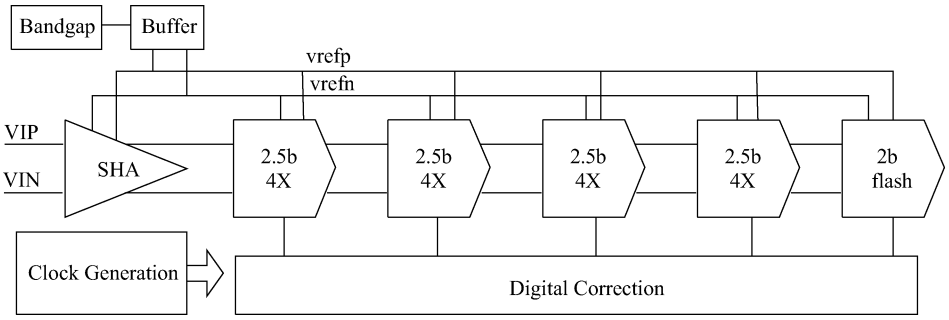

Fig. 1. The proposed pipeline ADC architecture.

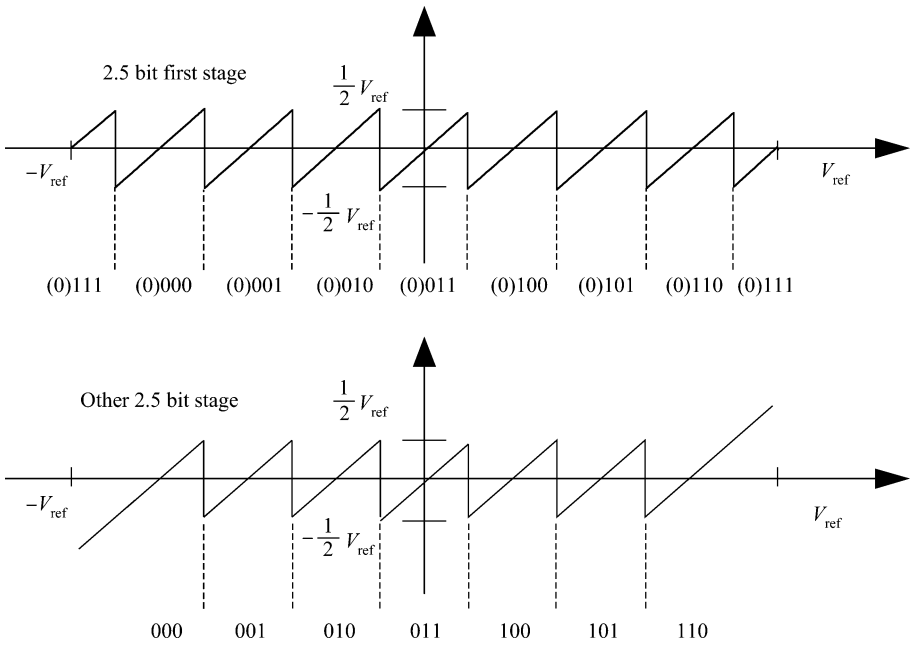

Fig. 2. Residue transfer functions of the first and other 2.5 bit stages.

ture of the proposed converter. The ADC core consists of four 2.5 bit MDAC stages followed by one 2 bit flash stage. Interstage scaling is used to save power. SHA is also included for a good dynamic range, and a reference generator for the purpose of SoC integration.

The transfer functions for the first and following stages are shown in Fig. 2, where digital outputs sent to the error correction block are also present. The difference between the two kinds of residue transfer functions is that two extra comparators are added in order to reduce residue output when the input signal approaches the signal boundary, therefore relaxing the swing requirement of the amplifier[14]. Also an extra bit is generated to signal the over range case.

2.2. Circuit implementation

2.2.1. SHA

Flip-around SHA is chosen primarily for its power and speed efficiency compared with charge-transfer SHA[12]. In order to accommodate certain common-mode voltage variations in input signal, a folded cascoded first stage amplifier is provided. PMOS input differential Mp1 and Mp2 is biased at a lower voltage when sampling the input signal, therefore small NMOS switches can be used for a smaller charge injection. Simple differential pair second stage Mn1 and Mn2 provide wide signal swing at the output, and an appropriate value of the Miller compensation capacitor C_c satisfies the stability requirements. Common mode feedback loops are applied to both the first and second stage output based on the switched capacitor principle. For good PVT variation, the common-mode reference voltage of the first and second stage output is $V_{gs\_mn1} + V_{dsat\_mn3}$ and $V_{dd}/2 + 0.1$ V, respectively. Biasing circuits also track the process variation automatically to minimize the sensitivity to the environment. Figure 3 shows the amplifier used in the design. The open-loop gain is larger than 70 dB over an output range of 2 Vpp from the simulation results.

2.2.2. MDAC

In the design, the architecture of the first 2.5 bit MDAC stage is shown in Fig. 4. During sampling phase Φ_s, sub-ADC and bottom plate of eight sample capacitors sample input signal, while two feedback capacitors and top plate of sample capacitors sample ground voltage. During amplification phase Φ_h, the feedback capacitors are connected between the input and output port of the amplifier, and the bottom plate of the sample capacitor is connected to the top reference V_{refp} or bot-

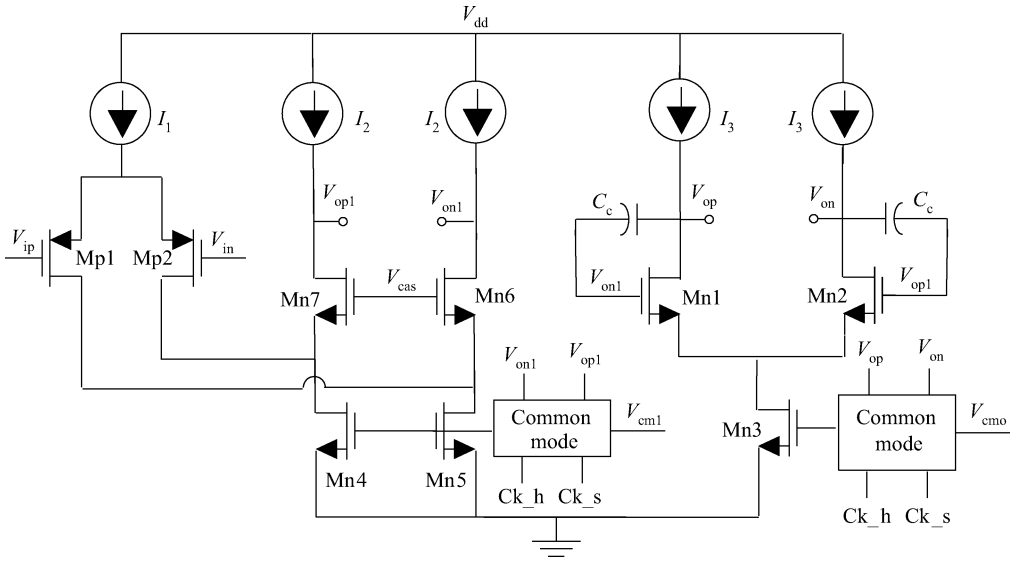

Fig. 3. Simplified diagram of the amplifier used in the design.

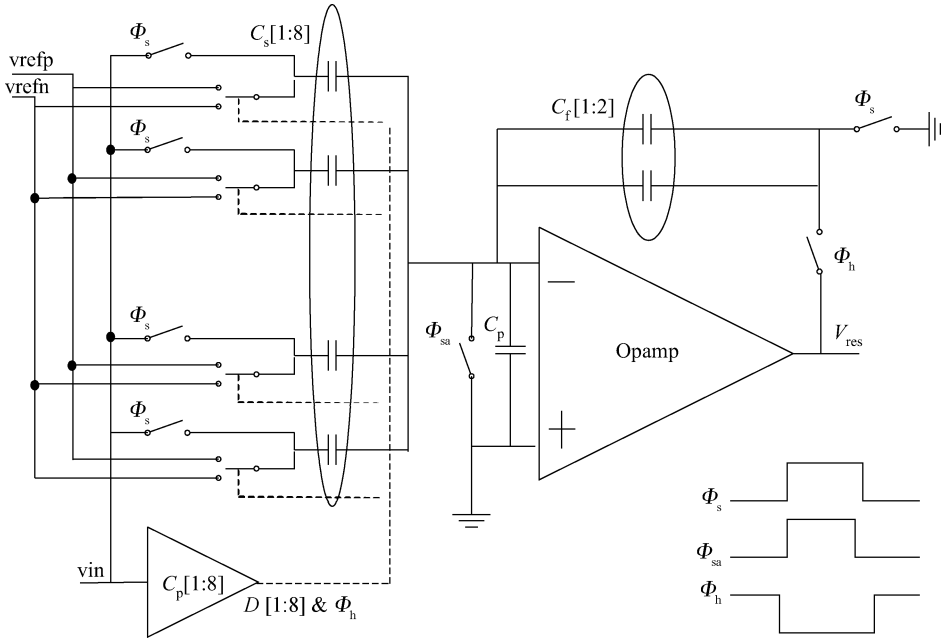

Fig. 4. MDAC configuration of the first stage.

tom reference V_{refn}, depending on the digital output of the sub-ADC, to set the residue voltage up at output.

Since the top plate of the sampling capacitor sample ground voltage during sampling phase Φ_s and the feedback factor of the amplification phase Φ_h is only

$$\beta = \frac{\sum_i C_s[i]}{\sum_i C_s[i] + \sum_i C_f[i] + C_p} \approx \frac{1}{5}, \tag{3}$$

the amplifier used in MDAC does not necessarily need to be unity gain stable, and the phase margin is greatly relaxed. Moreover, the small feedback factor makes the linear settling time significantly longer than the slewing time. This translates into a much lower bias current in the second differential stage, which often dominates the power consumption of the conventional unity gain stable and slew rate hungry two-stage amplifier design.

In this design, a thermometer coded capacitor array is chosen as the sub digital to analog converter because of the advantage of reduced interconnect complexity and the elimination of delay introduced by the encode circuit. Compared to the merged capacitor scheme mentioned in Ref. [17], a larger number of sample capacitors occupy a larger area, and this may make a systematic error of the capacitor dominant gain error and DAC error of the MDAC, which will introduce a large INL error and degrading dynamic range. Caution should therefore be taken on the layout of the capacitor array to balance random and systematic error.

2.2.3. On-chip reference

A stable reference buffer is critical for the performance of pipeline ADC. An on-chip reference buffer without external

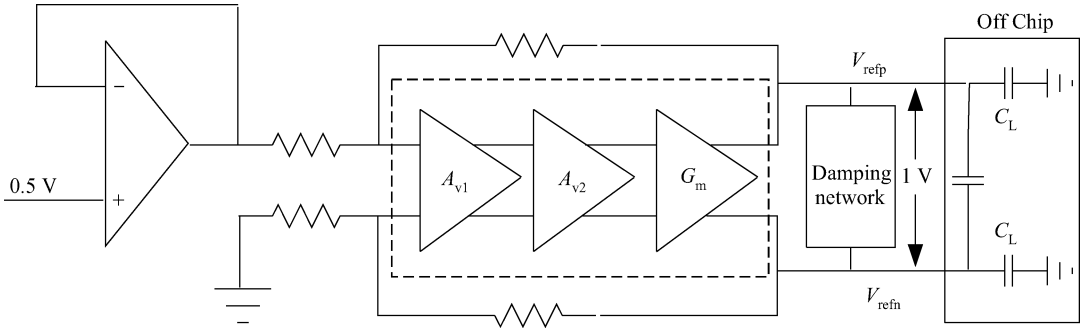

Fig. 5. Reference buffer.

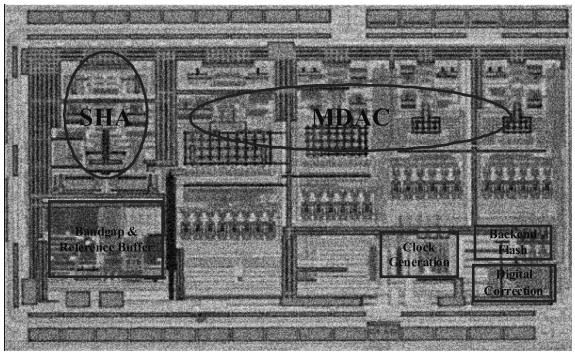

Fig. 6. Photomicrograph of the overall chip.

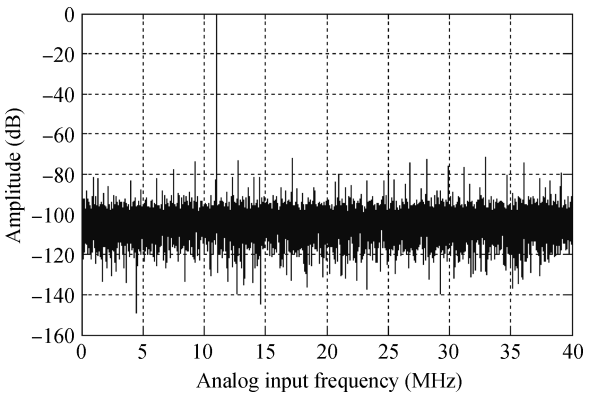

Fig. 7. FFT analysis results.

capacitor would consume a large amount of current because the buffer needs to be fast enough to charge or discharge the switched capacitor to a certain accuracy.

With the help of a large off-chip capacitor, on the one hand the thermal noise generated by the amplifier is largely attenuated. On the other hand, each capacitor switching activity only causes a small voltage variation in the off-chip capacitor without degrading the accuracy of the design, and as a result the buffer on-chip needs to keep the reference stable over a long period. But due to bonding wire induced inductance, the occurrence of ringing on the reference line may not be tolerable[12], therefore it is necessary to resort to an on-chip damping network to mitigate the effect.

Figure 5 shows the reference generator block. As shown in the figure, an internal bandgap generated 0.5 V voltage is buffered by a unity gain amplifier and then shifted through a single-to-differential amplifier to provide the 1 V differential reference voltage[11, 16]. From the figure, the reference buffer includes a transconductance amplifier that has a relatively large transconductance connected into the feedback loop to reduce the output impedance at low frequency. At DC the output impedance is represented by the expression $R_{\text{out}} = \frac{1}{A_{\text{v1}} A_{\text{v2}} g_{\text{m}}}$. The off-chip capacitor filters most of the high-frequency energy induced by the passive switched component.

3. Measured results

The ADC prototype was fabricated in SMIC 0.18 μm single-poly six-metal CMOS technology. The core occupies an area of 0.85 mm^2. Figure 6 shows a photomicrograph of the overall chip with the important components labeled.

Table 1. Key performance summary.

Parameter	Value
Process	0.18 μm 1P6M CMOS
Supply voltage	1.8 V
Sampling rate	80 MS/s
Resolution	10 bit
Full scale range	2 Vp-p
Area	0.85 mm^2
Power consumption	54 mW
DNL	+0.2/−0.5 LSB
INL	+0.8/−0.8 LSB
SFDR (f_{in} = 11 MHz, f_{s} = 80 MHz)	72.4 dBc
SNDR (f_{in} = 11 MHz, f_{s} = 80 MHz)	58.5 dB
ENOB (f_{in} = 11 MHz, f_{s} = 80 MHz)	9.4 bit

The current consumption of the whole chip in normal operation is 30 mA without digital driver. When a full scale input sine wave at f_{in} = 11 MHz is sampled with frequency f_{s} = 80 MHz, the measured results are SFDR = 72 dBc, ENOB = 9.43 bit, as shown in Fig. 7. The spurious tones presented in the FFT spectrum indicate the problem that the placement of the thermometer capacitor array in the first MDAC stage is not well designed, which introduces a kind of systematic error. Table 1 lists the key performance parameters of the design.

4. Conclusion

A 10 bit 80 MS/s optimized for WLAN analog front end is presented. It consists of a sample and hold stage for good dynamic range, four 2.5 bit per stage MDACs, followed by one 2 bit backend flash ADC, a digital error correction block, an on-chip low noise reference buffer and a non-overlapped clock generator. The ADC is fabricated in a 0.18 μm 1P6M CMOS process. The core area is 0.85 mm^2 and the power consumption is 54 mW. With an 11 MHz input frequency, the SNDR and SFDR are 58.5 and 72 dB at an 80 MHz sampling frequency, respectively.

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