Influence of drain and substrate bias on the TID effect for deep submicron technology devices

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Abstract: This paper presents a study of the total ionization effects of a 0.18 μm technology. The electrical parameters of NMOSFETs were monitored before and after irradiation with ^{60}Co at several dose levels under different drain and substrate biases. Key parameters such as off-state leakage current and threshold voltage shift were studied to reflect the ionizing radiation tolerance, and explained using a parasitic transistors model. 3D device simulation was conducted to provide a better understanding of the dependence of device characteristics on drain and substrate biases.

Key words: parasitic transistor; swallow trench isolation; total ionizing dose; off-state leakage
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1. Introduction

The aim of this work is to provide total dose effects analysis of core transistors in flash memory fabricated in commercial 0.18 μm CMOS processes. In modern bulk technologies, total ionizing effects are mainly due to the charge buildup in various dielectrics, such as silica and HfO_2[1]. The gate oxides of core devices in this technology node are as thin as 3 nm, and the total dose effects are sharply suppressed because of charge trapped in the oxide scale with T_{ox}[2]. As a result, total dose effects induced by gate oxide should be negligible. Prior to the introduction of STI (swallow trench isolation) dielectrics, commercial technologies often used LOCOS (local oxidation of silicon). The isolation dielectrics commonly used in deep submicron technologies are STI instead of LOCOS to increase component density, improve oxide quality, and reduce the stress of inter-metal dielectric stacks[3]. Furthermore, STI oxides have less lateral encroachment on the channel width than LOCOS oxides, which eliminates the bird's beak effect. However, STI oxides don't scale down like gate oxides, and as a result radiation induced charge trapped in the STI oxide, including bulk charge (N_{ot}) and interface charge (N_{it}) along the STI sidewall, could deplete or even invert the interface channel along the STI sidewall, leading to an increase in off-state leakage current[1,4].

Previously, a few papers have reported the total dose radiation effects on DIBL (drain-induced barrier lowing), including substrate bias influence on PMOS devices[5–7]. In this paper, we will first analyze the TID effects which are explained by the parasitic transistors model. The analysis of the dependence of TID effects on drain and substrate bias will be presented later. Finally, we will conduct 3D device simulation to validate and interpret the influence of the operating substrate and drain bias on TID effects.

2. Experimental details

All the devices were fabricated in 0.18 μm CMOS technology. STI acts as field isolation and the trench oxide thickness is about 400 nm. The gate oxide thickness is about 3 nm, and transistors with a channel width of 10 μm were used. The transistors were designed with a normal layout, and all the samples were ceramic packaged. The operating voltage is 1.8 V. Irradiation experiments were carried out at Xinjiang Technical Institute of Physics & Chemistry, Chinese Academy of Sciences, using a ^{60}Co γ irradiation source, typically at a dose rate of 200 rad(Si)/s. During radiation exposure, the gate of the device was biased at 1.8 V with all other terminals grounded. The temperature was monitored and kept at room temperature. Electrical measurements were obtained prior to irradiation and after step stress irradiation up to 100, 200, 250, 300, 400 and 500 krad(Si). Transfer characteristics (I_{ds}–V_{gs}) were measured in the linear region (V_{ds} = 0.05 V). In order to investigate the influence of drain bias on the TID effects, transfer characteristics (I_{ds}–V_{gs}) were measured at V_{ds} = 0.05/0.925/1.8 V. Similarly, transfer (I_{ds}–V_{gs}) characteristics were measured at V_{ds} = 0.05 V, V_{sub} = –1.8/–0.9/0 V to investigate the influence of substrate bias on the TID effects. These I_{ds}–V_{gs} curves were obtained within half an hour after irradiation exposure.

3. Results and discussion

3.1. I_{ds}–V_{gs} characteristics and the parasitic transistors model

Figure 1 shows typical I_{ds}–V_{gs} characteristics for n-channel transistors irradiated at V_{gs} = 1.8 V with other terminals grounded (ON bias) from 100 to 500 krad(Si). The device parameters were measured at V_{sub} = 0 V and V_{ds} = 0.05 V. At

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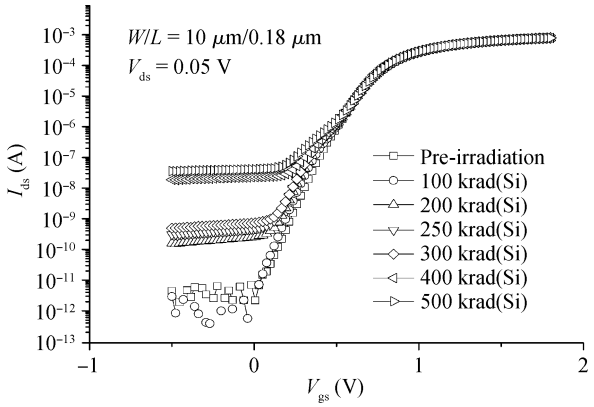

Fig. 1. I_{ds}–V_{gs} characteristics as a function of dose for the irradiated transistors with $W/L = 10/0.18$ μm.

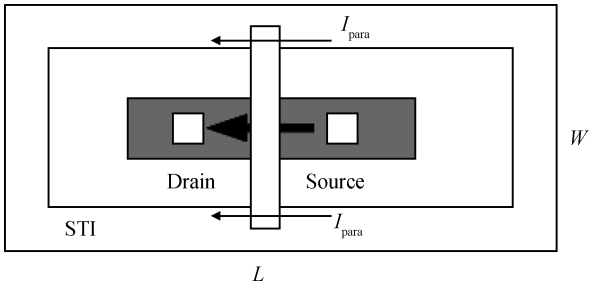

Fig. 2. Drain-to-source leakage path in an NMOSFET.

the dose level 200 krad(Si), a slight subthreshold hump appears and off-state leakage current reaches 0.1 nA, which is two orders larger than the pre-irradiated. Except for the case of 100 krad(Si) dose level, the off-state leakage current exhibits weak gate bias dependence, indicating that leakage current path induced by charge buildup in the deep interface along the STI sidewall is the main parasitic conduction rather than surface where parasitic transistors are well coupled with main transistor[6].

Figure 2 shows the radiation induced sidewall leakage which can be modeled by two parasitic transistors in parallel with the as-drawn transistor[2]. Prior to radiation exposure, the threshold voltage of parasitic transistors is high and drive current is low for the parasitic devices relative to the "as-drawn" structure. Upon exposure to ionizing radiation, the threshold voltage of parasitic devices is reduced significantly. This is because the "gate" oxide of parasitic structure is formed from the STI, which is much thicker than the "as-drawn" gate dielectric. In addition, holes trapped near the bulk/STI interface and in the bulk of STI act as a positive gate bias which depletes or inverts the P-type substrate. Besides negative voltage shifts, the drive current of the parasitic n-FET also increases significantly due to the fact that the effective width of parasitic transistors, to which drive current is proportional, increases as the surface along the STI sidewall inverts in response to charge buildup. In other words, the higher the irradiation dose, the larger the effective width of the parasitic transistors will be. However, up to 400 krad(Si), the parasitic transistors are in the strong inversion region and the off-state leakage current tends to be saturated since higher dose level (500 krad(Si)) induced leakage current doesn't increase proportionally.

The subthreshold hump effect becomes more pronounced after 400 krad(Si) because of the reduced STI parasitic corner channel transistor threshold voltage, from which we can conclude that at low dose irradiation (100, 200, 250, 300 krad(Si)) leakage current is mainly due to the channel deep in the interface along the STI interface being inversed or depleted by the charge trapped in the deep STI interface[9]. In other words, parasitic transistors near the deep STI/bulk have already turned on in relatively low doses ($\lesssim$ 300 krad(Si)). On the other hand, in the high irradiation dose parasitic surface channel transistors introduced by the charge trapped in STI corners start to affect the subthreshold characteristics of main channel transistor.

3.2. Leakage mechanism and the impact of drain bias

As shown in Fig. 3(a), the pre-irradiation I_{ds}–V_{gs} characteristic remains unchanged with variable drain biases. However, the irradiated device has a nearly two-order varied off-state leakage current with drain bias stepping from 0.05 to 1.8 V (Figs. 3(b), 3(c), and 3(d)). In contrast to the previously reported pre-irradiated I/O devices, which are hardened to V_{ds} variation in Ref. [11], core devices exhibit sensitivity to V_{ds} variation.

Several possibilities have been proposed for off-state leakage current: reverse-bias pn junction current ($I_{junction}$); GIDL, including gate oxide tunneling current (I_{gate}); and channel punchthrough current, including DIBL and bulk punchthrough current ($I_{channel}$). As a result, the total off-state leakage current is given by Eq. (1)[12]:

$$I_{off} = I_{junction} + I_{gate} + I_{channel}. \tag{1}$$

As illustrated in Fig. 3, the off-state leakage current is independent of gate bias under three drain biases, indicating that the leakage component I_{gate} has little contribution to the total leakage current I_{off}. Besides, the relationship between the GIDL current density J_{gate} and the applied voltage, i.e. $V_{gate-drain}$, is exponential as:

$$J_{gate} = A\frac{EV_{app}}{E_g^{1/2}}\exp\left(-BE_g^{3/2}/E\right), \tag{2}$$

$$A = \frac{\sqrt{2m^*}q^3}{4\pi\hbar^2},$$

$$B = \frac{4\sqrt{2m^*}}{3q\hbar},$$

where m^* is the effective electron mass; E_g is the energy band gap; V_{app} is the applied reverse bias; E is the electric field at the junction; q is the electronic charge; and $\hbar$ is $1/2\pi$ times Planck's constant. In other words, $I_{junction}$ and $I_{channel}$ dominate the total off-state leakage current.

Though larger leakage current corresponds to a higher irradiation dose level, up to 400 and 500 krad(Si), the leakage current becomes saturated, as shown in Figs. 3(c) and 3(d). The exponential relationship at low dose level between $I_{off\text{-}state}$ and TID indicates that the parasitic transistors are indeed in the linear region where the drain current's dependence on V_{ds} is as follows:

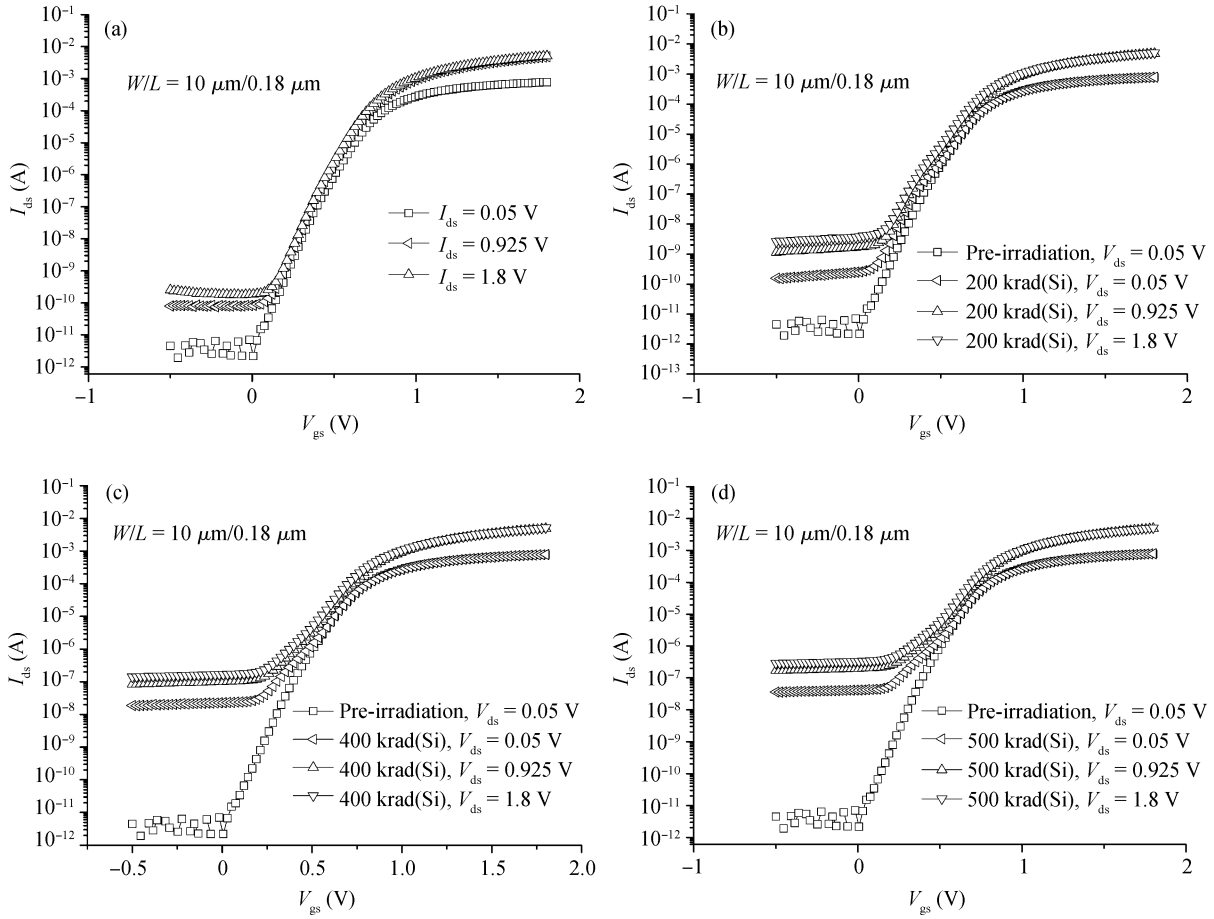

Fig. 3. Influence of drain bias on the pre-irradiated and irradiated transistors. (a) Pre-irradiation, (b) 200, (c) 400 and (d) 500 krad(Si).

$$I_{ds} = \mu_0 C_{ox} \frac{W}{L}(m-1)V_T^2 e^{(V_g - V_{th})/mV_T}(1 - e^{-V_{ds}/V_T}), \quad (3)$$

where V_{th} is the threshold voltage and V_T is the thermal voltage, C_{ox} is the gate oxide capacitance, μ_0 the zero bias mobility and m the subthreshold swing coefficient. Up to 400 and 500 krad(Si), the weakened exponential relationship between leakage current and TID suggests that the parasitic transistors are in the strong inversion region. The evolution from linear to saturation region of the parasitic transistors is illustrated in Fig. 4.

In short channel devices, due to the proximity of the drain and the source, the depletion regions at the drain–substrate and source–substrate junctions extend into the channel. The separation between the depletion region boundaries decrease. What's more, an increased reverse bias across the drain junctions will push together the two junctions. DIBL occurs when the depletion regions of the drain and the source interact with each other near the channel surface to lower the source potential barrier, resulting in a threshold voltage decrease. In order to quantitively characterize the influence of radiation on the threshold voltage shift, the DIBL effect parameter is defined by the following:

$$R = -\frac{\Delta V_{th}}{\Delta V_{ds}} = -\frac{V_{th}(V_{ds2}) - V_{th}(V_{ds1})}{V_{ds2} - V_{ds1}}. \quad (4)$$

Here, V_{th} was extracted by the constant current method, that is $V_{th} = V_{gs}$ @ $I_{ds} = 10^{-8}$ A. As shown in Fig. 5, the DIBL

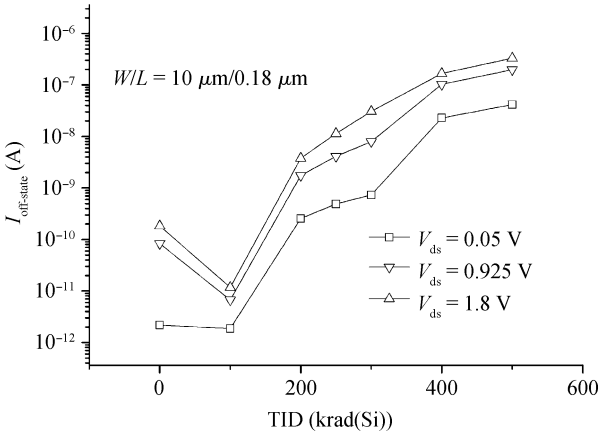

Fig. 4. Evolution of leakage current with TID for drain biases of 0.05, 0.925 and 1.8 V.

parameter increases sharply with the TID. The constant current method is improper in the case of 500 krad(Si) for the large leakage current. At doses below 200 krad(Si), although the off-state leakage current increased by about three orders, the DIBL parameter remained constant, which indicated that the conducting parasitic transistors were deep along the trench sidewall with little influence on the main transistor. At a high dose level, the DIBL effect induced threshold voltage shift is more apparent, revealing that the parasitic transistors are cou-

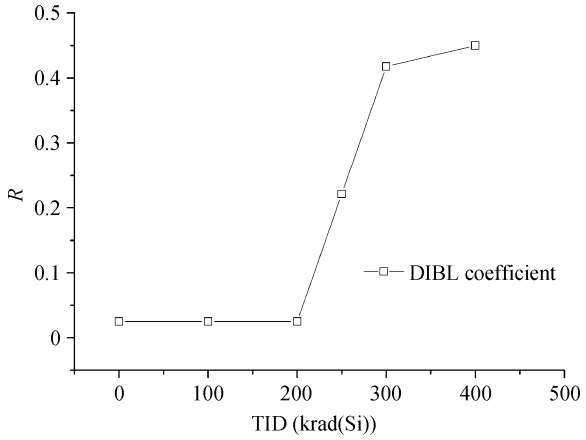

Fig. 5. DIBL parameter plotted against the total ionizing dose, except 500 krad(Si).

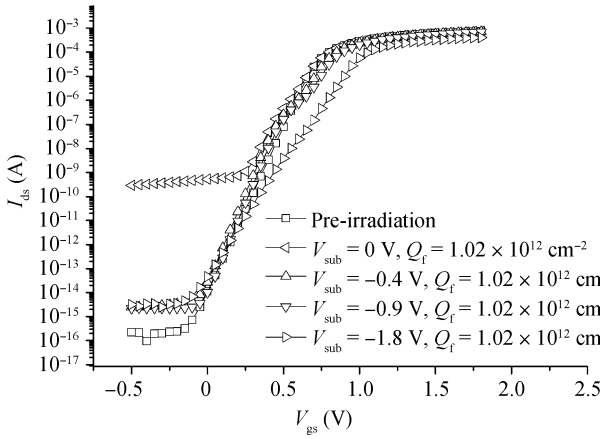

Fig. 7. Simulation results with uniform charge distribution along the STI interface for different substrate biases.

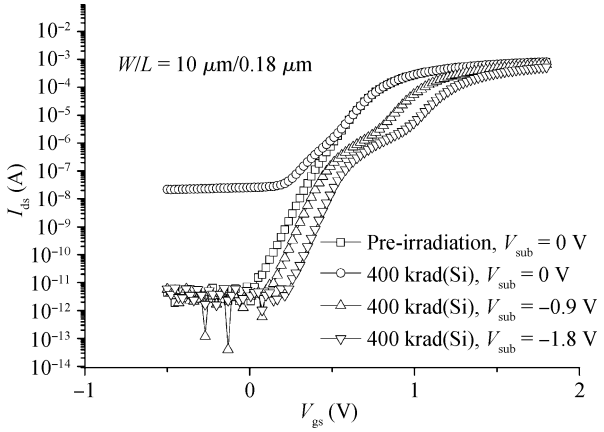

Fig. 6. Influence of substrate bias on the 400 krad(Si) irradiated transistor, compared with the pre-irradiated $V_{sub} = 0$ V.

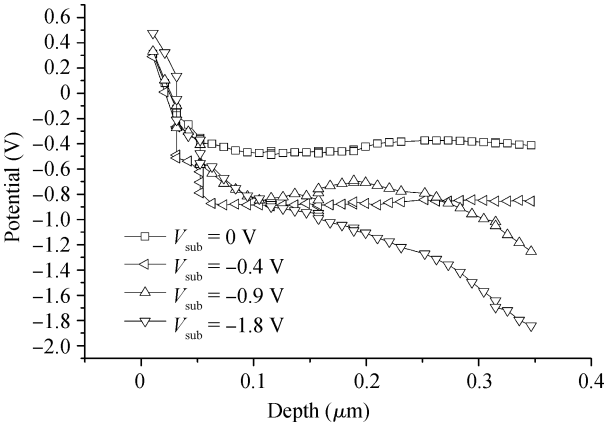

Fig. 8. Potential profile along the STI depth as a function of substrate bias.

pled with the main parasitic near the channel surface where three dimensional interactions take effect.

3.3. Impact of substrate bias during measurement

As shown in Fig. 6, the I_{ds}–V_{gs} characteristics of 400 krad(Si) for operating substrate biases $V_{sub} = 0$ V, $V_{sub} = -0.9$ V and $V_{sub} = -1.8$ V are compared with the corresponding pre-irradiation. During irradiation, V_{gate} was 1.8 V, with all other terminals grounded. Both −0.9 and −1.8 V effectively suppress the STI off-state leakage current, that is cutting off the parasitic conduction induced by STI trapped charge for $V_{gs} < 0$ V. The I_{ds}–V_{gs} characteristics look like those of a pre-irradiation device, except for the stretched-out subthreshold hump and threshold voltage shift. The subthreshold hump is caused by the V_{th} lowing of the surface corner channel inverted by the STI corner trapped charge[12].

To confirm the previous analysis of substrate bias effect, we conducted a 3D simulation using the Silvaco TCAD tool[14]. According to Ref. [15], considering the case of "overfilled" STI structure (as in our case here), the simulation results did not show the subthreshold hump effect with uniform charge distribution placed along the STI sidewall applied in the model, in contrast to "planar" trench or "recessed" trench. Thus uniform interface charge densities of 1.02 × 10^{12} cm^{-2} were placed in the STI sidewall/bulk interface during simulation, since the STI structure of our irradiated device is overfilled[16]. However, the results show that after adding a negative bias to the substrate, a subthreshold hump is obvious.

Figure 7 shows the simulation results of the I_{ds}–V_{gs} characteristics when a uniform interface charge of 1.02 × 10^{12} cm^{-2} is combined with substrate bias. The results clearly show that a negative substrate bias suppresses the parasitic inversion due to STI interface charge even at a low value, −0.4 V, and that uniform charge distribution could also induce a subthreshold hump, though this is relatively smaller than nonuniform charge distribution[11]. This is because of the higher electrical field when the substrate applies a negative bias voltage that there is a small subthreshold hump.

Figure 8 shows a comparison between the potential profile along the STI interface of $V_{sub} = 0$, −0.4, −0.9 and −1.8 V. As we can see from Fig. 8, the potential of $V_{sub} = 0$ V is apparently larger than that of $V_{sub} = -1.8$ V, and therefore the inversion region is wider, which means that the width of the parasitic transistor is also larger, inducing more conducting current in the subthreshold region. On the other hand, as shown in Fig. 8, opposed to an accumulated surface in the main channel at $V_{sub} = 0$ V, a depleted layer is created at the main channel surface,

which enhances the control of the main channel and decreases the off-state leakage current greatly. Though a negative substrate bias after irradiation could obviously suppress off-state leakage, devices which were irradiated with negative bias became worse[16]. This is complicated, so we must be careful when choosing the substrate bias.

4. Conclusion

We presented the experimental results of gamma irradiation effects on the STI leakage current in a 0.18 μm technology, in particular those influenced by the drain and substrate bias. The charge buildup in the STI is found to be the main reason for off-state leakage, and the parasitic transistors model is introduced to explain it. The DIBL effect interprets the effect of off-state leakage at $V_{gs} = 0$ V and substrate hump well. A negative substrate bias can be used to effectively suppress the STI leakage, which could however increase the threshold voltage and introduce a severe substrate hump. Substrate potential profiles along the STI depth, provided by TCAD tool simulation, agree with the assumption that negative substrate bias decreases the width of the parasitic transistors, thus suppressing STI leakage.

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