A novel structure for improving the SEGR of a VDMOS*

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Abstract: The mechanism of single-event gate-rupture in an N-channel VDMOS in a space radiation environment was analyzed. Based on the mechanism, a novel structure of VDMOS for improving single-event gate-rupture is proposed, and the structure is simulated and it is demonstrated that it can improve a VDMOS SEGR threshold voltage by 120%. With this structure, the specific on-resistance value of a VDMOS is reduced by 15.5% as the breakdown voltage almost maintains the same value. As only one mask added, which is local oxidation of silicon instead of an active processing area, the new structure VDMOS it is easily fabricated. The novel structure can be widely used in high-voltage VDMOS in a space radiation environment.

Key words: VDMOS; single event gate-rupture; local oxidation of silicon; specific on-resistance
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1. Introduction

In recent years, with the rapid development of space walks, outer space exploration, the use of atomic energy and nuclear science, the number of micro-electron devices that are used in space radiation environments grows daily. Especially, the VDMOS is a key component of DC/DC converters, which supply power for satellites. Hence many companies and institutions are paying more and more attention to research and exploration in this area. In 1983, the US launched the Strategic Defense Initiative, which included space-based systems, and micro-electron device radiation hardening research has been done by most governments. In order to take advantage of the possibility of outer-space exploration, the micro-electron device radiation-hardening is the one of most important issues that needs to be resolved.

Nowadays, it is widely accepted that single-event gate rupture (SEGR) can be initiated from an ion striking the neck region, if certain conditions are met. The lowest SEGR threshold voltages occur when the ion strike is perpendicular to the die surface and the most sensitive strike location is the center of the neck region[1−3]. The neck region is defined as the area separating the p-body regions of the VDMOS cells. When an ion strikes this region, it creates a dense track of electron–hole pairs, which shunts the protective layer defined by the depletion region causing a portion of the drain voltage to reach the Si–SiO_2 interface, which is shown in Fig. 1. As is known, for an N-channel MOSFET with a positive drain voltage in an off-state condition, the applied field causes the holes to drift to the Si–SiO_2 interface where they pile-up while slowly diffusing toward the p-body/source contact. As the holes density at the Si–SiO_2 interface increases, the potential across the oxide above the neck area increases. If this potential exceeds the minimum potential to induce SEGR, then gate-oxide breakdown occurs and holes are injected through the oxide causing a permanent resistive short due to localized heating. This condition is referred to as SEGR[1−3].

In this paper, a novel structure for improving the SEGR of VDMOS is proposed, and its tech-scheme is to increase the oxide thickness by the local oxidation of silicon (LOCOS), which can endure an applied field and causes the holes/electrons to drift to the Si–SiO_2 interface. Using the proposed structure, the lowest SEGR threshold voltage is improved and the specific on-resistance (R_{ON}) value of the VDMOS reduces by 15.5% than that of the traditional VDMOS structure, as the breakdown voltage almost maintains the same value. In addition, instead of an ACTIVE mask, only one mask, called the LOCOS mask, is used in the novel structure manufacturing process, and the novel structure can also be widely used in high-voltage VD-

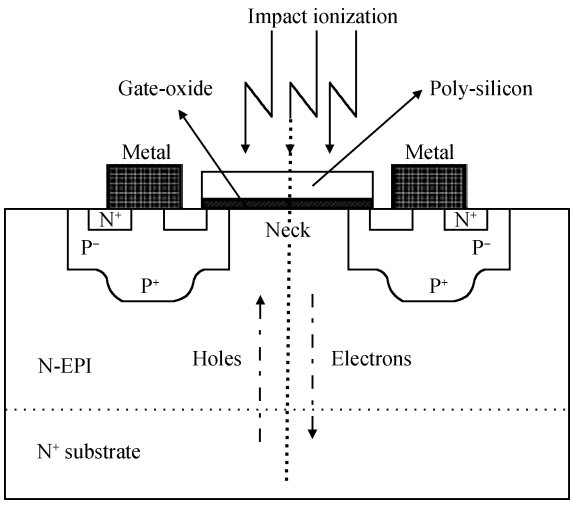

Fig. 1. Sketch map of the impact ionization strike VDMOS.

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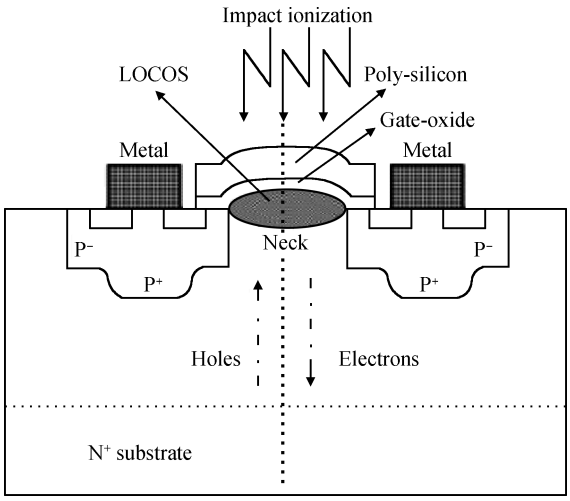

Fig. 2. Cross section of the proposed VDMOS structure.

MOS in space radiation environments.

2. Structure and analysis

2.1. Device design

From Ref. [4], we can know that the breakdown voltage of the 10 nm oxide layer is about 5–10 V, and the thickness of the gate oxide for a common VDMOS is about 60–80 nm, hence the breakdown voltage of the gate oxide for a common VDMOS being lower than 80 V. In order to enhance the breakdown voltage and maintain other parameters at the same time, a novel structure is proposed, which is shown in Fig. 2. The LOCOS technology is used, of which the thickness is 1.7 μm, and it is appropriate for a 200 V N-channel VDMOS. Hence the difference between the proposed structure and traditional VDMOS structures is that the LOCOS structure is fabricated before gate oxidation in high-press oxidation.

From Fig. 2, we can know that the LOCOS structure is above the neck area of a VDMOS, and the numbers of holes/electrons which are piled-up by the source will increase. At the same time, the channel length and gate oxide thickness are maintained in the new structure, and hence the threshold voltage and breakdown voltage of the proposed VDMOS can also be maintained. In addition, the 1.7 μm oxide can endure an applied field that causes the holes/electrons to drift to the $Si–SiO_2$ interface much better than 60–80 nm oxide for a common VDMOS. Finally, using the proposed structure, the lowest SEGR threshold voltage can be improved obviously.

The designed process for the novel structure of N-channel 200 V-VDMOS is as follows:

Field oxide → guard ring photo/etch → boron implant → anneal → strip oxide → thin oxide → LPCVD SiN → LOCOS photo/etch → high-press oxide → strip SiN → BOE → gate oxide → LPCVD poly-silicon → poly-silicon doping → poly-silicon oxide → PBODY photo/etch → boron implant → PBODY anneal → source photo/etch → phosphorus implant → P^+ photo/etch → boron implant → LPCVD SiO_2 → anneal → contact photo/etch → metallization → passivation → test.

With regard to the structure and process mentioned above, the simulated cross section of the proposed structure is shown in Fig. 3.

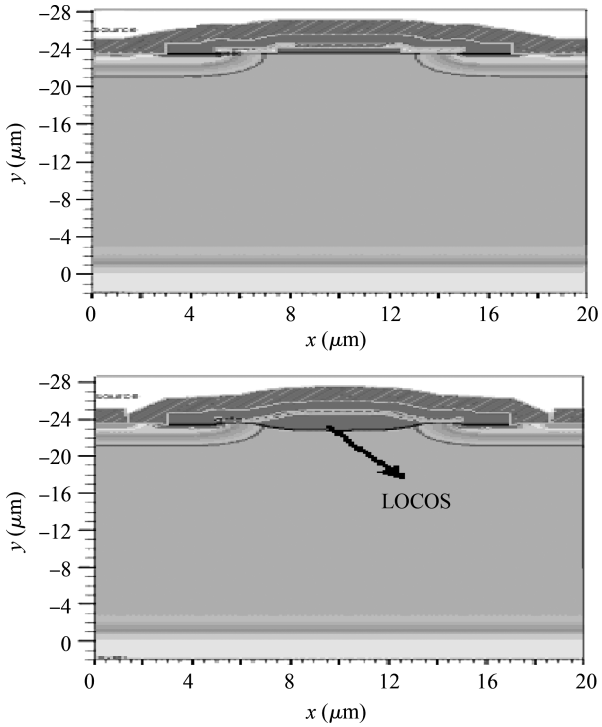

Fig. 3. Simulated cross section of (a) the common structure and (b) the proposed structure. Cell size is 20 × 20 μm^2.

2.2. On-resistance analysis

The R_{ON} of the VDMOS is made up of several components, and the contact resistance between the source and drain metallization and the silicon, metallization and lead-frame are ignored, because these are normally negligible in high voltage devices[4–6], such as 200 V. The R_{ON} of VDMOS is given by

$$R_{ON} = R_{CS} + R_{CH} + R_{NECK} + R_{EPI} + R_{SUB} + R_{CD}, \quad (1)$$

where R_{CS} is the contact resistance between the source metallization and the silicon and source diffusion resistance, R_{CH} is the channel resistance, R_{NECK} is the component-resistance of the region between the two body regions, R_{SUB} is the substrate resistance and R_{CD} is the contact resistance between the drain metallization and the silicon.

From Refs. [4–6], R_{EPI} is the most important component in high-voltage VDMOS, and is more than 50% in 200 V N-channel VDMOS.

3. Simulation and validation

The LOCOS structure above the neck of the proposed VDMOS is inlayed into the neck area, and 0.75 μm thickness of the extension layer is depleted in a high-press oxide process. Virtual N-epi is reduced by 0.75 μm, and the R_{ON} and BV_{DSS} will be changed. So it is necessarily to find out the trade-off between change value and SEGR.

In order to validate the effect of the proposed structure, 3D structures of the common VDMOS structure and the proposed

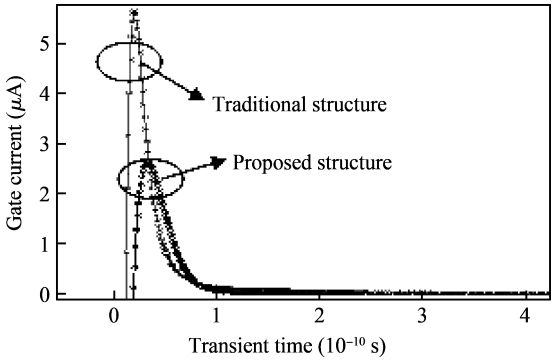

Fig. 4. Simulated curves between the gate current and the transient time of the proposed structure and the traditional structure at the same radiation condition.

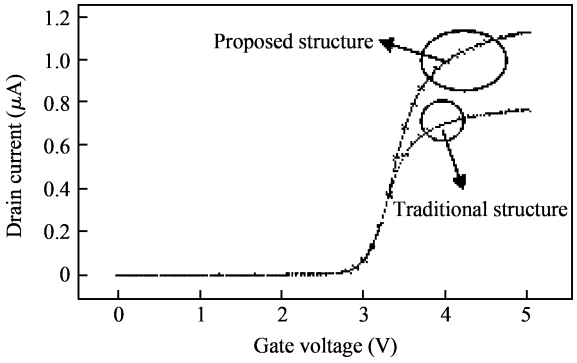

Fig. 6. Simulated transfer characteristic curves of the proposed structure and traditional structure at $V_{DS} = 0.1$ V.

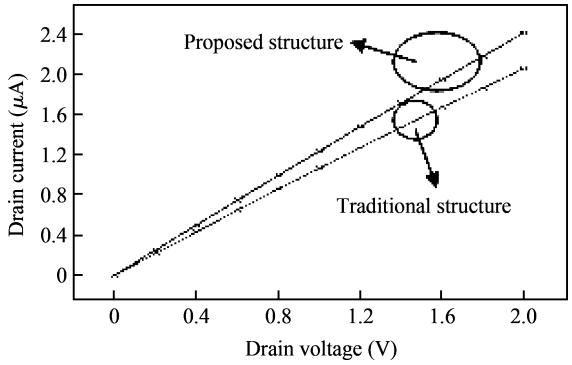

Fig. 5. Simulated specific R_{EPI} curve of the proposed structure at $V_{DS} = 2$ V and $V_{GS} = 15$ V.

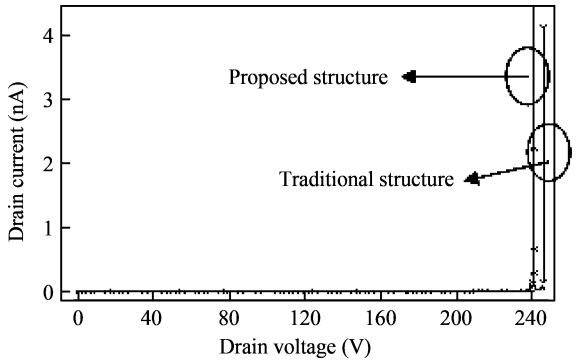

Fig. 7. Simulated breakdown curves of the proposed structure and traditional structure at $V_{GS} = 0.1$ V.

VDMOS structure are simulated by using SILVACO software. The radial distance, length, and time dependence of generated charge along tracks are specified. There can be a single particle strike or multiple strikes. Each track is specified by an entry point location (x_0, y_0, z_0) and an exit point location (x_1, y_1, z_1). This is assumed to be a cylinder with the radius defined with the RADIUS parameter[1, 7]. Certainly, the electron/hole pairs generated at any point is a function of the radial distance. Finally, in contrast to the gate current between the two different structures, and the effect of the proposed structure in improving SEGR can be validated.

Using the proposed structure, the curves between the gate current and the transient time of the proposed structure and the traditional structure at the same radiation condition are implemented, and the simulated results are shown in Fig. 4. From them, we can know than the maximal gate current of the traditional structure is 5.5×10^{-6} A, and that of the proposed structure is 2.5×10^{-6} A. Hence the lowest SEGR threshold voltage value of the novel structure is improved by 120%, which is used to validate that the proposed structure can improve the lowest SEGR threshold voltage of a VDMOS.

At the same time, using the process steps described above, the specific R_{ON}, V_{TH} and BV_{DSS} are simulated. The simulated curve between specific R_{ON} and V_{DS} is shown in Fig. 5, the specific R_{ON} value of traditional structure is 1824200 $\Omega/\mu m^2$, the value of the novel structure is 1579600 $\Omega/\mu m^2$, the specific R_{ON} value reduced by 15.5% than that of the traditional structure as the BV_{DSS} almost maintained the same value.

Figure 6 shows the simulated transfer characteristics curves between the drain current and the gate voltage at $V_{DS} = 0.1$ V, and the gate voltage changed from 0 to 5 V. From Fig. 6, the threshold voltage of the gate source is 3.1 V, and there is no change between the proposed structure and the traditional structure.

Figure 7 is the simulated breakdown curves between the drain current and the drain voltage at $V_{GS} = 0.1$ V, and drain voltage changes from 0 to 250 V at 5 V a step. From Fig. 7, the breakdown voltage of the proposed structure is 243 V, and the breakdown voltage of traditional structure is 246 V. So there is almost no change between the proposed structure and the traditional structure.

4. Conclusion

A novel structure of VDMOS for improving SEGR is developed. The simulated results show that the SEGR threshold voltage will improve by 120%, the R_{ON} value is reduced by 15.5% using the proposed structure, and there almost is no change for the V_{TH} and BV_{DSS} of the VDMOS. In addition, only one mask is used, which is local oxidation of silicon instead of an active area in processing the new structure VDMOS, which is easily fabricated. The novel structure and its process are simulated and demonstrated to be appropriate for high-voltage VDMOS in space radiation environments.

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