Novel method of separating macroporous arrays from p-type silicon substrate*

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Abstract: This paper presents a novel method to fabricate separated macroporous silicon using a single step of photo-assisted electrochemical etching. The method is applied to fabricate silicon microchannel plates in 100 mm p-type silicon wafers, which can be used as electron multipliers and three-dimensional Li-ion microbatteries. Increasing the backside illumination intensity and decreasing the bias simultaneously can generate additional holes during the electrochemical etching which will create lateral etching at the pore tips. In this way the silicon microchannel can be separated from the substrate when the desired depth is reached, then it can be cut into the desired shape by using a laser cutting machine. Also, the mechanism of lateral etching is proposed.

Key words: electrochemical etching; MCP; macroporous silicon; p-type silicon; separation

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1. Introduction

Glass microchannel plates (MCP) have been widely used in applications such as electron multipliers[1] and three-dimensional Li-ion microbatteries[2]. However, the relatively low operation temperature limits their applications. The development of silicon MCP (SiMCP) technology makes it possible to solve this problem. SiMCP can be baked at a temperature of 1200 ℃, which is much higher than that possible with glass MCP. In addition, the placement, size, and pore uniformity of SiMCP substrate channels have dimensional precisions greatly exceeding that of glass-fiber-based MCP[3]. In general, fabrication of high-quality SiMCP includes macropore array formation and separation from the substrate. Traditionally, the macropore array is separated by using methods such as grinding and polishing, plasma etching, or chemical back thinning[4]. Nevertheless, these methods are not only costly but may destroy the SiMCP structure, especially for p-type SiMCP with thin pore walls often less than 1 μm.

However, the method to separate macropore arrays from the silicon substrate by electochemical etching is supposed to be an easy and effective way, which has been studied by Ohji *et al.* They presented a technique of fabricating free-standing structures using single-step electrochemical etching for n-type silicon[5]. For p-type silicon, Chao *et al.* noticed that after prolonged anodization, the entire macroporous silicon layer could be electrochemically polished resulting in a self-supported macroporous silicon membrane[6]. Pagonis *et al.* presented a two-step electrochemical process for the formation of free-standing macroporous silicon membranes[7] and the phenomena were also reported by our group[8, 9]. In this paper, a technique to separate macropore arrays from the p-type silicon substrate by adding a modified electrochemical etching step is presented.

2. Experimental details

The sample is etched in 2 mol/L HF under 15 V anodic bias at room temperature with the etching current density between 6 and 20 mA/cm^2, which are modified based on our group's work in Refs. [8, 9]. The electrolytes were prepared by mixing HF (40% aqueous solution), N, N-Dimethylformamide (DMF, 99.5%), and deionized water at a volume ratio 1 : 4 : 5[10]. A non-ionic surfactant Triton X-100 was used to remove bubbles[11] and HCl was added to adjust the pH value between 1–4 to passivate the pore wall[12]. The set-up consisted of a double cell and LED arrays with a wavelength of 850 nm, as shown in Fig. 1 (see Ref. [13] p.19–20). To illuminate the whole silicon wafers, wafer-size LED arrays showed the best results (see Ref. [13] p.72). A platinum grid (9 cm in diameter) was used as the counter electrode (with a negative bias) and another platinum grid with the same size as a working electrode (with a positive bias). The current was adjusted by the light intensity. The whole system was controlled by a LabVIEW (a software from National Instruments corporation) operated computer system.

The process flow for fabricating Si MCP is described in detail by our group in Ref. [8]. The starting materials were 100 mm, 5–15 Ω·cm, single-side-polished p-type (100) silicon wafers with a thickness of 525 μm. The high power LED arrays were made up of 49 IR-LEDs (Each is 1 W with a wavelength of 850 nm). In order to protect the LED arrays, the illumination voltage was limited between 0–11.5 V. Silicon dioxide layer (300 nm) was grown on the wafer by thermal oxidation and

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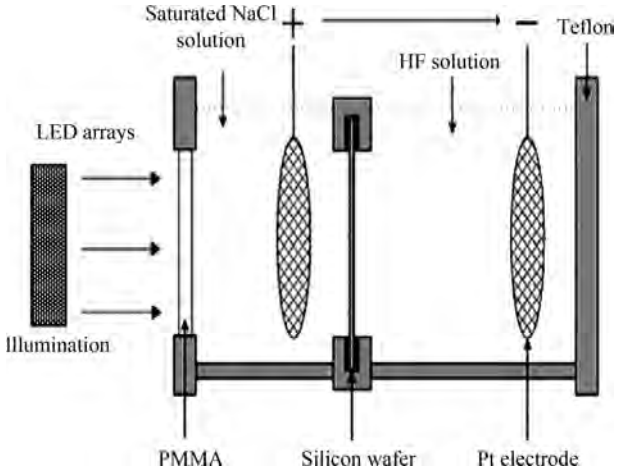

Fig. 1. Electrochemical set-up.

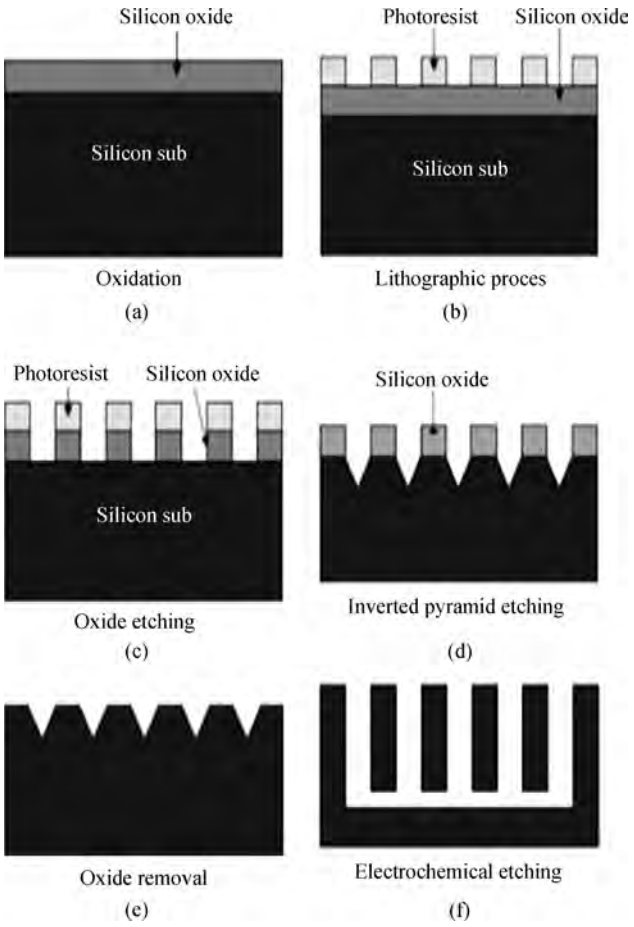

Fig. 2. Process flow for SiMCP.

patterned by a standard photolithographic process, and then the windows were opened and pyramidal notches were created by tetramethyl ammonium hydroxide (TMAH: 25wt%) etched at 85 ℃ for a few minutes. The wafer was then etched in the set-up depicted in Fig. 1. When the desired depth was reached, the current density was increased while keeping the bias constant or the bias was reduced while keeping the current density constant until the illumination voltage increased to 11.5 V. Etching in the lateral direction under the trenches then began. The

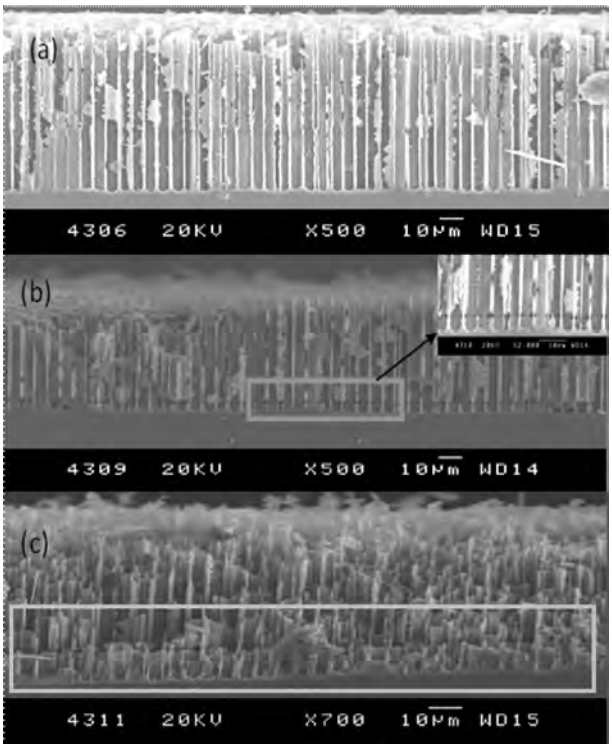

Fig. 3. SEM images showing cross-section views of (a) sample 1, (b) sample 2, and (c) sample 3.

process lasted long enough for separation of the microchannel plate layer from the substrate to be realized, as shown in Fig. 2(f).

3. Results and discussion

Figure 3 shows the SEM images corresponding to the cross-sectional views of three samples prepared by the process shown in Figs. 2(a)–2(e), and etched using the set-up shown in Fig. 1 under the same conditions (bias: 15 V and current density: 10 mA/cm^2) for 4 h. Sample 1 was etched under the same conditions for another hour as a reference and sample 2 was etched by decreasing the bias to 5 V until the illumination voltage was up to 11.5 V while the current density was kept constant for one hour more. Sample 3 was etched by increasing the current density to 19 mA/cm^2 by adjusting the illumination voltage up to 11.5 V while keeping the bias constant for another hour. The macropore arrays of samples 2 and 3 were undercut as shown in Figs. 3(b) and 3(c), but that did not happen to sample 1 (Fig. 3(a)). The mechanism may be understood in this way. During electrochemical etching, when the necessary number of reaction particle F^- for the formation of the macropores exceeds that of holes in the pore tips, etching will occur in the pore tips due to the geometric field enhancement and straight pores are formed as shown in Fig. 4(a). However, if the number of holes exceeds that of F^-, the additional holes will diffuse to the pore walls and create lateral etching, as shown in Figs. 4(b) and 4(c), and the tips will form in the pore walls. Thus, lateral etching is enhanced and the trenches are connected under the structures as shown in Fig. 4(d).

It is not easy to determine when the number of holes is superfluous during electrochemical etching. Here, we propose

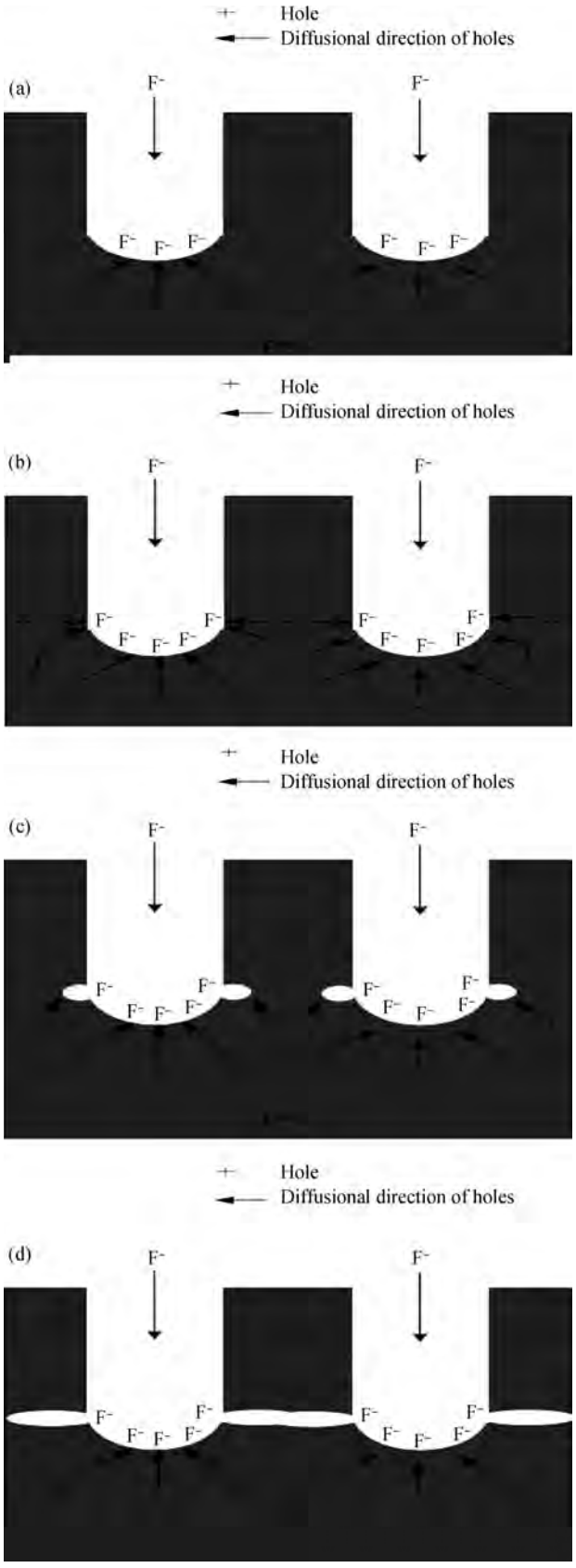

Fig. 4. Schematic diagram of the formation of free standing silicon structure.

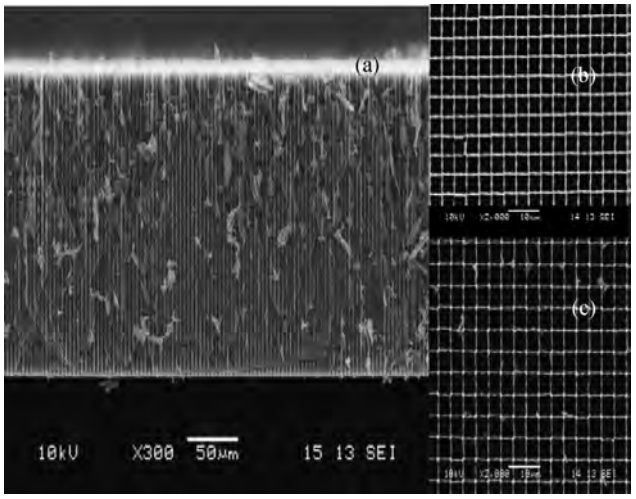

Fig. 5. SEM images of a SiMCP separated from a sample which was etched at 9 mA/cm^2 with the applied bias of 15 V for 662 min. (a) Cross section. (b) Front side. (c) Backside.

that superfluous holes are generated by increasing the illumination voltage to the upper limit (11.5 V). As holes are excited by backside illumination, the maximum voltage corresponds to the most number of holes. Actually, the current density is proportional to the bias and light intensity[14]. During constant current density etching, if the bias is decreased, the light intensity has to be increased to keep the current density constant. In constant bias etching, the light intensity has to be increased if we want to increase the current density. Thus, a process where increasing the current density while keeping the bias constant or decreasing the bias while keeping the current density constant until the illumination voltage is increased to 11.5 V is adopted to generate additional holes.

In fact, decreasing bias can enhance lateral etching by another mechanism. Because the etching current I is made up of two parts, $I = I_{\text{tip}} + I_{\text{wall}}$. One is tip current I_{tip}, which stands for vertical etching, and the other is wall current I_{wall}, which stands for lateral etching. At zero bias, $I_{\text{tip}} = I_{\text{wall}} = 0$, when a forward bias is applied, the I_{tip} increases much faster than I_{wall} due to geometric field enhancement. If the bias is high enough, I_{tip} become decisive, $I_{\text{wall}}/I_{\text{tip}} \approx 0$ and $I \approx I_{\text{tip}}$[15]. Thus, decreasing bias while keeping the current density constant can increase the value of $I_{\text{wall}}/I_{\text{tip}}$ and enhance lateral etching.

In electrochemical etching, the concentration of F^- at the pore tips will decrease with increased pore depth (see Ref. [9] and Ref. [13] p.201). Hence, if a sample is etched at a constant current and fixed voltage, the concentration of F^- will not be able to maintain etching at last with increasing pore depths. As the current density is adjusted by the light intensity, the illumination voltage will increase and reach the upper limit, meaning that lateral etching begins. Figure 5 shows the SEM images of a sample etched at 9 mA/cm^2 and applied bias of 15 V for 662 min. The illumination voltage reaches the upper limit in the 632nd minute then after 30 min, etching is stopped and the macroporous array is separated from the substrate. The pores on both sides of the SiMCP are in good condition, as shown in Figs. 5(b) and 5(c). Hence, this technique can be used to separate maroporous arrays from p-type silicon substrates.

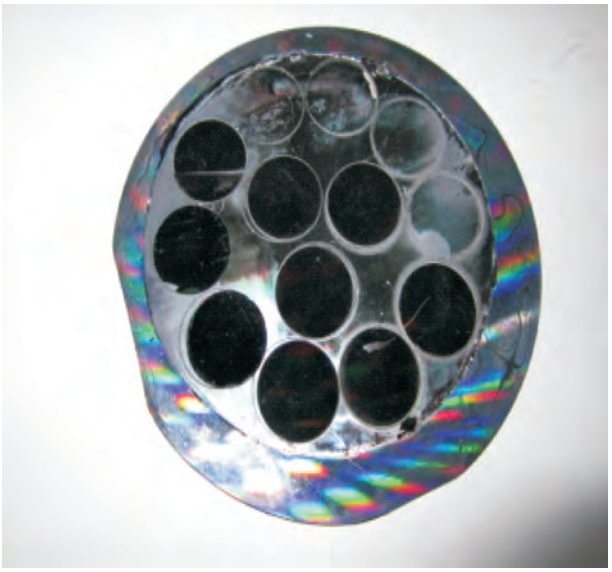

Fig. 6. Photograph of SiMCP which was cut into circle shapes by a laser cutting machine.

4. Conclusion

A method to separate macropore arrays from p-type silicon substrate to fabricate MCP is presented. Single-step electrochemical etching by increasing the current density while keeping the bias constant or decreasing the bias while keeping the current density constant is effective for fabricating MCPs. In addition, that the illumination voltage reaches the upper limit as a symbol of lateral etching having begun is proposed, which is very useful for computer control by detecting the potential. Another method that keeps the etching current density and bias constant, and then keeps etching for a few minutes more after the illumination voltage reaches the upper limit value is also described. Moreover, the Si MCP obtained by above methods can be easily machined into various shapes by laser cutting, as shown in Fig. 6.

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