Gate leakage current reduction in IP3 SRAM cells at 45 nm CMOS technology for multimedia applications

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Abstract: We have presented an analysis of the gate leakage current of the IP3 static random access memory (SRAM) cell structure when the cell is in idle mode (performs no data read/write operations) and active mode (performs data read/write operations), along with the requirements for the overall standby leakage power, active write and read powers. A comparison has been drawn with existing SRAM cell structures, the conventional 6T, PP, P4 and P3 cells. At the supply voltage, $V_{DD} = 0.8$ V, a reduction of 98%, 99%, 92% and 94% is observed in the gate leakage current in comparison with the 6T, PP, P4 and P3 SRAM cells, respectively, while at $V_{DD} = 0.7$ V, it is 97%, 98%, 87% and 84%. A significant reduction is also observed in the overall standby leakage power by 56%, the active write power by 44% and the active read power by 99%, compared with the conventional 6T SRAM cell at $V_{DD} = 0.8$ V, with no loss in cell stability and performance with a small area penalty. The simulation environment used for this work is 45 nm deep sub-micron complementary metal oxide semiconductor (CMOS) technology, $t_{ox} = 2.4$ nm, $V_{thn} = 0.22$ V, $V_{thp} = 0.224$ V, $V_{DD} = 0.7$ V and 0.8 V, at $T = 300$ K.

Key words: gate leakage; subthreshold leakage; low power; deep sub-micron; SRAM
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1. Introduction

In the last few years, the demand for processors with high processing capability and low power dissipation has increased at a rapid rate. Significant efforts have been made to design low-power static random access memories (SRAMs), since they are used in the cache memory, e.g. the L_1, L_2 and L_3 cache, of high-performance and mobile (battery powered application) processors. To achieve low power dissipation, we have to decrease the power consumption, both in the active and standby mode of memory operation. But the scaling down of complementary metal oxide semiconductor (CMOS) technology has raised issues related to leakage currents and its various components, which were not previously considered at micron-sized CMOS technology, and this is increasing at an alarming rate as the technology is being scaled down to achieve more functionality (area efficiency) and low power requirements. Leakage current is therefore considered as a critical design parameter in both high-performance processors and battery-powered handheld/portable applications in deep submicron (DSM) technology[1]. The International Roadmap for Semiconductors predicts a gate equivalent oxide thickness as low as 0.5 nm for future CMOS technologies[2]. The scaling of CMOS transistors is resulting in an increase in the gate leakage and subthreshold leakage current. The gate leakage is predicted to increase at a rate of 500× per technology generation, whereas subthreshold leakage is predicted to increase by 5×[2]. Gate leakage current therefore needs to be addressed carefully in the design process of very large scale integration circuits at the DSM regime. Out of the existing gate leakage reduction techniques, one of the most popular techniques is the use of a high-k gate dielectric material[3]. But further scaling of high-k deposition film will start to cause the same issues of leakage. So, to overcome these problems, a significant amount of attention is being paid at the device and circuit level of various SRAM cell structures.

In this paper, leakage current analysis is given for the conventional 6T, PP, P4, P3 and IP3 cells. All the simulations are carried out using 45 nm CMOS technology.

2. Conventional 6T and IP3 SRAM cells: a brief overview

2.1. Conventional 6T SRAM cell

The conventional SRAM cell has six MOS transistors, as shown in Fig. 1. As opposed to DRAM, it doesn't need to be refreshed as the bit is latched in it, and it can operate at lower supply voltages and has large noise immunity. However, the six transistors of an SRAM cell take up more space than a DRAM cell (which is made of only one transistor and one capacitor), thereby increasing the complexity of the cell[4].

The SRAM memory bit-cell has two CMOS inverters connected back to back (M1, M3, and M2, M4). The two pass transistors (M5 and M6) are the access transistors controlled by the word line (WL), as shown in Fig. 1. The cell preserves its one of two possible stable states, "0" or "1", as long as power is available to the bit cell. The SRAM cell draws current from the power supply only during switching. In the idle state the static power dissipation is zero, ideally. But at the DSM level the leakage power consumption is becoming a growing concern in modern mobile processors, even when the SRAM is in

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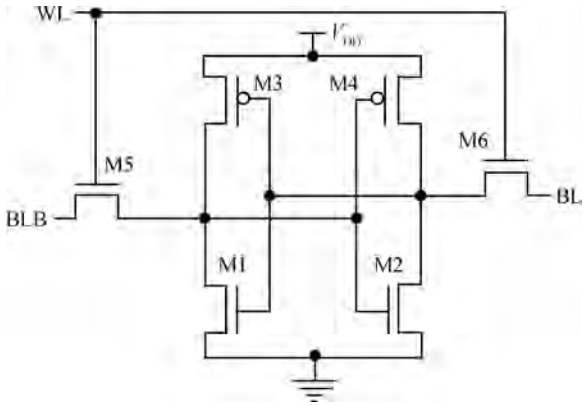

Fig. 1. A conventional 6T-CMOS SRAM cell[4].

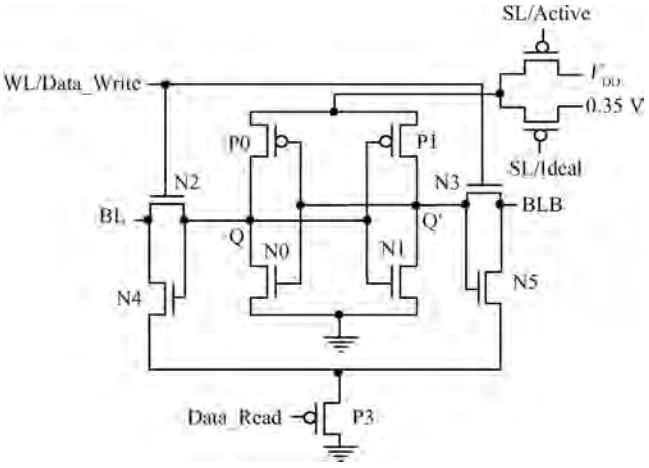

Fig. 2. An IP3 SRAM bit-cell[5].

idle mode. Also, at lower supply voltages data retention is becoming a challenge for memory designers, so it is strongly felt that a new circuit design approach is needed to address these design issues.

2.2. IP3 SRAM cell

The IP3 SRAM cell structure[5] has been proposed to address the overall standby leakage and active read power consumption; see Fig. 2. It uses the drowsy technique and pMOS stacking with ground. A significant reduction in the power (standby and active) has been observed at a performance-area penalty.

The IP3 is an integrated SRAM cell containing two sub-cells (write and read) with independent functionality. It applies the pMOS gated ground and drowsy technique to reduce the active and standby power without losing cell performance. Full-supply body biasing is used to further reduce the sub-threshold leakage when the cell is in standby mode. The data write and memory storage is performed at the upper sub-cell, while the lower sub-cell is used for data-read operation only. In standby mode, the drowsy voltage ($V_{DD} = 0.35$ V) is applied to the memory to retain the data in the upper memory sub-cell at a much reduced power loss. The drowsy voltage can be applied through the on-board power supply or through an external power supply. In the active mode of operation, the cell is

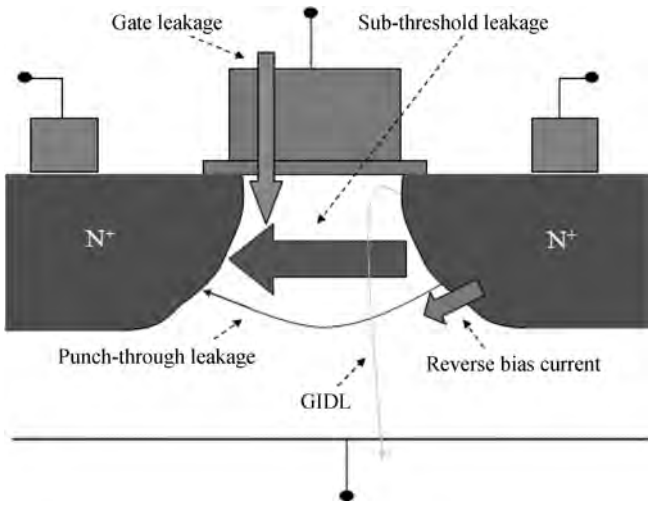

Fig. 3. Leakage current mechanisms of deep-submicron transistors.

supplied with V_{DD}. In the data write mode, the data read sub-cell is completely isolated from the data write sub-cell through BLs and vice-versa, which further improves the cell's stability.

3. Leakage current mechanism

In deep-submicron regimes, leakage currents, e.g. gate direct tunneling leakage, gate leakage, subthreshold leakage, gate induced drain leakage (GIDL), channel punch through leakage and reverse bias currents (see Fig. 3), are the major contributors to the overall power dissipation of CMOS circuits. Here, the subthreshold leakage, GIDL and channel punch through leakage currents are the off state leakage currents, while the reverse bias junction and gate oxide tunneling current appears in both the on and off states.

3.1. Gate direct tunneling leakage

The gate leakage flows from the gate through the "leaky" oxide insulation to the substrate. In oxide layers thicker than 3–4 nm, this kind of current results from the Fowler–Nordheim (FN) tunneling of electrons into the conduction band of the oxide layer under a high applied electric field across the oxide layer. However, for lower oxide thicknesses (which are typically found in 0.15 μm and lower technology nodes), direct tunneling through the silicon oxide layer is the leading effect. The mechanisms for direct tunneling include electron tunneling in the conduction band (ECB), electron tunneling in the valence band, and hole tunneling in the valence band, among which ECB is dominant. The magnitude of the direct gate tunneling current increases exponentially with the gate oxide thickness, t_{ox}, and supply voltage, V_{DD}. In fact, for a relatively thin oxide (of the order 2–3 nm), at a V_{GS} of 1 V, every 0.2 nm reduction in t_{ox} causes a tenfold increase in I_G[6, 7]. Gate leakage increases with temperature at about 2×/100 ℃.

It is the tunneling into and through the gate oxide. The reduction in gate oxide thickness results in an increase in the field across the oxide. The high electric field coupled with the low oxide thickness results in tunneling of electrons from the substrate to the gate, and also from the gate to the substrate, through the gate oxide, resulting in the gate oxide tunneling

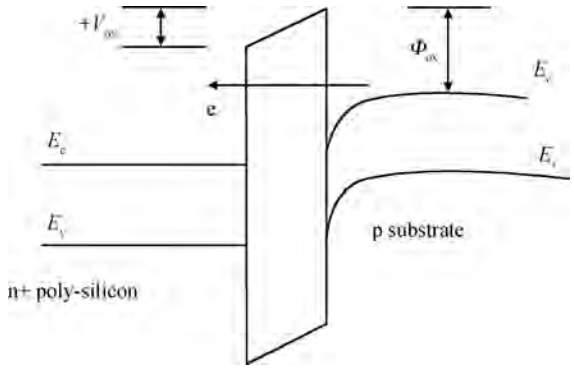

Fig. 4. Direct tunneling of electrons[8].

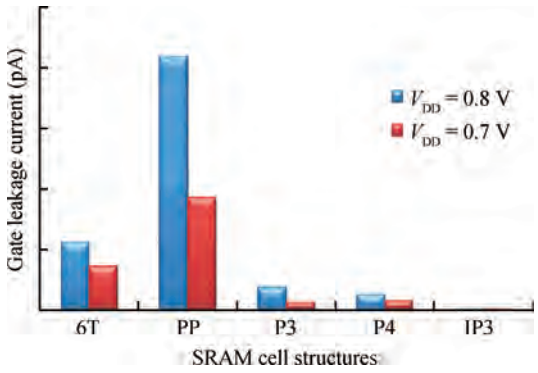

Fig. 5. Gate leakage at $V_{DD} = 0.8$ and 0.7 V.

current. The mechanism of tunneling between the substrate and the gate polysilicon can be primarily divided into two parts, namely the FN tunneling and the direct tunneling. In the case of FN tunneling, electrons tunnel through a triangular potential barrier, whereas in the case of direct tunneling, the electrons tunnel through a trapezoidal potential barrier. The tunneling probability of an electron depends on the thickness of the barrier, the barrier height and the structure of the barrier. Therefore, the tunneling probabilities of a single electron in FN tunneling and direct tunneling are different, resulting in different tunneling currents. In the DSM region, direct tunneling is a major gate oxide tunneling leakage issue.

In very thin oxide layers (less than 3–4 nm), instead of tunneling into the conduction band of SiO_2, electrons from the inverted silicon surface directly tunnel to the gate through the forbidden energy gap of the SiO_2 layer; see Fig. 4. In the case of direct tunneling, electrons tunnel through a trapezoidal potential barrier instead of a triangular potential barrier. Hence, the direct tunneling occurs at $V_{ox} < \Phi_{ox}$. The current density of the direct tunneling[8] is given by Eq. (1).

$$J_{DT} = AE_{ox}^2 \exp\{-B[1-(1-V_{ox}/\Phi_{ox})^{3/2}]/E_{ox}\}, \quad (1)$$

where $A = q^3/16\pi^2\hbar\Phi_{ox}$, $B = 4\sqrt{2m^*}$, $\Phi_{ox}^{3/2}/3\hbar q$, $\hbar$ is the $1/2\pi$ of Plank's constant, Φ_{ox} is the barrier height of the electrons in the conduction band, and E_{ox} is the field across the oxide.

The direct tunneling current is significant for low oxide thicknesses in DSM technology. Clearly, the reduction in gate oxide leakage will directly improve battery life in a battery-powered PDA.

4. A review of the related work

In this section, we will review some of the previously reported SRAM cell structures.

In Ref. [9], a gate leakage current reduction technique based on the pMOS pass-transistor SRAM bit-cell structure as a PP-SRAM cell has been proposed at 45 nm technology and 0.8 V supply voltage. In this cell, in order to decrease the gate leakage currents of the SRAM bit cell, nMOS pass transistors are replaced by pMOS pass transistors. The use of pMOS leads to performance degradation due to the different mobility coefficients for the nMOS and pMOS transistors. To overcome this problem, the width of the pMOS pass transistor is selected as 1.8× that of the nMOS. Thus, it has an area penalty.

In Refs. [10, 11], a P3 SRAM bit-cell structure at 45 nm technology has been proposed for semiconductor memories with high activity factor-based applications in DSM CMOS technology at 45 nm. This has been proposed to reduce the active and standby leakage power through the gate and sub-threshold leakage in the active and standby mode of the memory operation. The stacking transistor pMOS (PM4), connected in series (in line), is kept OFF in standby mode and ON in active (read/write) mode. The pMOS transistors are used to lower the gate leakage current, while a full-supply body-biasing scheme is used to reduce the sub-threshold leakage currents. The P3 SRAM bit-cell had a significant fall in dynamic as well as standby power, in comparison with the conventional 6T SRAM bit cell, at the cost of a small area penalty and issues with SNM.

5. Simulation and results

To analyze the gate leakage currents and standby power in the 6T, PP, P4, P3 and IP3 SRAM cells, a simulation is performed at 45 nm CMOS technology with $t_{ox} = 2.4$ nm at 27 ℃, and a supply voltage of $V_{DD} = 0.8$ and 0.7 V.

5.1. Gate leakage current

The IP3 cell has the lowest gate leakage current. At $V_{DD} = 0.8$ V, a reduction of 98, 99, 92 and 94% is observed in comparison with the 6T, PP, P4 and P3 SRAM cells, respectively, while at $V_{DD} = 0.7$ V, it is 97, 98, 87 and 84%; see Fig. 5.

5.2. Standby and read/write power

Figures 6, 7 and 8 show the total standby leakage, active write and active read power consumption of the 6T, PP, P4, P3 and IP3 designs at 0.8 and 0.7 V, respectively.

At $V_{DD} = 0.8$ V, the IP3 cell has 56% and 68%, and at $V_{DD} = 0.7$ V 44% and 56%, lower standby leakage power in comparison with the conventional 6T and PP cells, respectively, with no performance loss, i.e. no degradation in the SNM, the cell's stability. The standby leakage power consumption is lowest in the P4 and P3 cells at the cost of cell performance, i.e. poor SNM; see Fig. 6.

For the active write power (see Fig. 7) at $V_{DD} = 0.8$ V, the IP3 cell has a lower active write power by 44% and 71%, and at

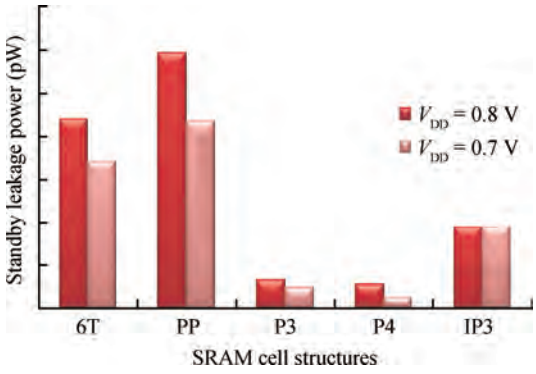

Fig. 6. Standby power comparison at $V_{DD} = 0.8$ and 0.7 V.

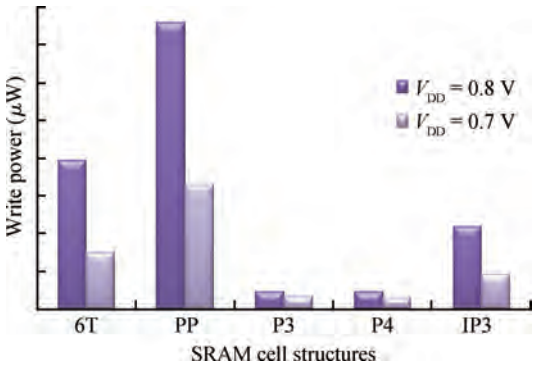

Fig. 7. Active write power at $V_{DD} = 0.8$ and 0.7 V.

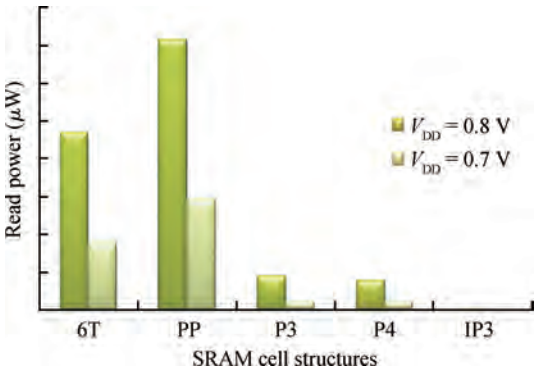

Fig. 8. Active read power at $V_{DD} = 0.8$ and 0.7 V.

$V_{DD} = 0.7$ V, with respect to the 6T and PP cell, respectively, with no loss in cell stability. The active write power consumption is lowest in the P4 and P3 cells but at the cost of poor SNM.

The active read power is lowest in the IP3 cell (see Fig. 8). At $V_{DD} = 0.8$ V, it is 99, 99, 96 and 97% lower in the 6T, PP, P4 and P3 cells, while at $V_{DD} = 0.7$ V, it is 99, 99, 96 and 96%, respectively, with no loss in cell performance.

5.3. Area

In Fig. 9, a relative comparison of the bit-cell areas of the SRAM designs is presented. It is evident that the IP3 cell has a performance-area penalty by 1.8% (P4, P3), 26% (PP) and 47% (6T).

The layout of the IP3 cell is presented in Fig. 10 at 45 nm CMOS technology. This is not the actual size of the layout and is sketched to observe the relative performance-area tradeoff in the presented cells.

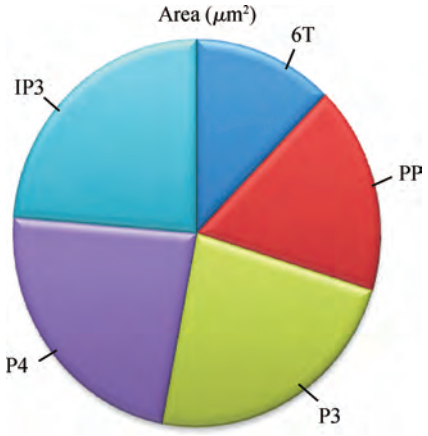

Fig. 9. Relative chip area comparison.

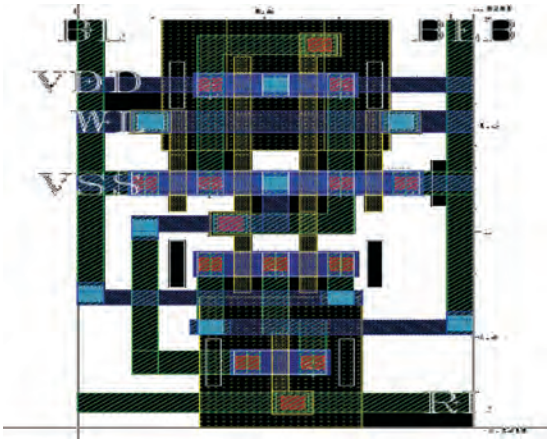

Fig. 10. Layout of the IP3 SRAM bit-cell.

6. Conclusions

In this paper, the gate leakage simulation and analysis of an IP3 SRAM cell was carried out, and the results were compared with conventional 6T, PP, P3 and P4 SRAM cells. It was observed that, at a supply voltage of $V_{DD} = 0.8$ V, a reduction of 98%, 99%, 92% and 94% is observed in gate leakage current in comparison with the 6T, PP, P4 and P3 SRAM cells, respectively, while at $V_{DD} = 0.7$ V, this is 97%, 98%, 87% and 84%. A significant reduction is also observed in the overall standby leakage power by 56%, the active write power by 44% and the active read power by 99%, compared with the conventional 6T SRAM cell at $V_{DD} = 0.8$ V, with no loss in cell stability and performance at a performance-area tradeoff. Therefore, the IP3 SRAM cell has the lowest power consumption with no loss in performance degradation for battery-powered applications, where the power performance is of prime concern.

Acknowledgement

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