Simulation of the sensitive region to SEGR in power MOSFETs

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Abstract: Single event gate rupture (SEGR) is a very important failure mode for power MOSFETs when used in aerospace applications, and the cell regions are widely considered to be the most sensitive to SEGR. However, experimental results show that SEGR can also happen in the gate bus regions. In this paper, we used simulation tools to estimate three structures in power MOSFETs, and found that if certain conditions are met, areas other than cell regions can become sensitive to SEGR. Finally, some proposals are given as to how to reduce SEGR in different regions.

Key words: single event gate rupture; SEGR; heavy ion; power MOSFET
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1. Introduction

Single event gate rupture (SEGR) is a very important failure mode induced by the impacts of heavy ions when power MOSFETs are used in aerospace applications. It is widely accepted that the incident particle creates a dense track of electron–hole pairs, which changes the potential difference between the two sides of the gate oxide, or causes a localized dielectric breakdown of the gate oxide. It is thought that the most sensitive strike location is the center of the neck region[1], while the experimental results show there are different SEGR failure regions in addition to the cell region. Figure 1 illustrates an EMMI picture of a power MOSFET, showing the leakage current points when 20 V is applied between the gate and source. The device was tested with the MIL-STD-750E method 1080 and had passed the condition of $V_{DS} = 50$ V, $V_{GS} = -10$ V and LET $= 98$ MeV·cm^2/mg (Bi^+), but during the post stress test, we found that the device's gate-to-source leakage current had exceeded the specification limits current ($\pm$ 100 nA). As we can see in Fig. 1, the EMMI current points are located in the gate bus regions. This tells us that if certain conditions are met, other regions will be susceptible to SEGR.

In this paper, we use the ISE simulation software to estimate three different structures in power MOSFETs. Utilizing simulation results, we show the responses of different regions to the heavy incident ions, and finally we discover the methods to reduce SEGR in different regions.

2. Simulation structures and conditions

There are two impacts of heavy ions on the gate oxide of power MOSFETs, and they make the gate oxide sensitive to SEGR. On the one hand, the gate oxide breakdown voltage decreases during irradiation exposure in heavy ions[2]. Figure 2 shows the breakdown voltage of a gate oxide with a certain thickness during different heavy ion irradiation. The values are calculated using Eq. (1) given by Ref. [1].

$$V_{CRIT} = E_{BD} T_{OX} \left(1 + \frac{Z}{44}\right)^{-1}. \quad (1)$$

where V_{CRIT} is the lowed oxide breakdown voltage due to ion interaction in the oxide; E_{BD} is the electric breakdown field of intrinsic oxide, and assumed to be 10^7 V/cm for SiO_2; Z is the atomic number of the ion; and T_{OX} is the gate oxide thickness. From Fig. 1, the gate oxide breakdown voltage should decrease during ion strike. This is related to the holes generated in the oxide that stay there during the impact because they are almost immobile, which is different from the electrons whose very high mobility causes their rapid swap out in the presence of the electric field[3]. The holes in the oxide build an inner electric field and decrease the gate oxide breakdown voltage.

On the other hand, a portion of the applied V_{DS} is coupled to the Si–SiO_2 interface beneath the gate oxide during or immediately after ion strike, which increases the voltage between

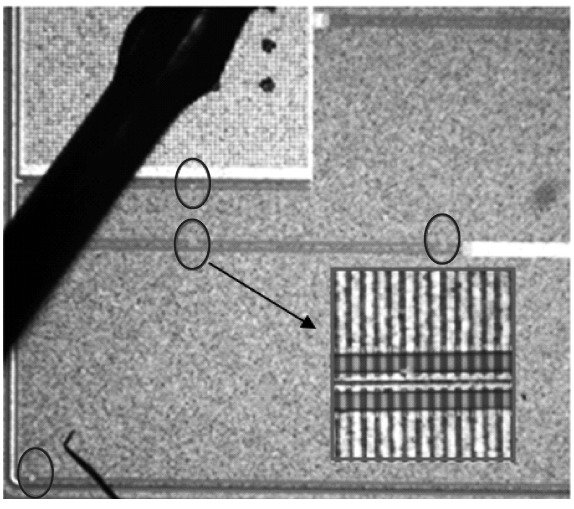

Fig. 1. EMMI picture of a power MOSFET after undergoing Bi^+ strikes.

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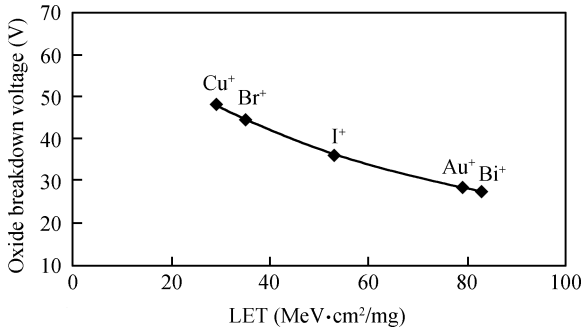

Fig. 2. Oxide breakdown voltage with a certain thickness under typical heavy-ion irradiation.

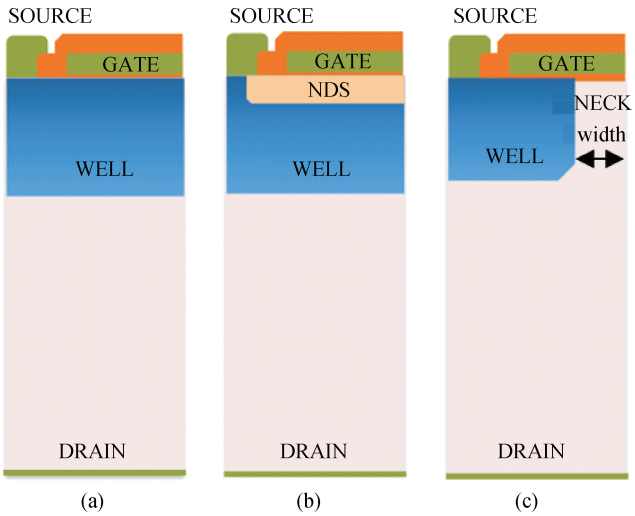

Fig. 3. Cross-sectional view of the simulation structures. (a) Channel region. (b) NDS region. (c) Neck region.

the two sides of the gate oxide. When the gate oxide breakdown voltage has been lowered by incident ions, the device is prone to SEGR.

If we find the potential trend at the Si–SiO_2 interface when exposed to heavy incident ions, we can discover how to reduce SEGR. There are three different doping profiles under the gate oxide, see Fig. 3. We use the three structures to simulate the responses of the different regions to the heavy incident ions.

2.1. The channel region or gate bus region

Two regions exist in the power MOSFET. Where there is only P-type silicon beneath the gate oxide, there are channel regions in the cell and the gate bus region. In the cell region, the channel length is always short and the width is always large, especially in the stripe-shaped cell. For simplification reasons, we remove the influence of the NDS (N type source) and only use the structure of Fig. 3(a) to simulate the impact of boron concentration on the potential at the Si–SiO_2 interface.

2.2. The NDS source region

A parasitic NPN profile exists beneath the gate oxide in some areas, where the gate oxide overlays the NDS. In the radiation-hardened power MOSFET, the non-self-aligned process requires a large overlaid area. If the power MOSFET is designed in a striped-cell style, the area is much larger for the larger width. We use the structure of Fig. 3(b) to simulate the impact of the phosphorus concentration on the potential at the Si–SiO_2 interface.

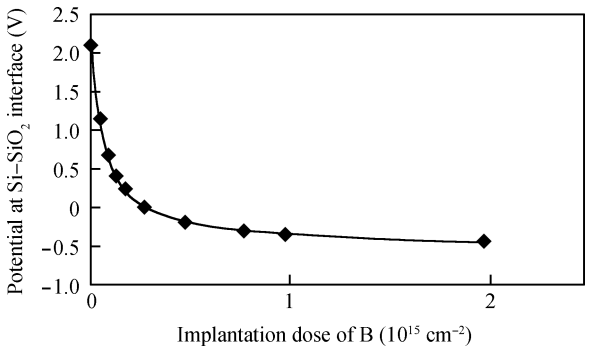

Fig. 4. Impact of the boron implantation dose on the potential at the Si–SiO_2 interface.

2.3. The neck region

The neck region is defined as the area separating the P-WELL regions of the individual cells. We use the structure of Fig. 3(c) to simulate the impact of the neck length on the potential at the Si–SiO_2 interface.

All the structures use the 200 V device epitaxy. The simulations start with DIOS, and all the process flows are the same except the tuning implantation dose and the mask for implantation. The single event effect is simulated with DESSIS, and the LET is set to 1 pC/μm, equal to 98 MeV·cm^2/mg, with a bias conditions of $V_{GS} = -15$ V and $V_{DS} = 50$ V. After the heavy ion penetrates the structure, the potential at the Si–SiO_2 interface is extracted.

3. Simulation results

During the ion strike, large numbers of electrons and hole pairs are generated along its trajectory. The electrons are swept out of the device from the drain, and the holes are swept upward to the Si–SiO_2 interface along the trajectory and deposited there. The holes can flow out from the source and lift the potential of the Si–SiO_2 interface by the distributed resistance along the current path.

3.1. The channel region or gate bus region

The implantation dose of boron is tuned to see the change in potential at the Si–SiO_2 interface. In Fig. 4, the potential decreases with the increase in the implantation dose of boron. This means that the higher the concentration in the WELL, the more stable the device. From Fig. 4, the potential at the Si–SiO_2 interface will greatly increase when the boron implantation dose is lower than 1×10^{14} cm^{-2}, since the distributed resistance will be great in that case. That is why we found the SEGR failure points located at the gate bus region in some of the power MOSFETs. In other words, if the gate bus region is only doped with boron concentration for the channel region, which is generally less than 1×10^{14} cm^{-2} for keeping the

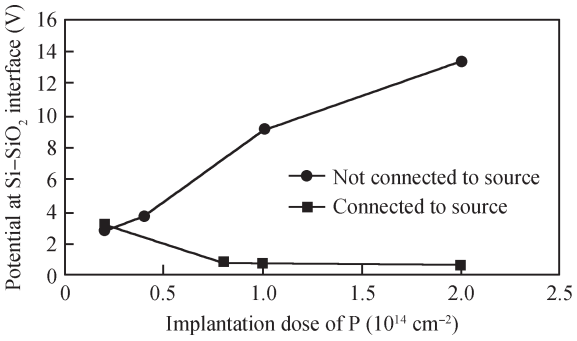

Fig. 5. Impact of the phosphorus implantation dose on the potential at the Si–SiO_2 interface.

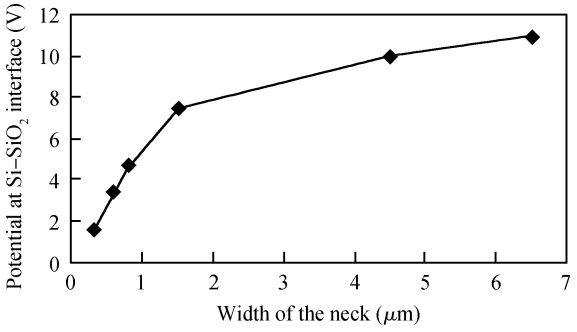

Fig. 6. Impact of the width of the neck on the potential at the Si–SiO_2 interface.

threshold voltage (V_{TH}) at 3 V, the gate bus region will be sensitive to the SEGR.

3.2. The NDS source region

The implantation dose of phosphorus is tuned to see the change in potential at the Si–SiO_2 interface. Figure 5 shows the change in potential. It can be noticed that if the NDS connects to the source, the potential at the Si–SiO_2 interface will decrease with the increase in phosphorus dose. Otherwise, the potential will increase lineally with the phosphorus dose. The main reason for this is that the distributed resistances along the current path of the holes are different in the two cases. In the structure of Fig. 3(b), both the WELL and NDS regions serve as the current path. If the NDS connects to the source, the holes will flow in the NDS region, which is always highly doped. But if the NDS has problems connecting to the source, the holes are forced to flow in the WELL region. The higher the phosphorus concentration, the deeper the NDS junction, and the larger the distributed resistance of the hole current. That is why the Si–SiO_2 potential will increase lineally with the phosphorus dose.

3.3. The neck region

The neck region of the power MOSFET is potentially the most sensitive region to SEGR[4]. The holes induced by heavy ions in this region have more difficulty flowing out of the device. Figure 6 shows the impact of the width of the neck on the potential at the Si–SiO_2 interface. A point in the width of the neck exists, and in this case the point is located at 2 μm. When narrower than 2 μm, the potential at the Si–SiO_2 interface increases with the increase in neck width more rapidly than when it is wider than 2 μm. When narrower than 2 μm, the holes can be swept out of the neck region by the field in the WELL junction. When wider than 2 μm, that effect becomes inferior, and the holes recombine with electrons. With the increase in the width of the neck, the potential will reach a saturation point where no holes can be swept out from the WELL.

4. Discussion

In the previous section, the breakdown voltage of the gate oxide decreases and the electric field increases in the dielectric due to increasing potential at the Si–SiO_2 interface induced by heavy ion strike. From our experiments, we found that failure points are located at the gate bus regions after B^+ strikes, and by our knowledge, there are no other reports of this in previous research. The simulation results presented in the previous section indicate that there are three different profiles beneath the gate oxide in the power MOSFET, and all those have a chance of SEGR. For example, if the gate bus region is only doped with boron of less than 1×10^{14} cm^{-2}, the potential at the Si–SiO_2 interface coupled from V_{DS} by incident ions can become greater than 2 V, which can be larger than the NDS or neck regions, and SEGR will happen primarily at the gate bus region. From the simulation results, we can get some methods to reduce SEGR in the three different regions.

(1) In the gate bus region, the boron concentration should be large, and can be increased by adding an additional high-dose boron implantation. In the channel region, in order to increase the boron concentration and keep the threshold voltage (V_{TH}) unchanged, the gate oxide thickness should be reduced. It is good to get lower potential voltage at the Si–SiO_2 interface and lower threshold voltage shifts under total ionization dose irradiation. However, the breakdown voltage of the dielectric oxide will reduce with a decrease in thickness, so a tradeoff must be made.

(2) In the NDS region, a good connection from the NDS to the source must be guaranteed. In radiation hardened power MOSFETs, the NDS resistance is always made larger to reduce the occurrence of single event burnout failure[5, 6], so the WELL should be doped higher and deeper, which can reduce the distributed resistance along the holes' current path.

(3) In the neck region, it is good to make the neck width shorter, and another method is to make the WELL junction as deep as possible, which can increase the chances of sweeping the holes induced by heavy ions out of the neck regions. Besides, a deeper WELL junction is good for reducing the occurrence of SEGR at the NDS region.

5. Conclusion

Heavy incident ions can couple the V_{DS} voltage to the Si–SiO_2 interface, and so increase the potential. In other words, heavy ions can increase the electric field in gate oxides, and in the worst case destroy the gate oxide. In this paper, the experimental and simulation results all show that SEGR can happen in regions other than the cell regions in power MOSFETs, if certain conditions are met. At the end of the paper, some suggestive methods are given to reduce the occurrence of SEGR.

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