

# A SiGe BiCMOS multi-band tuner for mobile TV applications

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**Abstract:** This paper presents the circuit design and measured performance of a multi-band tuner for mobile TV applications. The tuner RFIC is composed of a wideband front-end, an analog baseband, a full integrated fractional- $N$  synthesizer and an I<sup>2</sup>C digital interface. To meet the stringent adjacent channel rejection (ACR) requirements of mobile TV standards while keeping low power consumption and low cost, direct conversion architecture with a local AGC scheme is adopted in this design. Eighth-order elliptic active-RC filters with large stop band attenuation and a sharp transition band are chosen as the channel select filter to further improve the ACR preference. The chip is fabricated in a 0.35- $\mu\text{m}$  SiGe BiCMOS technology and occupies a silicon area of 5.5 mm<sup>2</sup>. It draws 50 mA current from a 3.0 V power supply. In CMMB application, it achieves a sensitivity of -97 dBm with 1/2 coding QPSK signal input and over 40 dB ACR.

**Key words:** tuner; multi-band; automatic gain control; adjacent channel rejection; SiGe BiCMOS

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## 1. Introduction

In recent years, digital mobile TV has become more and more popular all over the world for its convenience. As a result, a variety of terrestrial and satellite standards are emerging worldwide, such as DVB-T/H in Europe, T-DMB in South Korea and CMMB in China. The tuners aimed at these standards have many common characteristics, except for some slight differences, such as RF band, channel spacing and channel bandwidths. In order to realize a low-cost, low-power and small physical size tuner to meet the stringent market requirements, this paper presents the implementation of such a radio tuner using a 0.35  $\mu\text{m}$  SiGe BiCMOS process. It supports mobile TV applications in VHF III and UHF bands, which most terrestrial-based standards use to deliver TV programs. The chip occupies 5.5 mm<sup>2</sup> silicon area and consumes about 150 mW from a 3.0 V power supply. It should be noted that since many mobile TV standards use time-slicing operation, the average power consumption could be much lower than the peak power. In addition, special care must be paid in designing blocks such as DC offset cancellation (DCOC) or PLL. They should setup quickly when the tuner restarts and not disturb the time-slicing operation.

This paper mainly focuses on the improvement of the ACR performance. We describe the challenges related to mobile TV specifications and provide an overview of the selected architecture.

## 2. Challenges and the selected architecture

A broadcast TV tuner supporting the VHF III and UHF bands should cover a frequency range from 170 to 862 MHz. The biggest challenge is to achieve a good sensitivity over

the whole band while preventing the tuner from interference. Interference partly stems from in-band channels and partly from out-band signals, such as the 900 MHz GSM band. This problem typically can be solved by using external RF tracking filters or “up-down” conversion super-heterodyne architecture. Such solutions tend to be bulky or power-hungry, which make them unsuitable for mobile TV. Since most mobile TV standards use only a portion of the broadcast TV band, for example the VHF III (171–245 MHz) and the UHF bands (470–862 MHz), in each band the upper frequency is less than twice of the lower frequency. Thus the harmonic rejection requirements are not too severe, and multiple RF front-ends with direct conversion architecture become a practical, low-cost, low-power and flexible alternative.

Figure 1 shows the block diagram of the receiver. Two antennas are used to cover the VHF III band and the UHF band, and are followed by band-pass RF filters to filter out interference (e.g. 900 MHz GSM band) and relax the harmonics rejection requirement. Two low-noise amplifiers (LNAs), which are optimized for the UHF band and the VHF III band separately, amplify the RF signal and send it to the same digitally controlled variable gain amplifier (VGA). A quadrature mixer then converts the RF signal directly to baseband signal. The analog baseband path consists of two channel select filters, two baseband VGAs and an on-chip DC offset cancellation circuit. To meet the stringent adjacent channel rejection (ACR) specifications, for example, CMMB requires 37 dB  $N-1/N+1$  digital ACR and 42/43 dB  $N-1/N+1$  analog ACR, 8th order op-amp-RC elliptic low-pass filters are used as channel select filters and a well designed automatic gain control (AGC) strategy is adopted. A fractional- $N$  synthesizer is used for LO generation. This allows a wide range in selecting the external crystal reference, which ultimately can be shared with other applications

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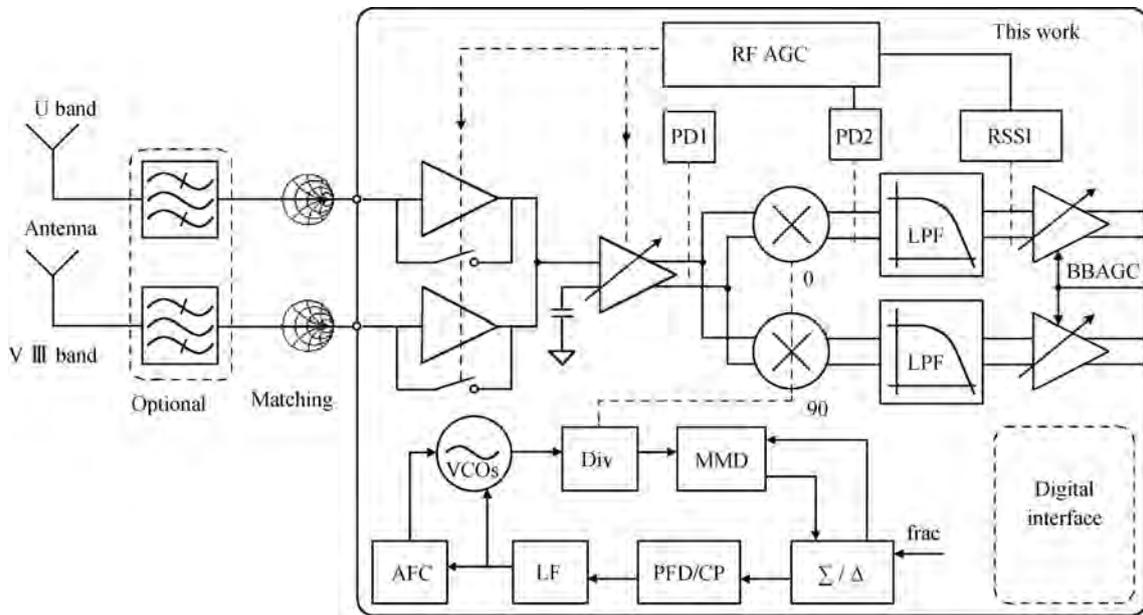


Fig. 1. System block diagram of the tuner.

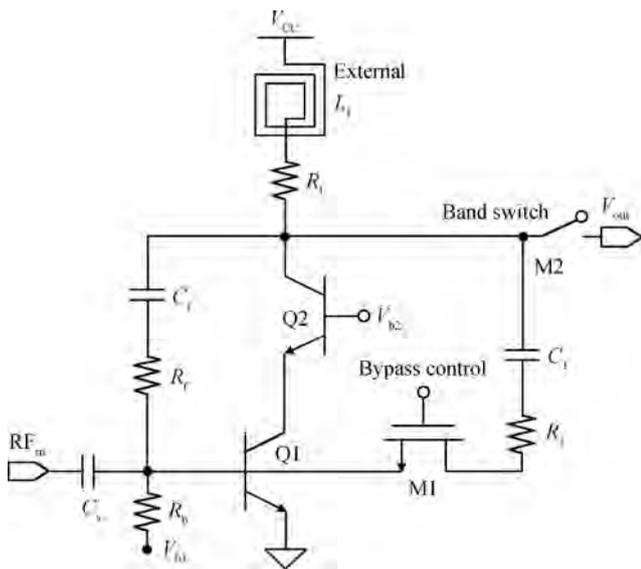


Fig. 2. Simplified schematic of wideband LNA.

to save cost, while maintaining a fine frequency step.

### 3. Circuit description

#### 3.1. LNA and mixer

The LNAs optimized for the UHF and VHF III bands are implemented with similar topology, as depicted in Fig. 2. The cascode structure with resistive shunt feedback is chosen to achieve good reverse isolation and broadband matching. A LNA bypass branch, consisting of M1, C1 and R1, provides a low gain path when the input signal is really huge. The external inductor L1, together with a bond wire inductor, is used to boost the gain at high frequencies and equalize the power gain of the LNA to a constant value. Transistor M2 acts as a switch for U/V band LNA selection.

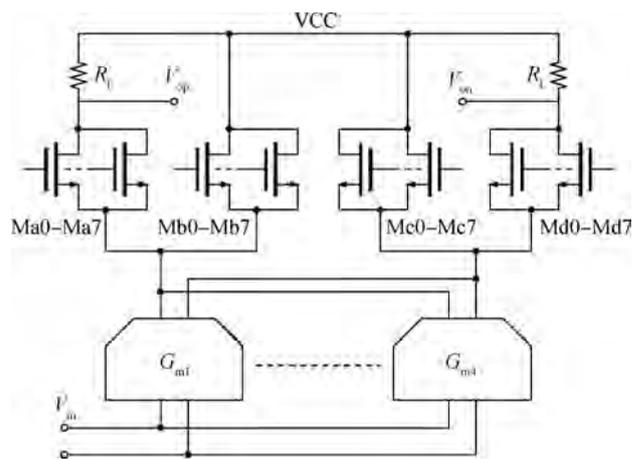


Fig. 3. Simplified schematic of RF PGA.

The quadrature mixer is formed by two Gilbert mixers with shared transconductor stages, which improves the image rejection ratio (IRR) by reducing phase error. Since linearity is of great concern, more current is biased at the transconductor stage. Resistive degeneration is also used to further improve the linearity of the mixer. The switching quad transistors are sized so that they operate close to their peak  $f_T$ .

#### 3.2. RF PGA and BB VGA

As shown in Fig. 3, the RF PGA is composed of four  $G_m$  cells and four groups of N-type MOSFETs to steer current<sup>[1]</sup>.  $G_m$  cells with different gains are used for coarse tuning and the MOSFETs perform fine tuning. The MOSFETs are programmed by using an 8-bit thermometer-code binary control to get a monotonous characteristic regardless of temperature and process variations. The MOSFETs pairs Max and Mbx ( $x = 0$  to 7) are sized to obtain a gain step of 1.6 dB. In each pair, two transistors have the same size and driven by two opposite

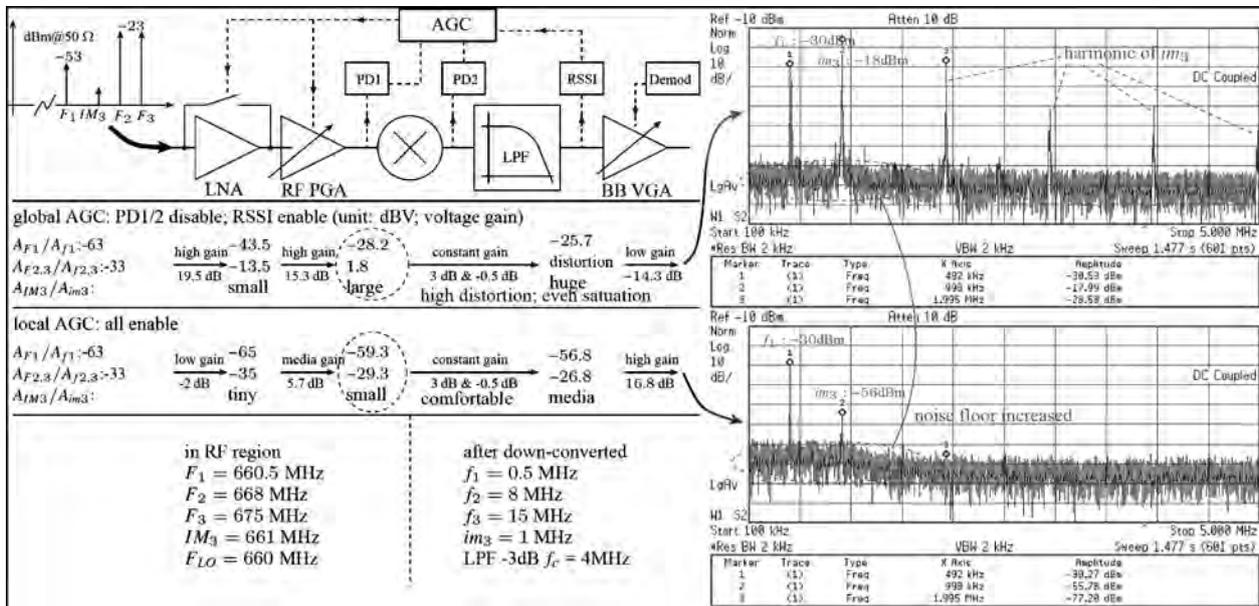


Fig. 4. Comparison of the two AGC schemes.

digital control signals. The whole RF PGA achieves 51.2 dB gain tuning range.

A current steering type VGA is chosen as the BB VGA for its excellent linear gain in dB characteristic over a wide dynamic range. A temperature compensation and dB linearization circuit is used to widen the linear-in-dB gain control range and prevent the VGA gain characteristic from changing over PVT variations. The BB VGA is controlled by a voltage from the demodulator IC, which allows the output level to be adjusted to fulfill the requirement of the demodulator ADC.

### 3.3. Automatic gain control

In terrestrial applications, the tuner not only needs to receive a signal with a wide range of power, but also must be able to handle a few high power blockers interferers. In addition, the signals can be affected by very deep fading. Thus an automatic gain control scheme is important to maintain a tuner with acceptable performance in all kinds of conditions.

Conventional tuners use a global AGC scheme, which only detects a desired signal power at baseband. If there is a lower noise figure, a higher sensitivity is desired. The frontend block is usually designed with large gain as indicated by the Friis equation ( $N_{F_{sys}} = NF_1 + (NF_2 - 1)/G_1 + (NF_3 - 1)/G_1 G_2 + \dots$ ). When strong interference occurs, the large frontend gain tends to cause a great deal of distortion or even saturation, which degrades the system SNR severely. Another solution is to use most of the receiver's dynamic range for the blockers while keeping the signal at a low level. The drawback of this approach is that the receiver output SNR stays constant regardless of the RF input signal level because the AGC level is set only by the desired signal, and sufficient headroom is reserved for blockers whether blockers are present or not<sup>[2]</sup>. This will inevitably limit the sensitivity of the tuner.

In this paper, a local AGC scheme is used so that the RF front-end and baseband gains are independently controlled to maximize their dynamic ranges. A discrete gain control loop

with over 70 dB range is realized in the RF front-end and a continuous gain control scheme with about 40 dB range is in baseband. In order to prevent each stage of the receiver from saturation by strong blockers, a wideband RF power detector and an internal received signal strength indicator (RSSI) are used to control the LNA and the RF PGA and guarantee a constant power at the input of the channel select filters. The desired channel power variations are compensated in the BB VGA. The combination of RF PGA and BB VGA allows the best gain configuration for all receive conditions, because each gain stage in the chain reacts to the power in the bandwidth of interest. The RF AGC is optimized for the best noise figure in the different loading scenarios, while the BB AGC maximizes the ADC loading.

An experiment is used to compare the effects of those two AGC schemes. A global AGC scheme is emulated by disabling PD1, PD2, and using only the RSSI signal to adjust the gains of each stage. As a result, it cannot detect the interference out of the desired channel. A sine wave located at 660.5 MHz is chosen as the signal ( $F_1$ ). Two interferences ( $F_2, F_3$ ) with frequency of 668 MHz and 675 MHz are located out of channel, but one of their 3rd-order inter-modulation ( $IM_3$ ) components is located in the channel. After the mixer, the desired signal, the interferences and the  $IM_3$  component are down converted to 0.5 MHz ( $f_1$ ), 8/15 MHz ( $f_2, f_3$ ) and 1 MHz ( $im_3$ ), respectively. In conditions of two AGC schemes, we keep the desired output signal ( $f_1$ ) with the same magnitude and measure the  $IM_3$  components. Since the BB VGA needs to drive a spectral analyzer with 50  $\Omega$  impedance instead of high demodulator impedance, a relatively low output level (-30 dBm) is chosen so that the BB VGA does not overload and influence the test results. As shown in Fig. 4, in global AGC scheme mode, the LNA, RF PGA and BB VGA are set to high gain, high gain and low gain, respectively; while in local AGC scheme mode, they are set to low gain, media gain and high gain, respectively. The output levels of each stage are calculated without considering the distortion and gain compression. The final output spectral

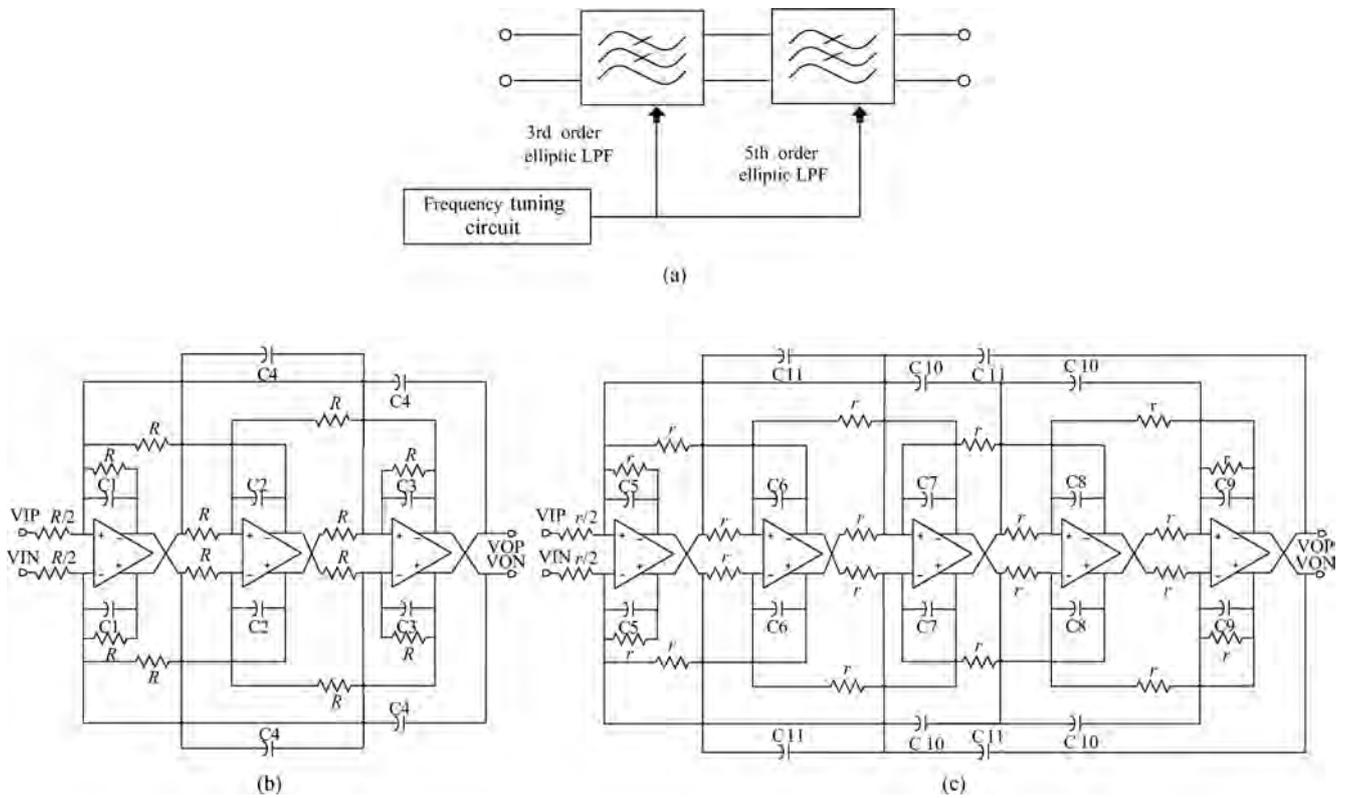


Fig. 5. (a) Filter architecture and the schematic of (b) the 3rd order and (c) the 5th order LPF.

shows that the  $IM_3$  in local AGC scheme mode is 38 dB smaller than that in global AGC scheme mode, though as a penalty, the latter has a lower noise floor. Another ACR test also proves that the former is about 10 dB better than the latter.

### 3.4. Channel select filter

To fulfill the stringent ACR requirements, the channel select low-pass filter (LPF) utilizes an 8th order elliptic prototype and an active-RC topology which features high linearity and a wide dynamic range in comparison with its  $G_m-C$  counterparts due to the closed-loop configuration.

As shown in Fig. 5(a), the overall LPF comprises the 3rd order first filter (Fig. 5(b)) and the 5th order second filter (Fig. 5(c)), both filters share the same automatic frequency tuning circuit. As the first filter reduces adjacent channel interferers in advance, the second filter can have looser linearity and selectivity specifications. Also, the two cascaded filter topology can lower the GBW requirements of the op-amps while achieving a sharp transition band and large stop-band attenuation at twice the filter corner frequency. Moreover, the power dissipation of the two filters can be optimized respectively. The LPF uses 4 bits capacitor banks with their digital control words automatically tuned by a frequency tuning circuit as described in Ref. [3].

The large stop-band attenuation and sharp transition band specification of the LPF indicates that a high  $Q$  filter prototype should be adopted. Since the LPF quality factor is inversely proportional to the op-amp GBW, an op-amp with an extended GBW is used instead of conventional two-stage Miller op-amp.

### 3.5. DC offset cancellation circuit

To prevent the baseband signal path from saturation due to DC offsets in a direct conversion receiver, a DC offset cancellation circuit is applied. It is implemented by a low-pass filter placed in the feedback path, which causes high-pass filtering in the overall closed loop. To keep the cut-off frequency of the DCOC loop constant, a transconductor stage with its gain inversely proportional to the gain of baseband VGA is introduced. The DCOC loop should keep the high-pass corner frequency low enough to leave the in-band signal intact. Thus, small capacitors (usually less than 100 pF) and a large resistive value provided by transconductors with long channel compound MOSFET transistors are desired when considering the monolithic integration.

### 3.6. Synthesizer

A multi-standard fractional- $N$  PLL that covers a frequency band from 170 to 862 MHz with low phase noise is implemented in this design. To extend the frequency range while keeping small  $K_{VCO}$ , a digital split-tuned LC-VCOs architecture is adopted. The concept is to coarsely tune the VCO with bank of switched capacitors, while finely tuning it with varactors. An adaptive frequency calibration (AFC) mechanism is adopted to compensate the process, voltage and temperature (PVT) variations. A hybrid multi-modulus divider (MMD) consisting of current mode logics (CML) and CMOS dividers is proposed along with an integrated  $\Sigma\Delta$  modulator for noise shaping. A fast settling low dropout regulator (LDO) protects the supply line by suppressing in-band random noise caused by the fractional- $N$  operation. To increase the loop in-band perfor-

Table 1. Summary of the performance and comparison with other works.

Parameter	Condition	This work (Spec. *)	Ref. [5]**
Technology		0.35 $\mu\text{m}$ BiCMOS	65 nm CMOS
Power supply (V)		3.0	1.8/1.2
Current (mA)		50	NA
Frequency (MHz)		171–245; 470–862	470–798; S-band
Sensitivity (dBm)	CMMB QPSK 1/2	< -97 (-95)	-99.8
	CMMB 16QAM 1/2	< -92 (-90)	-94
Max. input (dBm)		> 0 (-10)	NA
ACR (dB)	S1: analog interference	-44/-46 (-42/-43)	-45/-46
	S2: digital interference	-40 (-37)	-41

\* CMMB specification. \*\* UHF band results are used.

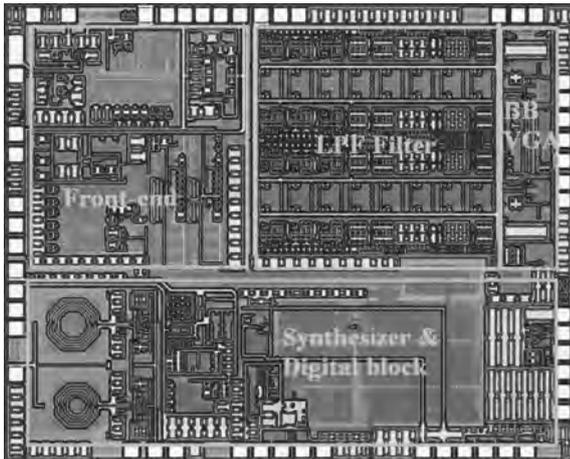


Fig. 6. Die photograph of the chip.

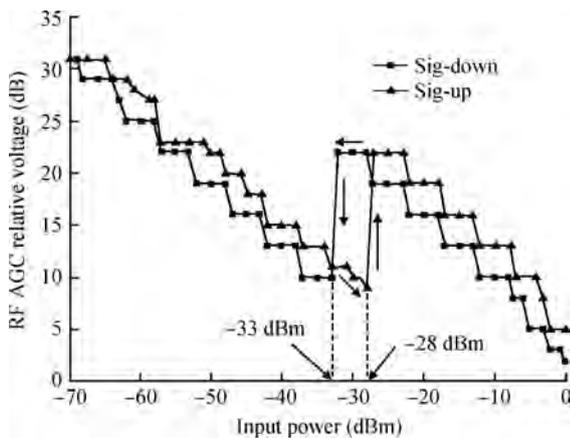


Fig. 7. Measured relative voltage gain of RF AGC versus input power.

mance, a fast reset phase frequency detector (PFD) is employed along with the current programmable charge pump (CP) which can be used to optimize the loop bandwidth to achieve fast settling and low phase noise<sup>[4]</sup>.

#### 4. Measurement results

The die photograph of the prototype chip is shown in Fig. 6. It has been fabricated in a 0.35- $\mu\text{m}$  SiGe BiCMOS process. It features four metal layers, a 43 GHz  $f_T$  high performance NPN transistor and dual metal-insulator-metal (MIM)

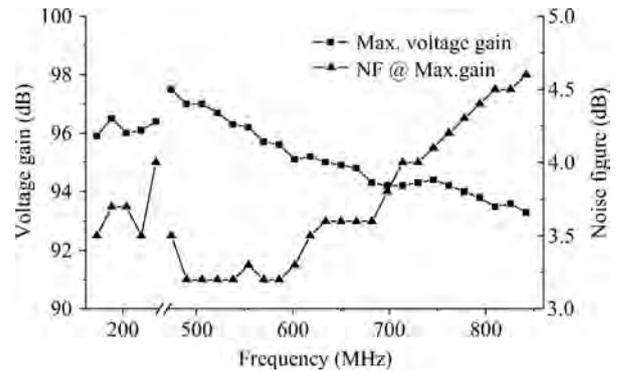


Fig. 8. Measured NF versus maximum gain over the two bands.

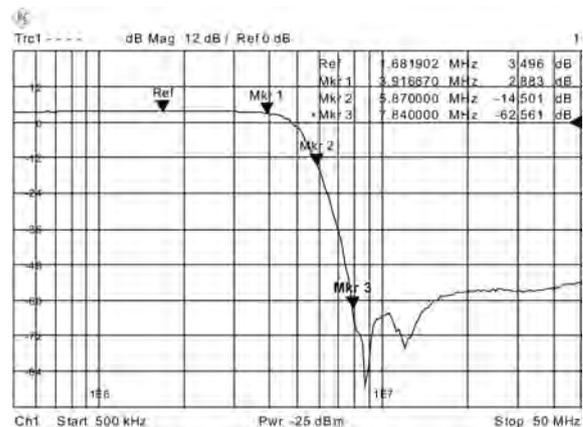
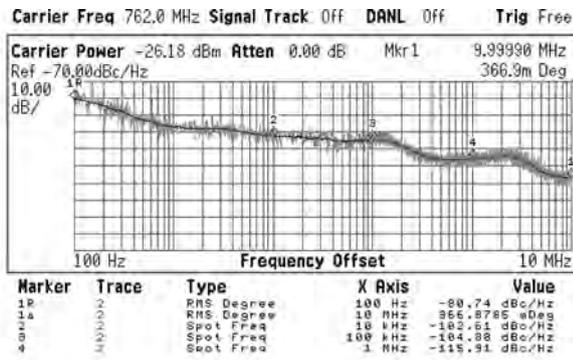


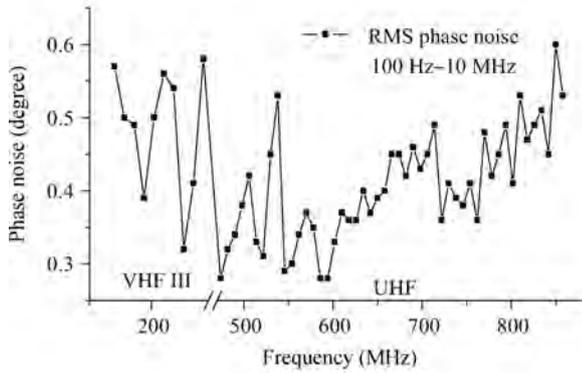
Fig. 9. Measured frequency response of the baseband filter.

capacitors (4.1  $\text{fF}/\mu\text{m}^2$ ). The whole chip occupies a silicon area of 5.5  $\text{mm}^2$  and consumes 50 mA current from a 3 V power supply. Typical system measurement results are summarized in Table 1.

Figure 7 plots the relative voltage gain of LNA and RF PGA varies with the input power. The RF PGA has a dynamic gain range of approximately 50 dB and the LNA provides another 20 dB, which makes the whole RF AGC achieve more than 70 dB dynamic gain range. A hysteric characteristic is introduced to keep the system stable. Figure 8 shows the noise figure over the whole two bands in maximum gain conditions. In all bands, NF is less than 5 dB, which is also verified by system sensitivity measurements. The frequency response of the proposed baseband 8th order elliptic LPF is shown in Fig. 9.



(a)



(b)

Fig. 10. (a) Measured phase noise at 762 MHz and (b) RMS phase noise of the two bands.

The proposed LPF with its corner frequency  $f_c$  set at 4MHz demonstrates a sharp transition band and features a  $2f_c$  stop-band attenuation of 66 dB. Figure 10 gives the measured phase noise at LO frequency of 762 MHz. It achieves  $-102.6$  dBc/Hz at 10 kHz offset,  $-115.9$  dBc/Hz at 1 MHz offset and 0.37 degree RMS phase noise integrated from 100 Hz to 10 MHz. The whole band RMS phase noise performance is also shown in this figure.

As shown in Fig. 11, a complete CMMB receiving platform is setup to play TV programs, which includes an antenna, a tuner, a baseband demodulator/decoder and software. The tuner receives local CMMB RF signal at carrier frequency of 762 MHz from the antenna, down converts it to baseband I/Q signal and then sends it to demodulator. It is controlled by a PC

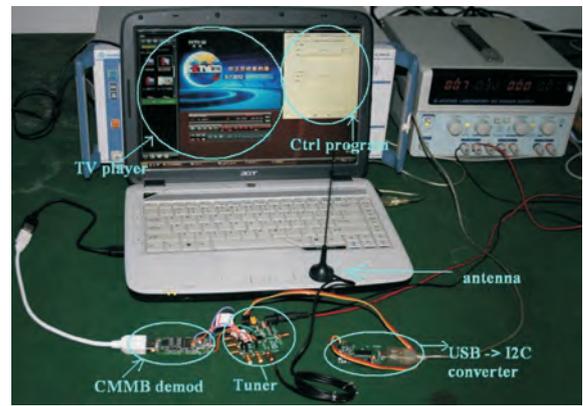


Fig. 11. Mobile TV tuner used in CMMB application.

program through a USB-to-I<sup>2</sup>C converter.

### 5. Conclusion

This paper presents the circuit design and measured performance of a multi-band tuner for mobile TV applications. It adopts a local AGC scheme and 8th order elliptic active-RC filters to meet the stringent adjacent channel rejection requirements. In CMMB application, the measurement results show that the tuner achieves  $-44/-46$  dB S1 ACR and  $-40$  dB S2 ACR performance.

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