ESD protection design for the gate oxide of an RF-LDMOS

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Abstract: This paper presents the investigation of integrated electro-static discharge (ESD) protection design for the gate oxide of an RF-LDMOS (radio frequency lateral double diffusion MOS). Through a comprehensive discussion of experimental and simulated results, a cascoded NMOS is presented as appropriate integrated gate oxide ESD protection with a high holding voltage and a flexible ESD design window.

Key words: cascoded NMOS; ESD; high voltage technology; radio frequency lateral double diffusion MOS; BV engineering implant

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1. Introduction

With the development of microelectronic technologies, ESD (electro-static discharge) protection becomes an important issue for electronic devices. Because ESD is an inevitable event during fabrication, packaging, testing, and assembly, ESD protection design is necessary for the reliability of a device. As a power amplifier, the RF-LDMOS (radio frequency lateral double diffusion MOS) is exciting due to its high voltage capability, low cost and high integration level. However, it is damaged easily once the ESD voltage overstresses the gate oxide[1]. Hence, integrated ESD protection is necessary for RF-LDMOS. This paper investigates the integrated ESD protection in HV (high voltage) technology and reveals experimental results measured using a TLP (transmission-line-pulse) test system. The results are discussed using two-dimensional device simulations. To meet the requirements of the ESD design window and high holding voltage, a cascoded NMOS is demonstrated and adopted as the appropriate integrated ESD protection for the gate oxide of an RF-LDMOS.

Figure 1 illustrates the structure of the RF-LDMOS. $V_{\rm th}$ diffusion regulates the threshold voltage of the RF-LDMOS. Its gate oxide is too vulnerable once an ESD event takes place[1]. The drift region between the gate and N^+ drain is designed to support high breakdown voltages, low on-state resistance and good hot carrier injection reliability[2]. A P^+ sinker connects the bottom side to the N^+ source through a P^+ sinker and metal.

Integrated ESD protection at the gate terminal is necessary for a three-pad RF-LDMOS in order to achieve full-chip protection. As shown in Fig. 2, positive or negative charge that accumulates at the input/output/GND terminals forms the forward or backward current $I_1/I_2/I_3$. Because of its 45 mm channel width and a parasitic diode, the RF-LDMOS protects itself against forward and backward current I_2/I_3 damage effectively. To prevent the RF-LDMOS from ESD events at each two pads, an appropriate gate terminal ESD protection must be integrated, as Figure 2 shows.

2. Investigations of ESD protection design in HV technology

As power ICs, both the RF-LDMOS and its integrated ESD protection were manufactured in an HV process flow. ESD protection design in HV technology is challenging due to its desired high holding voltage and narrow ESD design window. As a widely used ESD protection device, the SCR

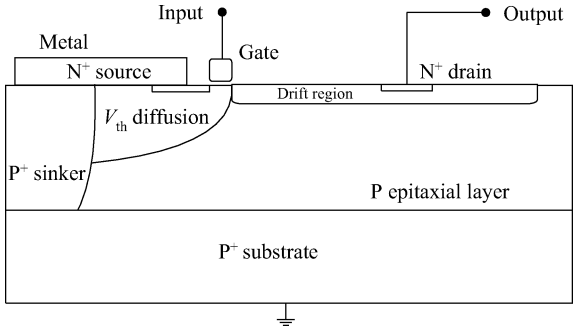

Fig. 1. Cross-section of the RF-LDMOS structure.

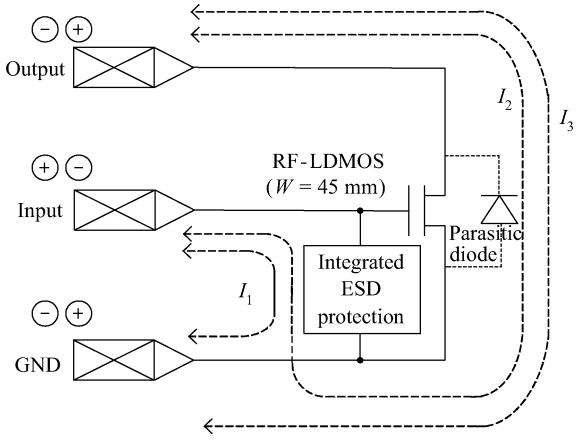

Fig. 2. Full-chip protection against ESD damage for RF-LDMOS.

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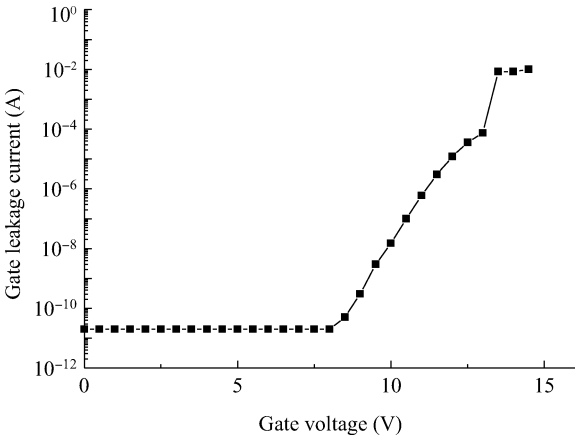


Fig. 3. Applied gate voltage versus gate leakage current of the RF-LDMOS's gate oxide manufactured in an HV process.

(silicon controlled rectifier) displays excellent properties, such as high robustness, fast speed and low parasitic capacitance. However, this device's gate voltage sweeps from –0.5 to 6 V during operation, while the holding voltage (V_{hold}) of an intrinsic SCR pines at only around 1.2 V[3]. This means that an SCR is not suitable as ESD protection for the gate-oxide of an RF-LDMOS because of its high latch up susceptibility. Compared to SCR, a parasitic BJT in MOS is a better choice because of its tunable design window and high V_{hold}. Considering that the robustness of MOS qualities are eliminated by introducing the HV process flow[4], the influences of device parameters are investigated in order to improve the ESD robustness of this device. The gate oxide breakdown voltage and breakdown voltage (BV) engineering implant have been practically experimented on fabricated test chips in an HV diffusion process flow in order to achieve the desired ESD design window.

2.1. Gate oxide breakdown

In Fig. 3, the I–V characteristics applied from gate to source show the gate oxide behavior under gate voltage (V_g) stresses. With V_g raising over 9 V, the gate leakage current increases sharply, indicating latent damage in the gate oxide. When the applied V_g increases over 15 V, clear damage is apparent. According to the rule that ESD protection must turn on when an ESD event takes place and be transparent during normal operation, the desired ESD design window ranges from 6 V (the maximum RF-LDMOS signal) and 9 V for appropriate integrated ESD protection.

2.2. Breakdown voltage (BV) engineering implant

To prevent the gate oxide from ESD damage, a solution-defined BV engineering implant was adopted to trigger parasitic BJT early. The BV engineering implant, which is the V_{th} diffusion in Fig. 1, is illustrated as the dashed line in Fig. 4. It did not cost any more.

The drain to source junction breakdown BV_{DS} determines the triggering of lateral parasitic BJT. At room temperature condition it follows:

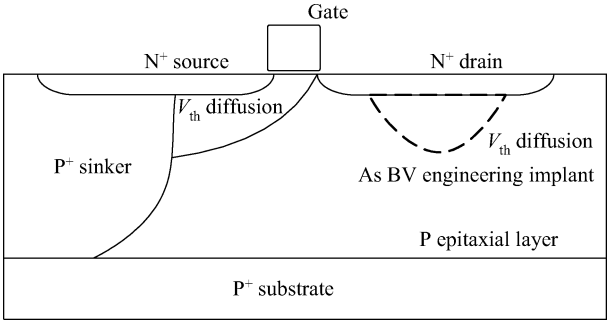


Fig. 4. Schematic of the BV engineering implant.

Table 1. Experimental results of the BV engineering implant.

Length	Implant	IM	BV_{DS}
3.0	Without_implant	–	9.3
1.2	Without_implant	–	9.2
0.6	Without_implant	–	8.7
0.6	With_implant	5	6.6
0.6	With_implant	3	6.4
0.6	With_implant	2	6.5

$$BV_{DS} = \frac{\varepsilon_s E_m^2}{2qN}, \quad (1)$$

where ε_s, q and E_m are silicon dielectric constant, unit charge and the maximum electric field when breakdown occurs, respectively, which is approximately a fixed value[6]. N is the boron doping concentration in the nearby drain region.

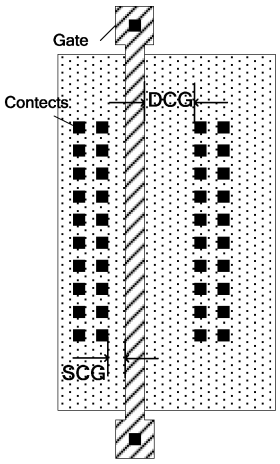
IM is the space from the gate to the implant. An appropriate doping concentration implant into the drain causes the BV_{DS} to fall off, as shown in Table 1. Furthermore, considering the punch-through effect, gate length and implant position variation affects the BV_{DS} slightly.

2.3. DCG (drain contact to gate) and SCG (source contact to gate) effects

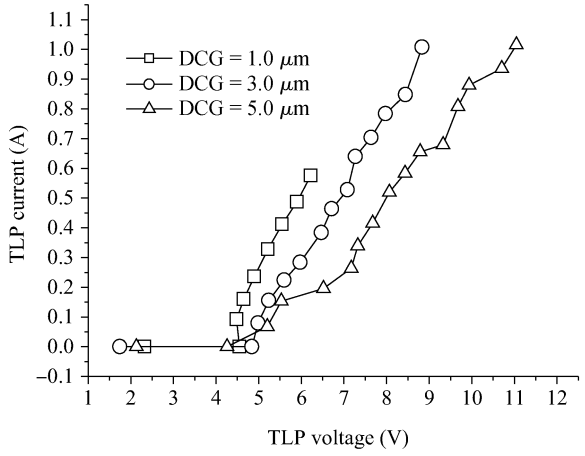
DCG (drain contact to gate) and SCG (source contact to gate) are the clearance from the poly-gate edge to the drain contact and source contact, respectively, as shown in Fig. 5(a), respectively. For an MOS manufactured in an HV process, during parasitic BJT operation hot carriers can be injected into the SiO_2 material and trapped there easily. It causes uniform conduction throughout the whole fingers[4]. An adequate DCG removes the hot spots which spread into the drain contact regions effectively. In the investigation, DCG varied from 1 to 5 μm, and caused a second breakdown (or, thermal breakdown) current. I_{t2} significantly improved from 0.58 to 1.07 A, as shown in Fig. 5(b). In addition, Figure 5(c) shows the small effect of SCG variation from 1 to 5 μm on ESD protection robustness because the hot spot generated at the drain junction only faces the channel.

2.4. Channel length effects

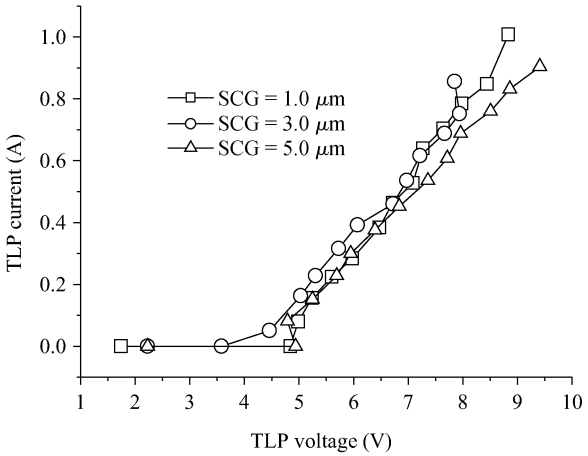
In HV technology, diffusion process flow introduces a non-uniform MOS channel. In addition, a lightly doped epitaxial layer introduces a wide range of variable current gain



(a)



(b)



(c)

Fig. 5. (a) DCG/SCG clearance in NMOS layout and TLP IV characteristics with (b) DCG and (c) SCG variations.

and a high base resistance of parasitic BJT. Thus TLP characteristics strongly depend on channel length (L_g), as shown in Fig. 6. There are two phenomena worth consideration. Firstly, according to[7]

$$V_{\text{hold}} = \frac{V_{\text{DB}}}{k2^{1/n}} \left(\frac{L}{L_{\text{diff}}} \right)^{2/n}, \qquad (2)$$

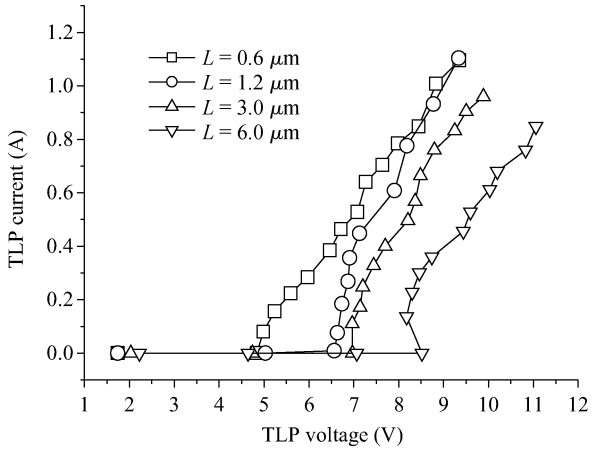


Fig. 6. TLP IV characteristics with channel length variations.

the V_{hold} becomes higher with a longer channel length L. L_{diff} is the electron diffusion length in P-type substrate, k and n are empirical constants. In the experiments, the V_{hold} increased from 4.5 to 8 V when the length varied from 0.6 to 6 μm. Secondly, the robustness level of longer L device was lower in experimental investigations. The I_{t2} with a minimum gate length of 0.6 μm was 1.07 A, whereas that of 6 μm gate length was only 0.85 A. To achieve high V_{hold} without a reduction of robustness, several NMOS were stacked together as integrated ESD protection for the RF-LDMOS in the next section.

3. Configuration of the cascoded NMOS

According to aforementioned investigations, a longer gate length made V_{hold} higher for NMOS. However, a gate length that is too long reduces the robustness of the NMOS. A solution where several NMOS are cascoded is investigated in order to meet the requirements of a high holding voltage and a flexible ESD design window. The device itself consists of a stack of NMOS in cascode configuration, where these NMOS are merged into the same active area. Figure 7(a) displays the schematic of the cascoded NMOS.

Figure 7(b) shows the TLP characteristics of the cascoded nNMOS (n is the number of NMOS that are cascoded together). Despite the holding voltage improving from 4.5 to 14 V, the I_{t2} almost standed upon 0.93/0.93/0.82 A when cascading 2/3/4NMOS respectively. As the results show, the cascading configuration increased the holding voltage and did not reduce ESD robustness.

In order to investigate the physical mechanism of cascoded NMOS, two-dimensional device simulations were performed. As shown in Fig. 8(a), the cascoded 3ggNMOS consisted of three NMOS, M1, M2 and M3. There were five parasitic BJTs governing the device operation including NPN1, NPN2, NPN3, NPN4 and NPN5. Its equivalent circuit, which is based on the Ebers–Moll equivalent model, is described as Fig. 8(b).

Assuming all of gate voltages were grounded, the parasitic BJTs turned on and operated once the avalanche current induced base potential exceeded 0.6 V. Figure 9(a) shows the current distribution of the device during parasitic BJT operation. It ensured that current flowed through parasitic

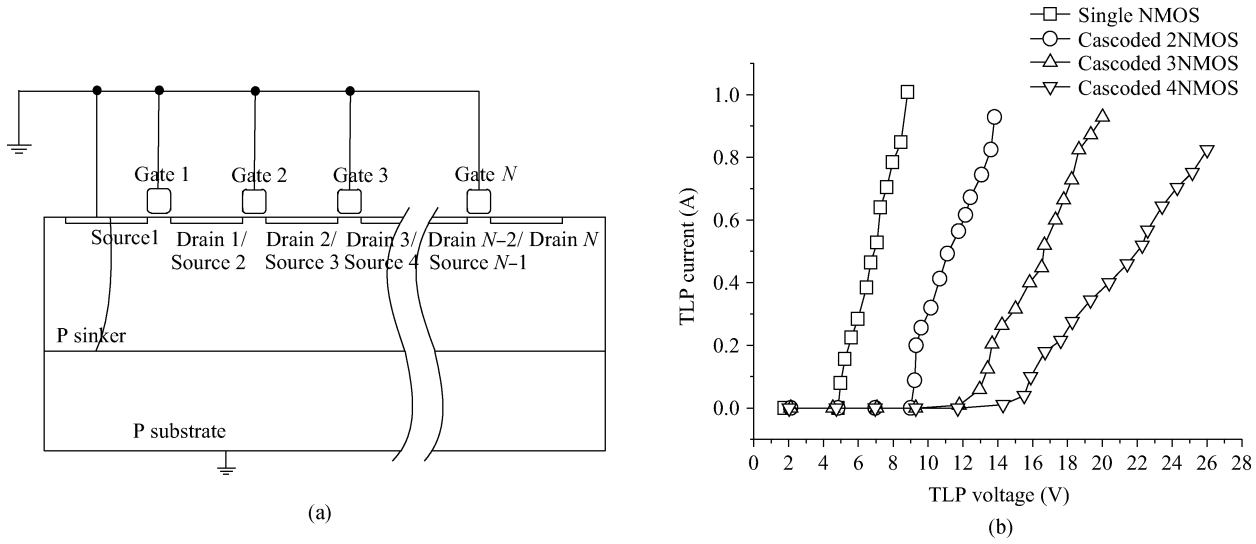


Fig. 7. (a) Schematic of cascoded nNMOS and (b) TLP characteristics of cascoded NMOS with different cascoded numbers.

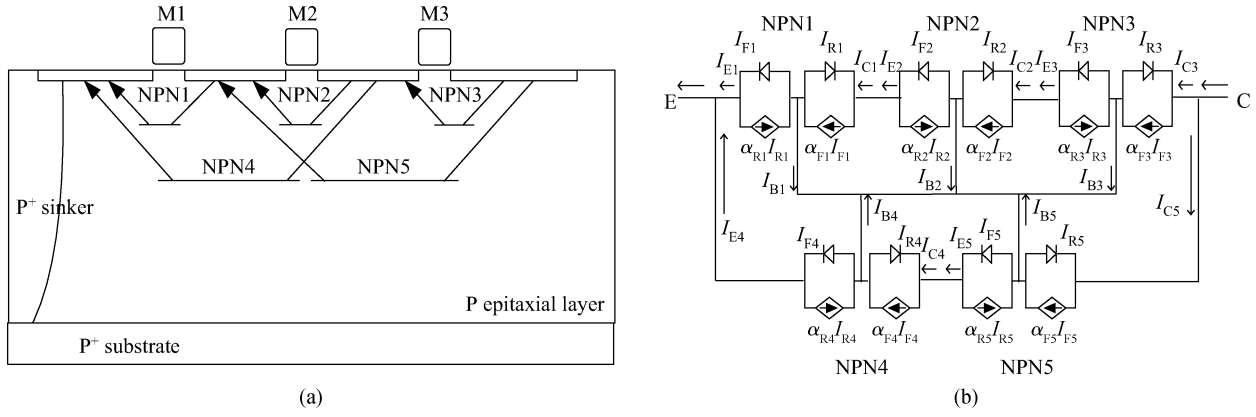


Fig. 8. (a) Schematic of cascoded 3NMOS and (b) Ebers–Moll model equivalent circuit.

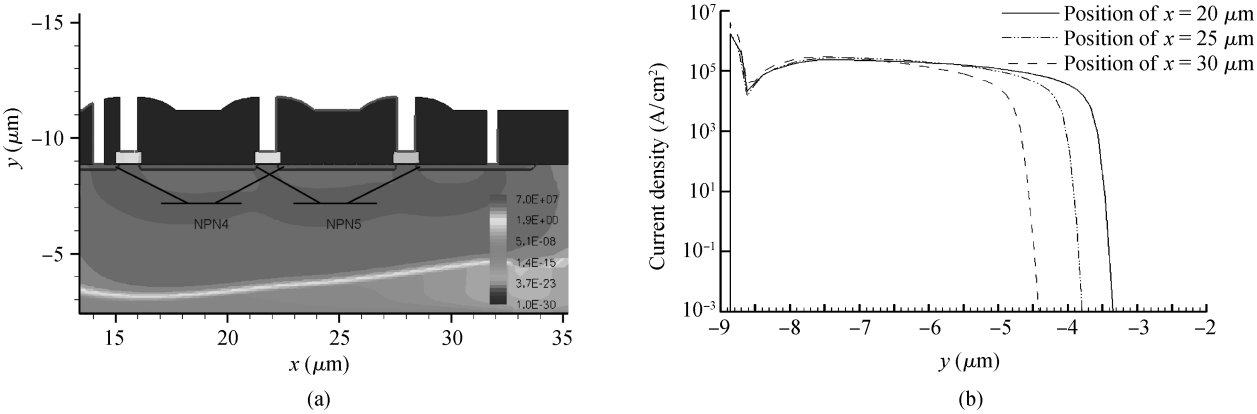


Fig. 9. (a) Two-dimensional device simulation of current distribution and (b) current density at x position of the cascoded 3NMOS during parastic BJT operation.

NPN4/NPN5 and sustained their action. Figure 9(b) shows that NPN1–NPN2–NPN3 was another current channel because of the high current density around $y = 8.8$ μm at $x = 20/25/30$ μm. Comparing to a single NMOS, the cascoded 3NMOS had a wider current channel to flow ESD charge that was like NPN4–NPN5 and NPN1–NPN2–NPN3. A higher current path caused the later thermal breakdown, according to the measured results.

Based on the Ebers–Moll model shown in Fig. 8(b), the holding voltage of the cascoded 3NMOS is as follows:

$$V_{\text{hold}} = V_{\text{CEnpn1}} + V_{\text{CEnpn2}} + V_{\text{CEnpn3}}. \quad (3)$$

For a single parasitic NPN, the collector–emitter voltage (V_{CE}) is given by[8]

$$V_{CE} = \frac{kT}{q} \ln \frac{I_B + I_C(1-\alpha_R)}{\alpha_R[I_B - I_C(1-\alpha_F)/\alpha_F]}. \quad (4)$$

Hence,

$$V_{hold} = \frac{kT}{q} \ln \frac{I_{B1} + I_{C1}(1-\alpha_{R1})}{\alpha_{R1}[I_{B1} - I_{C1}(1-\alpha_{F1})/\alpha_{F1}]} + \frac{kT}{q} \ln \frac{I_{B2} + I_{C2}(1-\alpha_{R2})}{\alpha_{R2}[I_{B2} - I_{C2}(1-\alpha_{F2})/\alpha_{F2}]} + \frac{kT}{q} \ln \frac{I_{B3} + I_{C3}(1-\alpha_{R3})}{\alpha_{R3}[I_{B3} - I_{C3}(1-\alpha_{F3})/\alpha_{F3}]}. \quad (5)$$

Here α_F and α_R are the large-signal forward and reverse common-base current gains, respectively. I_{B1}, I_{C1}, I_{B2}, I_{C2}, I_{B3} and I_{C3} are base or collection current, as Figure 8(b) shows. They strongly depend only on device parameters and process flow while did not vary apparently when cascading more NMOS. Comparing with a single NMOS, its V_{hold} increased effectively through cascoding 3NMOS together.

Consequently, cascading several NMOS increased the holding voltage and did not reduce ESD robustness. For a high gate operation voltage RF-LDMOS, the V_{hold} of integrated ESD protection could be elevated to the desired level to meet requirements of latch up immunity.

4. Conclusion

With the development of microelectronic technologies, ESD protection becomes an important issue. The ESD protection investigations for the gate oxide of an RF-LDMOS are presented in this paper. Based on experiments, a cascoded NMOS was demonstrated and selected as ESD protection for the gate oxide of an RF-LDMOS to obtain a flexible ESD design window and potential latch-up risk immunity.

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