# Impact of the lateral width of the gate recess on the DC and RF characteristics of InAlAs/InGaAs HEMTs*

Zhong Yinghui(钟英辉)[1,2], Wang Xiantai(王显泰)[2], Su Yongbo(苏永波)[2], Cao Yuxiong(曹玉雄)[2], Jin Zhi(金智)[2,†], Zhang Yuming(张玉明)[1], and Liu Xinyu(刘新宇)[2]

[1]Microelectronics Institute, Xidian University, Xi'an 710071, China
[2]Institute of Microelectronics, Chinese Academy of Sciences, Beijing 100029, China

**Abstract:** We fabricated 88 nm gate-length InP-based InAlAs/InGaAs high electron mobility transistors (HEMTs) with a current gain cutoff frequency of 100 GHz and a maximum oscillation frequency of 185 GHz. The characteristics of HEMTs with side-etched region lengths ($L_{\rm side}$) of 300, 412 and 1070 nm were analyzed. With the increase in $L_{\rm side}$, the kink effect became notable in the DC characteristics, which resulted from the surface state and the effect of impact ionization. The kink effect was qualitatively explained through energy band diagrams, and then eased off by reducing the $L_{\rm side}$. Meanwhile, the $L_{\rm side}$ dependence of the radio frequency characteristics, which were influenced by the parasitic capacitance, as well as the parasitic resistance of the source and drain, was studied. This work will be of great importance in fabricating high-performance InP HEMTs.

**Key words:** kink effect; HEMT; gate recess; InP; InAlAs/InGaAs
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## 1. Introduction

Millimeter and submillimeter-wave frequency ranges are of great interest for remote atmospheric sensing, next-generation automotive collision-avoidance radars, broadband satellite communications and low noise detectors. InP-based high electron mobility transistors (HEMTs) have demonstrated high-frequency, low microwave and millimeter wave noise, and high-gain performance due to high sheet carrier density, high peak drift velocity and high mobility in the channel. The devices are therefore considered to be one of the most promising for these applications. Excellent results for InP-based HEMTs have been reported by different groups, e.g. $f_{\rm T}$ = 628 GHz and $g_{\rm m,\,max}$ = 1.62 S/mm for 30 nm InAs pseudomorphic InP HEMTs[1] and $f_{\rm T}$ = 385 GHz, $f_{\max} > 1$ THz for sub-50 nm InP HEMTs[2]. Although these HEMTs are perfect candidates for active high-frequency devices, there will still be some problems if the length of the side-etched region ($L_{\rm side}$) is not perfectly optimized. The kink effect, a sudden rise in the drain current at a certain drain-to-source voltage ($V_{\rm DS}$), is one of the most important anomalies in DC characteristics. It results in high drain conductance, $g_{\rm m}$ compression and poor linearity. Generally, it is deemed that impact ionization and deep traps in the buffer[3] or barrier[4] are responsible for the kink effect in InAlAs/InGaAs HEMTs. In our experiments, different characteristics owing to the kink effect are exhibited in devices with a different $L_{\rm side}$, even on the same wafer, and therefore the kink effect may be related to the process conditions as well as the crystal growth. In addition to decreasing the $L_{\rm side}$, the introduction of an InP etching-stopper layer as surface passivation can make the pinning Fermi level close to the conduction band minimum, thus the initial density in the channel would be high enough to make the imaged electron inconspicuous[5] and finally improve the kink effect. Meanwhile, the radio frequency (RF) characteristics will vary with $L_{\rm side}$, and are influenced by the parasitic capacitance $C_{\rm p}$ as well as the parasitic resistance of $R_{\rm s}$ and $R_{\rm d}$.

In this paper, the design, fabrication and measurements of 88 nm gate-length InP-based InAlAs/InGaAs HEMTs are presented. Frequency characteristics of $f_{\rm t}$ = 100 GHz and $f_{\max}$ = 185 GHz are demonstrated, and we fabricate the HEMTs with $L_{\rm side}$ values of 300, 412 and 1070 nm. Based on the experiment, the kink effect is qualitatively explained through energy band diagrams, and finally eased off by reducing the $L_{\rm side}$. Meanwhile, the $L_{\rm side}$ dependence of the RF characteristics, which are influenced by the parasitic capacitance $C_{\rm p}$ as well as the parasitic resistance of $R_{\rm s}$ and $R_{\rm d}$, is studied. This work will be of great importance for fabricating high-performance InP HEMTs.

## 2. Material structures

Figure 1 shows a schematic cross-section of the InP-based HEMTs. The epitaxial layer structures were grown on 3 inch semi-insulating (100) InP substrates by molecular beam epitaxy (MBE). The epitaxial structure of the HEMTs employed in our study was designed and optimized with the parameters shown in Table 1. The layers, from bottom to top, consisted of an InAlAs buffer, an InGaAs channel, an unstrained InAlAs spacer layer, a Si-doped plane ($5 \times 10^{12}$ cm$^{-2}$), a 12 nm thick unstrained InAlAs Schottky barrier layer, and a composite InGaAs cap layer consisting of a Si-doped InGaAs cap layer ($3 \times 10^{19}$ cm$^{-3}$) and a Si-doped $\rm In_{0.53}Ga_{0.47}As$ transition layer ($5 \times 10^{18}$ cm$^{-3}$). All the InAlAs layers were lattice matched with the InP substrate. The two-dimensional electron gas (2DEG)

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† Corresponding author. Email: jinzhi@ime.ac.cn
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Table 1. The structure of the device epitaxial layer.

| Layer | Material | Doping | Thickness (nm) |
|---|---|---|---|
| Cap layer | $In_{0.6}Ga_{0.4}As$ | Si: $N^{++}$ $3 \times 10^{19}$ cm$^{-3}$ | 15 |
| Cap layer | $In_{0.53}Ga_{0.47}As$ | Si: $N^{+}$ $5 \times 10^{18}$ cm$^{-3}$ | 15 |
| Barrier layer | $In_{0.52}Al_{0.48}As$ | Undoped | 12 |
| Si planar-doped layer | | $5 \times 10^{12}$ cm$^{-2}$ | |
| Spacer layer | $In_{0.52}Al_{0.48}As$ | Undoped | 3 |
| Channel | $In_{0.53}Ga_{0.47}As$ | Undoped | 15 |
| Buffer layer | $In_{0.52}Al_{0.48}As$ | Undoped | 500 |
| S.I. InP Sub | | | |

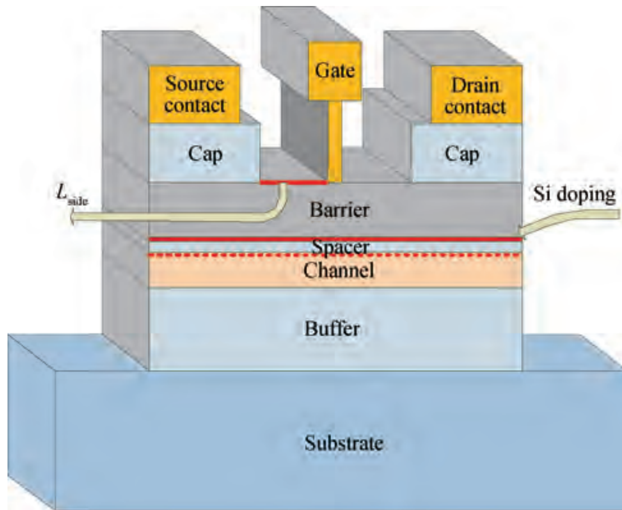


Fig. 1. A schematic cross-section of the InP-based HEMT.

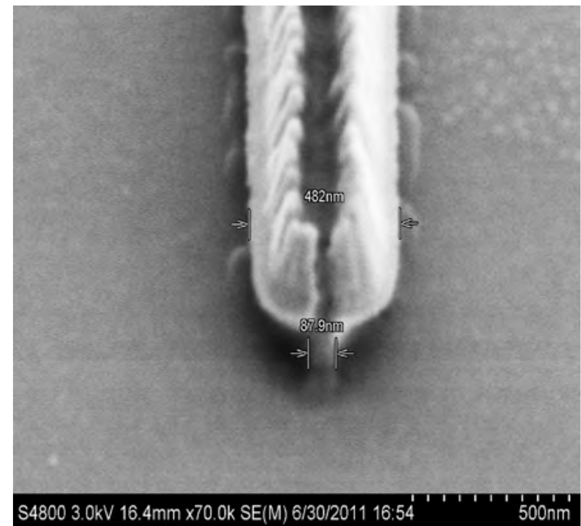


Fig. 2. An SEM photograph of a T-gate.

sheet density was $3.266 \times 10^{12}$ cm$^{-2}$ and the mobility was 8000 cm$^2$/(V·s) at room temperature.

## 3. Fabrication process

The fabrication of the HEMTs was based on both optical and electron beam lithography. The source and drain ohmic contacts were spaced 2.4 $\mu$m apart by a lift-off process. After pattern lithography, Ni/Ge/Au/Ge/Ni/Au (40/40/660/80/30/2200 Å) was evaporated by an electron beam evaporator to achieve ohmic metallization. Then the devices were annealed in nitrogen at a temperature of 270 ℃ for 3 min to decrease the contact resistance between the metal and semiconductor. Transmission line method (TLM) measurements revealed a contact resistance of 0.0698 Ω·mm and specific contact resistivity of $5.98 \times 10^{-7}$ Ω/cm$^2$ on linear TLM patterns. After that, device isolation was achieved through the mesa formation by means of phosphorus acid-based wet chemical etching to expose the $In_{0.52}Al_{0.48}As$ buffer layer. In order to measure the on-wafer DC and RF characteristics, the coplanar waveguide bond pads were formed using photoresist AZ5214, and Ti/Au (250/3000 Å) connection wires were evaporated.

The final and most important process in the HEMT fabrication was the gate process, which included gate lithography, recess and metallization. The 88 nm T-gate, as shown in Fig. 2, was defined by electron beam lithography in a trilayer of PMMA/Al/UVIII. The gate recess was formed by succinic acid/hydrogen peroxide wet chemical etching. Devices with different $L_{side}$ values of 300, 412 and 1070 nm were fabricated by controlling the etching time to be 1.5, 3 and 5 min. Surface-related effects were minimized by limiting the $L_{side}$. The gate recess of the devices was observed by a scanning electron microscope (SEM), as shown in Fig. 3. During the whole process, no surface passivation was performed, and this will cause a parasitic gate-capacitance effect and then weaken the high-frequency performance.

## 4. Results and discussion

The on-wafer DC and RF characteristics were measured using the Agilent E8363B PNA series vector network analyzer and on-wafer probes at room temperature.

### 4.1. DC characteristics

Figures 4(a)–4(c) show the current–voltage ($I$–$V$) characteristics at room temperature for the HEMTs with different $L_{side}$ values. The source–drain current was well pinched off. The device with the smallest $L_{side}$ of 300 nm exhibited the largest output conductance.

As shown in Fig. 4, the magnitude of the kink may change significantly with increasing $L_{side}$. The device is biased at a value of $V_{GS}$ above the threshold. In equilibrium ($V_{DS} = 0$ V) state, the Fermi level ($E_F$) will be pinned at neutral level ($q\Phi_0$) because the surface levels formed by the traps originated from oxygen, metals and other surface contamination, and also

Fig. 3. SEM photographs of HEMTs with different $L_{\rm side}$ values of (a) 1070, (b) 412 and (c) 300 nm. The etch time was (a) 5, (b) 3 and (c) 1.5 min.

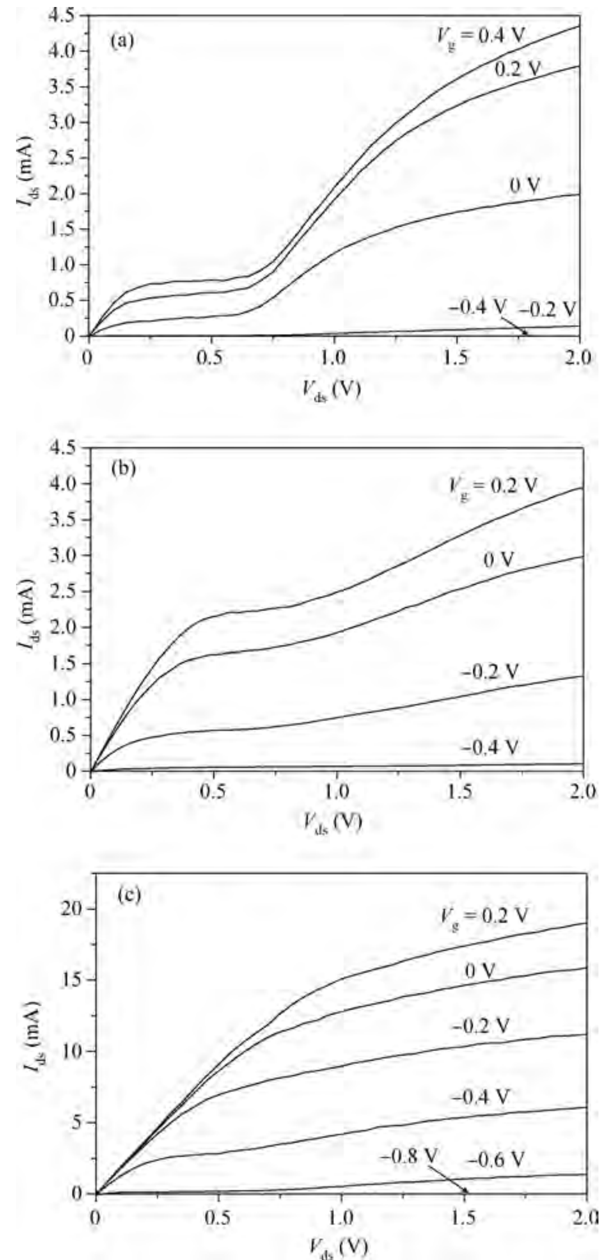


Fig. 4. The typical $I$–$V$ characteristics of HEMTs with $L_{\rm side}$ values of (a) 1070, (b) 412 and (c) 300 nm. The etch time was (a) 5, (b) 3 and (c) 1.5 min.

pinned at the buffer-substrate interface due to the trap formed during MBE[6, 7] (Fig. 5(a)). When $V_{\rm DS}$ increases, impact ionization will occur because of the small energy band gap ($E_{\rm g}$) of the $\rm In_{0.53}Ga_{0.47}As$ channel. Hence, a mass of holes and electrons will be produced on the high-field drain end of the gate, and the holes will flow through the channel toward the source, where the recombination speed is low, and then finally accumulate in the channel. Then, the quasi-Fermi level ($E_{\rm Fp}$) of the holes in the channel layer will move closer to the valence band. The quasi-Fermi level for the electrons and that for holes is no longer equal. The $E_{\rm Fp}$ must bend in order to maintain Fermi pinning at the surface and the buffer, resulting in a current of small holes flowing to the surface and buffer until the $E_{\rm Fp}$ is almost flat. Obviously, as holes reach the surface and the buffer-substrate interface, the charge at these locations is changed. Then, additional electrons will be imaged in the channel, raising the $E_{\rm Fn}$ and the potential of the channel as shown in Fig. 5(c). Finally, the drain–source current ($I_{\rm ds}$) will be abruptly increased (Fig. 5(c)), which is the so-called kink effect. When the $L_{\rm side}$ is short enough, the kink will not appear. This can be explained by the fact that the channel electron density reduced by the surface depletion was recovered by the penetration of elec-

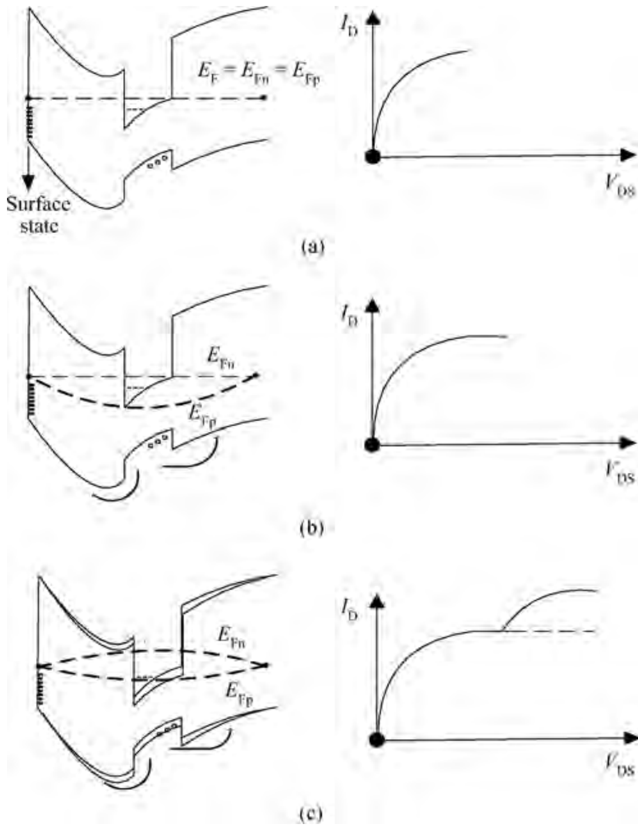


Fig. 5. The kink (the source end of the gate recess region) mechanism. (a) The quasi-Fermi levels for electrons ($E_{Fn}$) and holes ($E_{Fp}$) are equal at low $V_{DS}$. (b) When the holes begin to accumulate, the $E_{Fp}$ in the channel moves closer to the valance band. (c) Some of the holes move to the surface depletion region to equalize $E_{Fp}$, resulting in an increase in channel electron density.

trons from the adjacent electron-rich region if the $L_{side}$ is short enough, as shown in Fig. 4(c)[8].

### 4.2. RF characteristics

The $f_T$ value was determined by extrapolating the current gain ($H_{21}$) and the $f_{max}$ by extrapolating the maximum available/stable power gain (MAG/MSG) and unilateral power gain ($U$) using a least-squares fitting with a –20 dB/decade slope after subtracting the parasitic parameters due to the probing pads.

Figure 6 shows the typical RF characteristics of HEMTs with $L_{side}$ values of 1070, 412 and 300 nm at the same bias condition. With the decrease in $L_{side}$, $f_T$ gradually increases from 32 to 100 GHz, and $f_{max}$ increases at first and reaches its maximum of 215 GHz at $L_{side} = 412$ nm. The $L_{side}$ dependence of $f_T$ and $f_{max}$ can be explained by the influence of parasitic capacitance as well as the parasitic resistance of $R_s$ and $R_d$. The reduction in $L_{side}$ enhances the electric field in the channel and hence cuts down the electron transmit time. Also, the access part of $R_s$ and $R_d$ will be reduced with the decrease in the recess region, resulting in an increase in the transconductance, finally improving the $f_T$. On the other hand, the shorter the $L_{side}$, the larger $C_{gd}$ will be. According to Eq. (1), $f_{max}$ will decrease with the increase in $C_{gd}$. However, the access part of $R_s$ and $R_d$ will decrease with the reduction in $L_{side}$, which means that the reduction in $L_{side}$ is beneficial for the improvement of $f_{max}$.

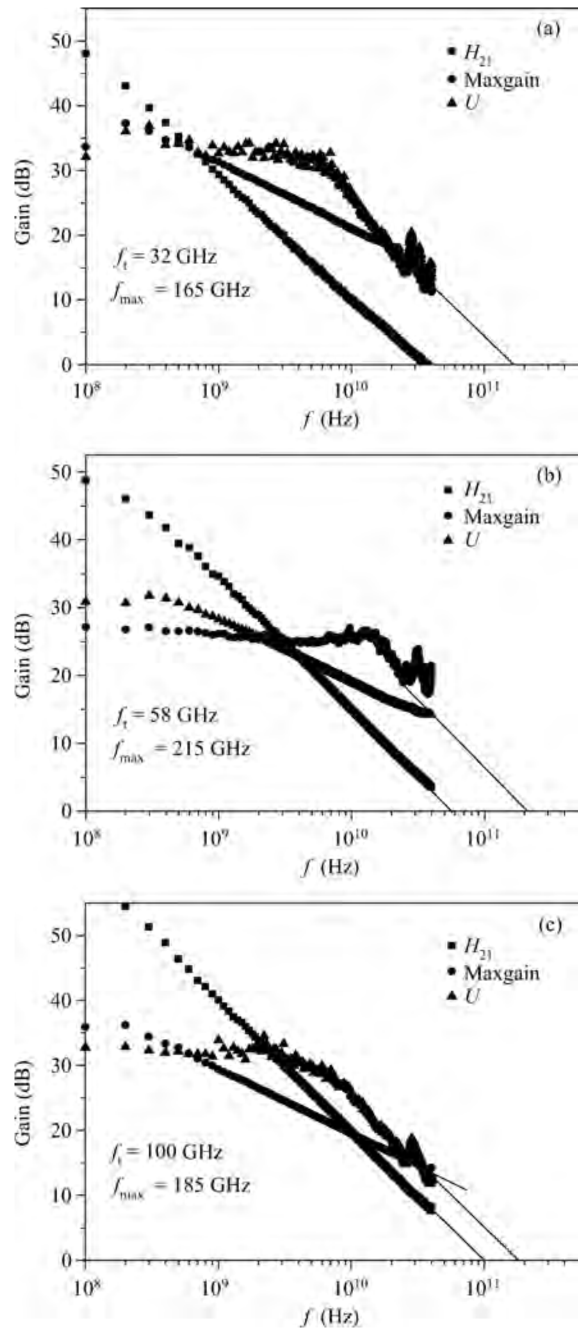


Fig. 6. The typical current gain ($H_{21}$), maximum available/stable power gain (MAG/MSG) and unilateral power gain ($U$) of HEMTs with $L_{side}$ values of (a) 1070, (b) 412 and (c) 300 nm. The gate voltage is 0 V and the drain voltage is 2 V. The etch time was (a) 5, (b) 3 and (c) 1.5 min.

On the whole, $f_{max}$ can be maximized with an optimized $L_{side}$.

$$f_{max} = \frac{f_t}{\sqrt{4g_{ds}(R_i + R_s + R_g) + \frac{2C_{gd}}{C_{gs}}\left[\frac{C_{gd}}{C_{gs}} + g_m(R_i + R_s)\right]}}. \quad (1)$$

In particular, the device was originally designed to be 2 × 50 $\mu$m, but the layers along the source and drain metals were damaged in the mesa process, as shown in Fig. 7. The effective gate width of the HEMT was reduced by one-third of the original with the same parasitic.

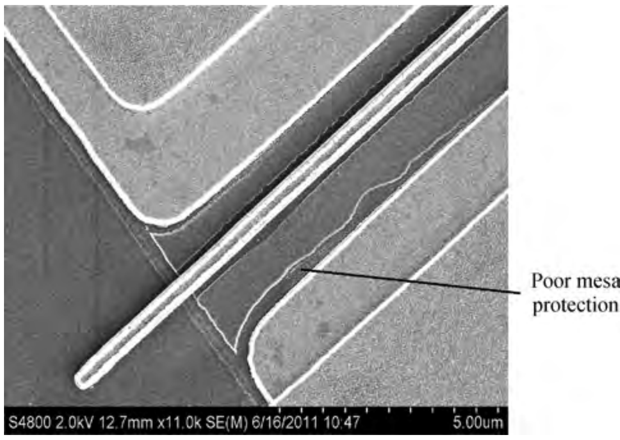


Fig. 7. An SEM photograph of the device (the layers along the source and drain metals were damaged in the mesa process).

$$g_{\mathrm{m}} = \frac{W C'_{\mathrm{ox}} \mu_{\mathrm{n}}}{L} (V_{\mathrm{GS}} - V_{\mathrm{T}})(1 - \alpha), \tag{2}$$

$$f_{\mathrm{T}} = \frac{g_{\mathrm{m}}}{2\pi (C_{\mathrm{gs}} + C_{\mathrm{gd}})}. \tag{3}$$

According to Eqs. (2) and (3), the characteristics of the device will deteriorate quite seriously. It can be inferred that the $I_{\mathrm{ds}}$ and frequency would be increased by at least 50% with proper mesa protection.

## 5. Conclusions

The design, fabrication and measurements of 88 nm gate-length InP-based InAlAs/InGaAs HEMTs were described in this paper. The frequency characteristics of $f_{\mathrm{t}} = 100$ GHz and $f_{\max} = 185$ GHz were demonstrated, and HEMTs of three different $L_{\mathrm{side}}$ values of 1070, 412 and 300 nm were fabricated. The kink effect can be eased off by shortening the $L_{\mathrm{side}}$. Meanwhile, the variation in $L_{\mathrm{side}}$ will influence the RF characteristics, and the $L_{\mathrm{side}}$ should be optimized to improve the kink effect and gain excellent RF characteristics of $f_{\mathrm{T}}$ and $f_{\max}$. This work will be of great importance in fabricating high-performance InP HEMTs.

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