Design of a CMOS multi-mode GNSS receiver VCO

Long Qiang(龙强)†, Zhuang Yiqi(庄奕琪), Yin Yue(阴玥), and Li Zhenrong(李振荣)

National Key Laboratory of Wide Band-Gap Semiconductor Technology, School of Microelectronics, Xidian University, Xi'an 710071, China

Abstract: A voltage-controlled oscillator (VCO) with dual stages of accumulation mode varactors for a multi-mode global navigation satellite system (GNSS) application, which adopts sigma–delta fractional-N technology in the synthesizer, is presented. The structure is selected to optimize the frequency coverage and tuning linearity, based on a general analysis of the parasitic capacitance in the coarse tuning switch bank cells, which cover the global positioning system (GPS) and Beidou (BD) bands. The VCO implemented in the 0.18 μm CMOS process can cover the GPS L1, BD B1, B2 and B3 bands with sufficient margin, and exhibits low phase noise by using this tuning curve linearization technique. The equalized $K_{\rm vco}$ characteristic behavior further offers a wide voltage tuning range and improves the stability of the closed loop.

Key words: VCO; phase noise; GPS; tuning linearity; GNSS; multi-mode

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1. Introduction

At present, most research concentrates on global positioning system (GPS) or Beidou (BD) applications, and only supports one or two bands of global navigation satellite system (GNSS) applications, which restricts the application area for low power and low-cost application[1, 2]. With the development of navigation systems, we need to integrate the different bands of GNSS in one chip. So the voltage-controlled oscillator (VCO) needs to have a wide tuning range to cover the GPS and BD bands, and provide excellent tuning linearity, simultaneously. In this paper we adopt the dual-varactor stage, combine digital and analog tuning in the VCO core, and compare with the conventional structure[3]. This widens the coverage range of the VCO, providing superior phase noise and tuning linearity, simultaneously, but the area of the chip and current dissipation has distinctly increased.

The structure of the sigma–delta fractional-N synthesizer is shown in Fig. 1, and the following sections present an optimized VCO[4] design. A deductive analysis for the coarse tuning switch bank[5] is made, based on which the structure of the dual-varactor stages is chosen, and the switch bank is analyzed in detail. The $K_{\rm vco}$[6] equalization principle featuring this architecture is explained in detail. This VCO implemented in the 0.18 μm CMOS process demonstrates the efficiency of this architectural optimization.

2. VCO architecture selection and optimization

In the transceivers for modern communication applications, an often used approach to achieve a wide tuning frequency range with small VCO gain and relatively linear tuning curve, simultaneously, is to break a single broadband tuning curve into several narrow sub-bands with sufficient frequency overlap[7]. The continuous tuning can be implemented using MOS varactors, while the discrete sub-band is chosen by a capacitive switch bank with several coarse tuning bits in the phase locked loop (PLL) calibration procedure[8]. The structure of the VCO is shown in Fig. 2.

In order to meet the requirements of both tuning linearity and frequency coverage under the constraint of power consumption, we have to take into consideration the trade-offs in the different structures, while making optimizations.

To cover the whole GNSS frequency range with sufficient production margin and to keep excellent tuning linearity below the specification, the determination of the number of the switch bank bits is of great significance.

2.1. Analysis of the switch bank structure

Based on conventional single-stage varactor architecture, the structure consisting of four or five binary-weighted switch bank bits is the best possible candidate to meet all the requirements[9−12]. The structure of the switch bank is shown in Fig. 3. Due to the tight specifications, however, meticulous analysis has to be made. Compared with the four-bit structure, the five-bit structure offers a narrower space, by half, between the fine tuning curves, and henceforth a larger overlap among every three consecutive curves. The VCO gain can therefore be reduced significantly. The flatness in the $K_{\rm vco}$ curve is an essential characteristic to improve the PLL performance. A low $K_{\rm vco}$ makes the VCO less sensitive to the injection of noise from the bias, and according to the open loop gain of a PLL,

$$G_{\rm OL}(p) = \frac{I_0}{2\pi} Z(p) \frac{K_{\rm VCO}}{p} \frac{1}{N_{\rm div}}, \tag{1}$$

with I_0 denoting the charge-pump current, $Z(p)$ the loop filter impedance and $N_{\rm div}$ the division ratio of the feedback loop. A large variation in $K_{\rm vco}$ may cause loop stability problems, degrade closed loop integrated phase noise and even possibly render the loop divergent. Furthermore, a lower VCO gain can also have better rejection of voltage supply variations. In this sense,

† Corresponding author. Email: Plike8846@163.com
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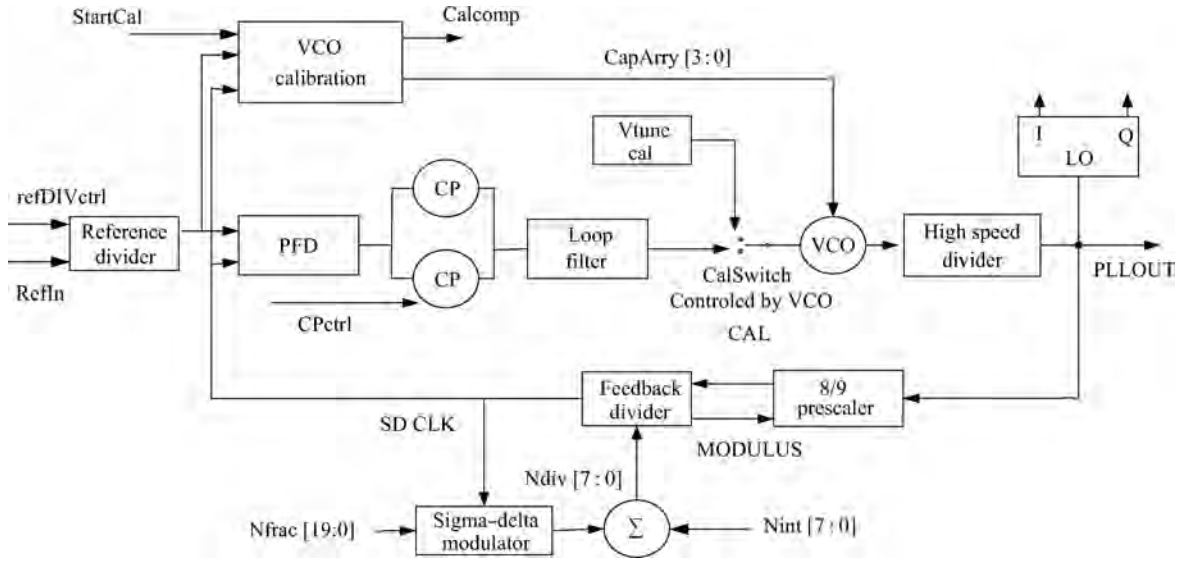

Fig. 1. The structure of the sigma–delta fractional-N synthesizer.

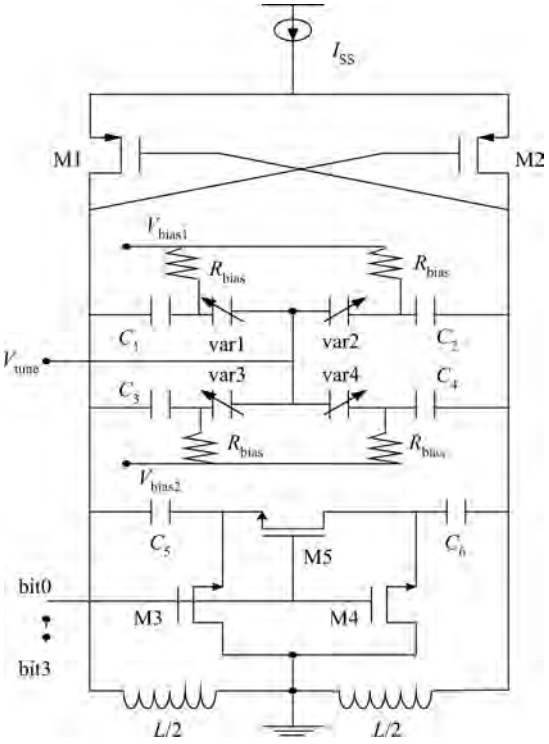

Fig. 2. Schematic of a VCO with dual-varactor stages.

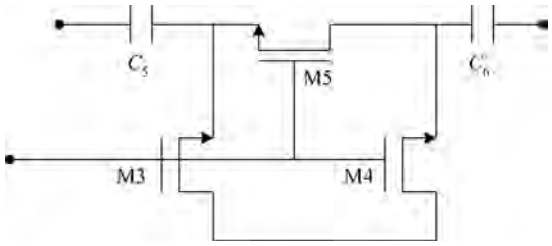

Fig. 3. The structure of a switch bank cell.

the four-bit structure performs too high K_{vco} value, to span nearly twice the space as that in the five-bit one. This disadvantage is unavoidable in such architecture, because the $C(V)$ characteristic of the MOS varactor exhibits a large C_{max}/C_{min} ratio only within a transition voltage of about 0.3 V.

Unfortunately, adding more bits to the switch bank does not necessarily improve the overall VCO performance. A severe problem is that it may cause worse phase noise if the target frequency coverage is to be maintained. In fact, there is a hidden trade-off between the frequency coverage and the quality value due to the layout parasitics, which show increasing importance as the transistors scale down. This can be explained from the structure of a switch bank cell, as shown in Fig. 3. In this design, n-type MOS transistors are used to build the RF switch, $C_{d,Total}$ is the sum of the total drain parasitic fringe capacitance C_d and the parasitic capacitance C_L relating to layout and interconnect. C_d is equal to $W_{sw}C_{dd}$, where W_{sw} is the width of the switching transistor and C_{dd} is the drain fringe capacitance in a unit length. C_L is estimated to be 5–10 fF and does not change with the MOS size. C_s is the resonator capacitance with inductor. The Q factor is written as[13]

$$Q_{cell} = \frac{1}{\omega_0 C_s R_{ON}} \propto \frac{W_{sw}}{\omega_0 C_s}, \tag{2}$$

where R_{ON} is given by Eq. (3).

$$R_{on} = \frac{1}{\mu_n C_{ox} \dfrac{W}{L} (V_{GS} - V_t)}. \tag{3}$$

In this work, a single switch device for two capacitances in a differential fashion was used, which improves the quality factor of the switched capacitances. One half of the resistance, R_{on}, is added to each capacitance when the switch is on. The M3 and M4 transistors are used as the resistors, which reduces the area of the resistor.

For an N-bit switch bank, the number of homogeneous switch cells are binary weighted, i.e. 1, 2, …, 2^{N-1} cells controlled by bit_0, bit_1, …, bit_{N-1}, respectively. The minimum

and maximum switching capacitance values are calculated as

$$C_{\mathrm{sw,min},N} = (2^N - 1)\left(\frac{1}{C_{\mathrm{s},N}} + \frac{1}{C_{\mathrm{d},N} + C_{\mathrm{L}}}\right)^{-1}, \quad (4)$$

$$C_{\mathrm{sw,max},N} = (2^N - 1)C_{\mathrm{s},N}, \quad (5)$$

where $C_{\mathrm{s},N}$, C_{L} and $C_{\mathrm{d},N} = W_{\mathrm{sw},N}C_{\mathrm{dd}}$ are the capacitance for a single cell corresponding to the N-bit structure. In order to make a comparison between the $(N-1)$-bit and N-bit structure, we suppose the same cross-coupled MOS transistors, varactors and inductor. To cover the same frequency range, it needs $C_{\mathrm{sw,min},N} = C_{\mathrm{sw,min},N-1}$ and $C_{\mathrm{sw,max},N} = C_{\mathrm{sw,max},N-1}$. The homogeneity of the cells implies that the total quality factor of the entire switch bank[14] for the all-ON state is the same as that of a single cell, i.e. $Q_{\mathrm{total}} = Q_{\mathrm{cell}}$. Then the ratio of the total quality factor of the N-bit structure to that of the $(N-1)$-bit structure can be calculated as

$$\frac{Q_N}{Q_{N-1}} = \frac{W_{\mathrm{sw},N}C_{\mathrm{s},N-1}}{W_{\mathrm{sw},N-1}C_{\mathrm{s},N}} = 1 - \frac{2^{N-1}C_{\mathrm{L}}}{(2^{N-1}-1)W_{\mathrm{sw},N-1}C_{\mathrm{dd}}} < 1. \quad (6)$$

From this ratio, we can see that the switch bank with one more bit brings down the quality factor and causes the degradation of phase noise. More explicitly, we can express the switching transistor width and Q-factor corresponding to the N-bit structure from Eqs. (2)–(5) by iterative calculation:

$$W_{\mathrm{sw},N} = \frac{1}{2^N - 1}W_{\mathrm{sw},1} - \frac{2C_{\mathrm{L}}}{C_{\mathrm{dd}}}, \quad (7)$$

$$Q_N = Q_1 - \frac{2kC_{\mathrm{L}}}{\omega_0 C_{\mathrm{dd}}C_{\mathrm{s},1}}(2^N - 1), \quad (8)$$

where k is a constant. Obviously, both the switching transistor width and Q-factor decrease exponentially with N. Intuitively, the decline in Q-factor is simply because the parasitic capacitance does not decrease proportionally with the transistor width as N goes up. This apparently excludes the possibility of arbitrarily fine sub-bands in the VCO design. Against rising flicker noise, the navigation requirement for close-in phase noise also limits the decrease in the cross-coupled transistor width to compensate the MOS width of the switching cells. Therefore, the above analysis is rather against the use of the conventional five-bit architecture for navigation specification.

2.2. Dual-varactor stages

A feasible approach to solve the dilemma in the selection of switch bank structure under the constraints of power consumption and chip area is to employ multiple varactor stages[15] in the resonator tank. The structure of the dual varactor stage is shown in Fig. 4. In this design, we use the "lighter" four-bit structure with dual stages of accumulation mode varactors[16] biased at different voltages to guarantee the frequency coverage with a much lower VCO gain, while maintaining the tuning linearity from noticeable degradation, as shown in Fig. 4.

The capacitance versus voltage characteristics of the accumulation mode MOS varactor are very steep, which is shown in Fig. 5. This is the main drawback to this structure achieving a constant K_{vco}. The principle is to equalize the VCO gain in

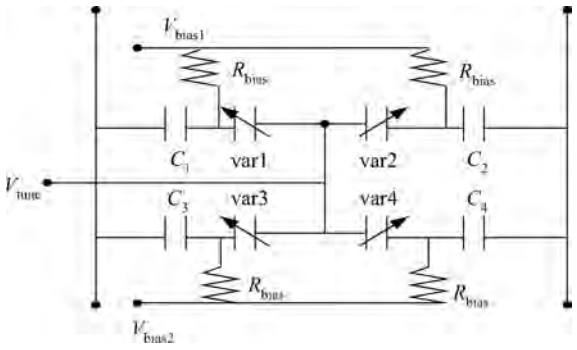

Fig. 4. The structure of the dual varactor stage.

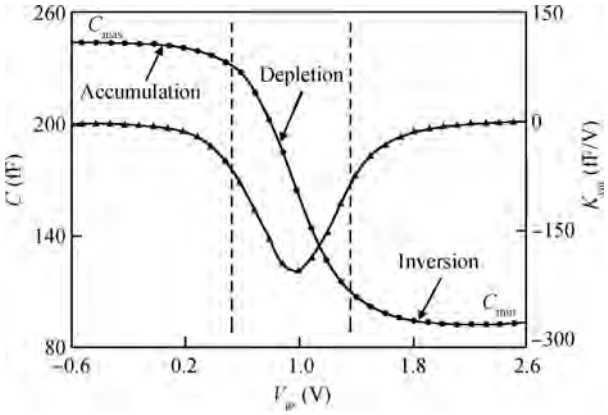

Fig. 5. The $C(V)$ characteristics of the accumulation mode MOS varactor.

a larger span of tuning voltage[17]. From the scheme, we can see that the steep part of each stage characteristic is centered on (near) its corresponding bias voltage. The total K_{vco} curve is the sum of two VCO gains, which is spread much wider than the original single K_{vco} curve over the voltage control range[18, 19]. Better linearity[20] in the tuning curves is obtained by equalizing K_{vco} so that the frequency space can be covered at a much smaller slope. A quantitative gauge of K_{vco} can be given by a factor of merit (FOM):

$$\mathrm{FOM}_{K_{\mathrm{vco}}} = \sigma_{K_{\mathrm{vco}}}/K_{\mathrm{vcoave}}. \quad (9)$$

This merit consists of the quadratic error between the K_{vco} and the average K_{vco} (K_{vcoave}) (Eq. (9)) over the voltage control range (Eq. (10)) normalized to the K_{vcoave}, with K_{vcoave} the average gain and $\sigma_{K\mathrm{vco}}$ the quadratic error[21].

$$K_{\mathrm{vcoave}} = \frac{1}{\Delta V}\int K_{\mathrm{vco}}(V)\mathrm{d}V, \quad (10)$$

$$\sigma_{K\mathrm{vco}} = \sqrt{\frac{1}{\Delta V}\int (K_{\mathrm{vco}}(V) - K_{\mathrm{vcoave}})^2\mathrm{d}V}. \quad (11)$$

Our design determines that the $\mathrm{FOM}_{K_{\mathrm{vco}}}$ equals 1.4, which is less than 50% of the conventional value. As stated in the previous subsection, a lower and flatter K_{vco} makes the VCO less sensitive to injected phase noise, keeps the loop more stable and offers a low supply pulling. Henceforth, the four-bit structure with dual-varactor stages relieves the conflict between

phase noise and frequency coverage to a great extent in the VCO design for navigation specification.

2.3. Further optimizations

With the VCO covering the navigation bands, the main task is to optimize the phase noise. The trade-off among the suppression of the noise contribution from the cross-coupled MOS transistors, the quality factor of the inductor and the switch bank cells, tank capacitance, power consumption and chip area are considered globally[22]. The stringent navigation specification for close-in phase noise, mainly consisting of flicker noise, requires special attention.

A usually ignored important phenomenon relating to the breakdown effect of transistors in the optimization of phase noise has to be pointed out here. Generally, the increase in bias current[23, 24] injected to the VCO core will improve the phase noise index. Beyond a certain extent, however, the large output swing makes the low-voltage rated cross-coupled MOS work in the breakdown region (or at least in a quasi-breakdown region) in some portion of an oscillation period, causing larger parasitic capacitance of the transistors[25]. This is a side effect in that it makes the tank "heavier", contradictive to the common concept about the influence of large signal swing on phase noise. The average MOS capacitance relates to the breakdown portion, which can be quantitatively calculated based on a statistical model. But more directly, this portion is displayed as the frequency reduction in the large signal (transient) simulation from the small signal (AC) simulation result (no breakdown occurs).

A two-turn spiral 1.3 nH differential inductor is designed by using the top metal layer. A patterned ground shield (PGS) is employed underneath to reduce substrate losses, which effectively raises the quality factor at the operation frequency. However, the parasitic capacitance of PGS[26, 27] is hard to estimate accurately due to the lack of a precise EM model. The only reliable approach is to fix the parasitic capacitance of the tank by frequency simulation referring to the measurement of the previous implementation.

3. Measurement results

The VCO chip is fabricated in a 0.18 μm CMOS process with six metal layers. The die photo is shown in Fig. 6. The VCO consumes 2 mA from a 1.8 V voltage supply, and the measured result demonstrates the efficiency of this architecture. As an insurance measure to adapt to PVT (process, voltage, temperature) variations, we added three additional cap cells switched by two control bits. The oscillator with a divider-by-two has a frequency range from 1195 to 1775 MHz , which covers the GNSS bands with sufficient margin. The coverage range is shown in Fig. 7.

The phase noise is measured in the closed loop environment with an Agilent Spectrum Analyzer. We used a very narrow bandwidth loop filter to show the close-in phase noise of the VCO. The measured phase noise at the 100 kHz and 1 MHz frequency offsets are –80, –115.9 dBc/Hz at the GPS L1 band and the BD B1 band; and –84.19, –108.9 dBc/Hz at the BD B2/B3 band, respectively (see Figs. 8 and 9). The low phase noise in fact benefits from the low parasitic capacitance of the entire switch bank and the cross-coupled transistors of larger width.

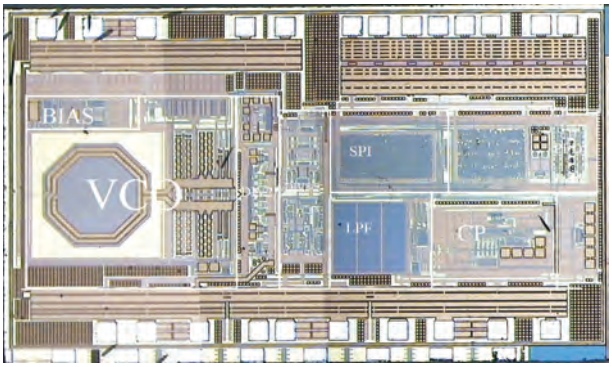

Fig. 6. Die photo of the fabricated VCO with a divider-by-two and a voltage reference.

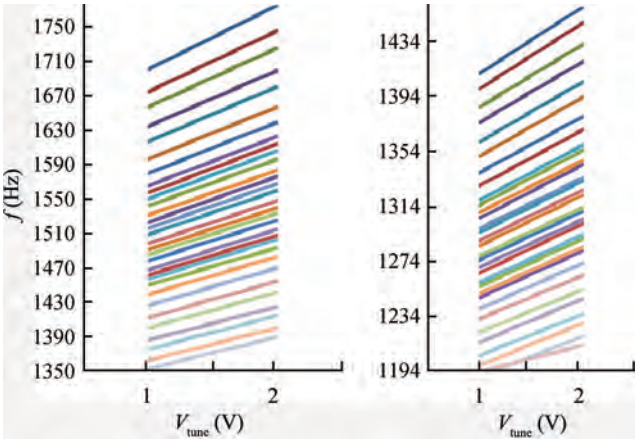

Fig. 7. The coverage range of PLL.

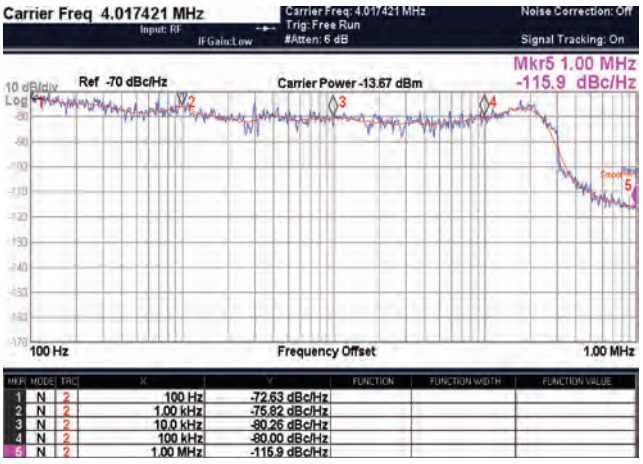

Fig. 8. The measured GPS L1 and BD B1 band phase noise of the VCO. The phase noise at the 1, 10, 100 kHz and 1 MHz frequency offsets are –75.82, –80.26, –80 and –115.9 dBc/Hz, respectively.

4. Conclusion

A four-bit VCO with dual-varactor stages for multi-mode GNSS applications is implemented in a 0.18 μm CMOS pro-

Table 1. A comparison with other PLLs.

Parameter	Ref. [28]	Ref. [19]	Ref. [29]	This work	This work
Technology	0.13 μm CMOS	0.18 μm CMOS	0.13 μm CMOS	0.18 μm CMOS	0.18 μm CMOS
Frequency (GHz)	3.1	1.752	1.8	1.571/1.561	1.268/1.207
Tuning range (GHz)	3.1–5.2	0.924–1.85	1.67–1.93	1.195–1.750	1.195–1.750
N (dBc/Hz)	–119 dBc @ 1 MHz	–127.1 dBc @ 1 MHz	–138 dBc @ 3 MHz	–115.9 dBc @ 1 MHz	–108.9 dBc @ 1 MHz
PDC (mW)	9.2	10.8	18	12.6	12.6
Supply voltage (V)	1.2	1.8	1.2	1.8	1.8

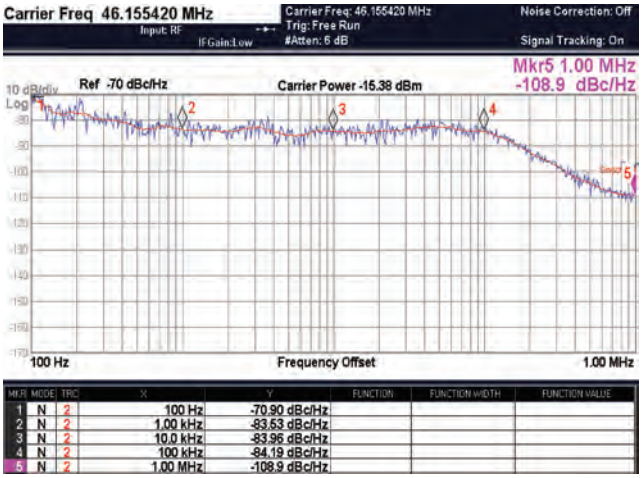

Fig. 9. The measured BD B2 and B3 band phase noise of the VCO. The phase noise at the 1, 10, 100 kHz and 1 MHz frequency offsets are –83.53, –83.96, –84.19 and –108.9 dBc/Hz, respectively.

cess. The selection of this architecture is based on a meticulous analysis of the influence of the parasitic capacitance in the switch bank cells on phase noise and frequency coverage. The optimized design exhibits a low phase noise at different bands: –80 dBc at 100 kHz and –115.9 dBc at 1 MHz at the GPS L1 band and BD B1 band; and –84.19 dBc at 100 kHz and –108.9 dBc at 1 MHz at the BD B2/B3 band, which simultaneously covers the GPS and BD bands. The spread K_{vco} curve can further offer a wide tuning range for the charge pump and improve the stability of the phase locked loop. The performance of this VCO is compared with other recently published VCOs in Table 1. These VCOs intend to adopt more switch banks, which widen the tuning range but bring down the quality factor of the switch bank and decrease the phase noise. Against rising flicker noise, the navigation requirements for the close-in phase noise also limits the decrease in the cross-coupled transistor width to compensate the MOS width of the switching cells. So this work optimizes the dual-varactor stage and switch bank to satisfy the requirements of multi-mode GNSS. Therefore, at the same process, this work achieves a wide tuning range, superior phase noise and excellent tuning linearity with no extra chip area and current dissipation.

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References

[1] Steyaert M, Coppejans P, de Cock W, et al. A fully-integrated GPS receiver front-end with 40 mW power consumption. International Solid-State Circuits Conference, Digest of Technical Papers, 2002: 396

[2] Xiao Hongbing, Guo Peiyuan. Modeling and simulation of higher-order PLL rotation tracking system in GNSS receiver. International Conference on Mechatronics and Automation, 2009: 1128

[3] Broussev S S, Lehtonen T A, Tchamov N T. A wide-band low phase-noise LC-VCO with programmable K_{vco}. IEEE Microw Wireless Compon Lett, 2007, 17(4): 274

[4] Craninckx J, Steyaert M. A CMOS 1.8-GHz low-phase-noise voltage controlled oscillator with prescaler. IEEE J Solid-State Circuits, 1995, 30: 1474

[5] Cannone F, Avitabile G. Multi-band VCO based on distributed VCO and switched-capacitors banks. Microwaves, Radar and Wireless Communications, 2008: 1

[6] Svelto F, Deantoni S, Castello R. A 1.3 GHz low-phase noise fully tunable CMOS LC VCO. IEEE J Solid-State Circuits, 2000, 35(3): 356

[7] Dec A, Suyama K. RF micromachined varactor with wide tuning range. IEEE Radio Frequency Integrated Circuits (RFIC) Symposium, 1998, 33(11): 922

[8] Li Zhenbiao, Ni Wenhai, Ma Jie, et al. Dual-band CMOS transceiver for 3G TD-SCDMA. IEEE Int Solid-State Circuits Conf Dig Tech Papers, 2007

[9] Fong N H W, Plouchart J O, Zamdmer N, et al. Design of wide-band CMOS VCO for multiband wireless LAN application. IEEE J Solid-State Circuits, 2003, 38: 1333

[10] Andreani P, Mattisson S. On the use of MOS varactors in RF VCO's. IEEE J Solid-State Circuits, 2000, 35: 905

[11] Ho C C, Liang G H, Huang C F, et al. VCO phase-noise improvement by gate-finger configuration of 0.13-μm CMOS transistors. IEEE Electron Device Lett, 2005: 258

[12] Jung B, Harjani R. A high-frequency LC VCO design using capacitive degeneration. IEEE J Solid-State Circuits, 2004: 2359

[13] Aktas A, Ismail M. CMOS PLLs and VCOs for 4G wireless. Chap 5. Kluwer, 2004

[14] Sadhu B, Harjani R. Capacitor bank design for wide tuning range LC VCOs: 850 MHz–7.1 GHz (157%). Proceedings of IEEE International Symposium on Circuits and Systems (ISCAS), 2010: 1975

[15] Moon Y J, Roh Y S, Jeong C Y, et al. A 4.39–5.26 GHz LC-tank CMOS voltage-controlled oscillator with small VCO-gain variation. IEEE Microw Wireless Compon Lett, 2009, 19(8): 524

[16] Sameni P, Siu C, Iniewski K, et al. Characterization and modelling of accumulation-mode MOS varactor. IEEE CCECE/CCGEL, 2005: 1554

[17] Li H, Rein H M. Millimeter-wave VCOs with wide tuning range and low phase noise fully integrated in a SiGe bipolar production

technology. IEEE J Solid-State Circuits, 2003, 38(2): 184
[18] Yu Y H, Su F K, Chen Y J E, et al. A 1 V wide tuning range VCO for UHF DTV tuner. Asia-Pacific Microwave Conference, 2007: 1
[19] Kim J, Shin J, Kim S, et al. A wide-band CMOS LC VCO with linearized coarse tuning characteristics. IEEE Trans Circuits Syst II, 2008: 309
[20] Rogers J W M. The effect of varactor nonlinearity on the phase noise of completely integrated VCOs. IEEE J Solid-State Circuits, 2000, 35: 1360
[21] Mira J, Divel T, Ramet S, et al. Distributed MOS varactor biasing for VCO gain equalization in 0.13 μm CMOS technology. IEEE Radio Frequency Integrated Circuits (RFIC) Symposium, Digest of Papers, 2004: 131
[22] Li Z, Kenneth K O. A 1-V low phase noise multi-band CMOS voltage controlled oscillator with switched inductors and capacitors. IEEE RFIC Symposium, 2004: 467
[23] Hung C C, Liu S I. A leakage-suppression technique for phase-locked systems in 65 nm CMOS. IEEE International Solid-State Circuits Conference, Digest of Technical Papers, 2009: 400
[24] Levantino S, Samori C, Bonfanti A, et al. Frequency dependence on bias current in 5 GHz CMOS VCOs: impact on tuning range and flicker noise upconversion. IEEE J Solid-State Circuits, 2002: 1003
[25] Razavi B. RF microelectronics. Prentice Hall, Upper Saddle River, NJ, 1998
[26] Rotella F M, Zachan J. Modeling and optimization of inductors with patterned ground shields for a high performance fully integrated switched tuning VCO. Proceedings of the IEEE Custom Integrated Circuits Conference, 2002: 221
[27] Yue C P, Wong S S. On-chip spiral inductors with patterned ground shields for Si-based RF IC's. IEEE J Solid-State Circuits, 1998, 33(5): 743
[28] Hauspie D, Park E C, Craninckx J. Wide-band VCO with simultaneous switching of frequency band, active core, and varactor size. IEEE J Solid-State Circuits, 2007, 42(7): 1472
[29] Vaananed P, Mikkola N, Helio P. VCO design with on-chip calibration system. IEEE Trans Circuits Syst, 2006, 53(10): 2157