A low power flexible PGA for software defined radio systems*

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Abstract: This paper proposes a new low power structure to improve the trade-off between the bandwidth and the power consumption of a programmable gain amplifier (PGA). The PGA consists of three-stage amplifiers, which includes a variable gain amplifier and DC offset cancellation circuits. The cutoff frequency of the DC offset cancellation circuits can be changed from 4 to 80 kHz. The chip was fabricated in 0.13 μm CMOS technology. Measurement results showed that the gain of the PGA can be programmed from –5 to 60 dB. At the gain setting of 60 dB, the bandwidth can be tuned from 1 to 10 MHz, while the power consumption can be programmed from 850 μA to 3.2 mA at a supply voltage of 1.2 V. Its in-band OIP3 result is at 14 dBm.

Key words: low power; DC offset; programmable gain amplifier; software defined radio

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1. Introduction

The requirements of next-generation wireless terminals are driving RFIC design toward ubiquitous multistandard connectivity at low power consumption and cost[1, 2]. The software defined radio (SDR) technique may be the right answer to this application demand. It can cover various wireless standards, including WLAN, TD-SCDMA, WCDMA, and CDMA2000, as shown in Table 1. The transceiver for SDR wireless communications must support a broad range of specifications, such as gain range, bandwidth, linearity, selectivity, and low power.

To reach the ultimate goal, the first step is to choose appropriate transceiver architecture. Among the many architectures available, zero-IF architecture is the most attractive one for SDR due to its simplicity and suitability for monolithic integration[3]. Though zero-IF architecture possesses many preferable characteristics, it still has a DC offset problem[4]. A small DC offset can be amplified by using a first stage amplifier to a level that saturates the following stage amplifiers and consequently prohibits the amplification of the desired signal. Thus, a programmable gain amplifier (PGA) must provide an effective solution to cancel the DC offset. Furthermore, the power consumption is another figure of merit, because in a battery-powered transceiver, extending the battery life as long as possible is one of the most important challenges. Some attempts to reduce the power consumption have been reported[2, 5], but there is still a lot room for improvement. Reference [2] utilizes a flexible amplifier array to reduce power, while its total dynamic gain range is limited. Reference [5] proposes a low-power constant bandwidth variable gain amplifier, but it needs extra buffer circuit to protect its low input resistance when inserted into the receiver chain.

This paper presents a low power, high dynamic range flexible PGA for software defined radio front-ends. A bandwidth boosting technique is proposed to improve the trade-off between bandwidth and power consumption. The PGA consists of three-stage amplifiers. Each amplifier includes mainly variable gain amplifier (VGA) and DC offset cancellation circuits. Its gain and bandwidth can be controlled by a digital signal.

2. PGA architecture

Figure 1 shows the architecture of a flexible PGA, which consists of three-stage amplifiers. Each amplifier mainly consists of VGA and DC offset cancellation circuits. In PGA architecture, we apply some techniques to realize a low power flexible PGA for software defined radio front-ends. Firstly, the first stage and the second stage amplifier can be bypassed and shut down according to the requirements. Secondly, the bandwidth of the PGA can be programmed by a digital signal from one

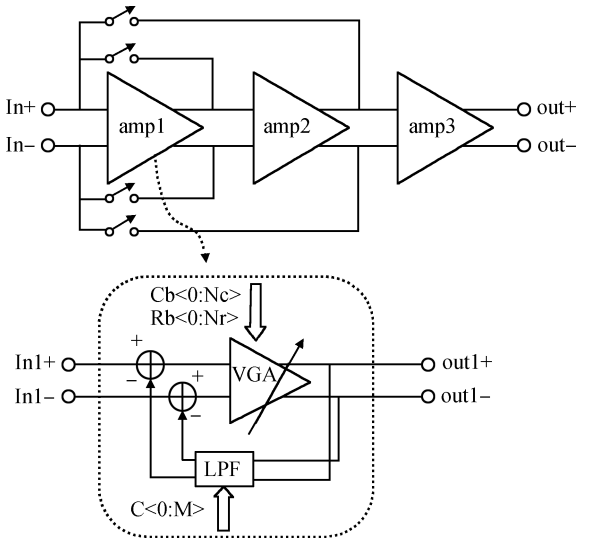

Fig. 1. Three-stage PGA and schematic of each amplifier.

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Table 1. Specifications of multistandard.

Standard	Bandwidth (MHz)	Sensitivity (dBm)	Modulation	Date rate (Mbit/s)
802.11b	22	–76	QPSK	11
TD_SCDMA	1.6	–108	QPSK	> 2
WCDMA	3.84	–117	QPSK	> 2
CDMA2000	1.25	–104	QPSK	> 2

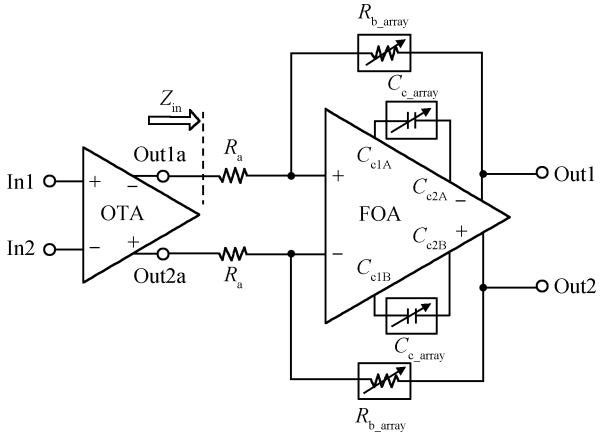

Fig. 2. Schematic of the VGA.

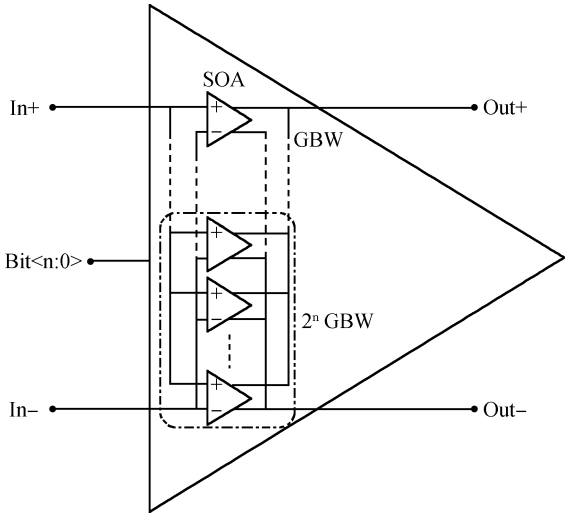

Fig. 3. The simplified schematic of the FOA.

megahertz to more than ten megahertz. Thirdly a novel VGA circuit is proposed to improve the trade-off between the bandwidth and the power consumption of the PGA by using an additional smart operational transconductance amplifier (OTA), as shown in Fig. 2. More detail may be found in Section 3.

Furthermore, the gain requirement of an SDR should be satisfied. WCDMA represents the worst case scenario for our SDR. With a full scale (FS) ADC input power of 2 dBm, and a DR of 50 dB, the quantization noise (QN) level would be –48 dBm. The minimum RX gain required at the WCDMA sensitivity level ($S_{\min}$) is given by $G_{\max} = \mathrm{QN} + M_{\mathrm{qn}} + SNR_{\min} - S_{\min}$. For QN to be negligible with respect to the RX thermal noise, 10 dB margin (M_{qn}) is taken[6]. The sensitivity level $S_{\min}$ is –117 dBm and the minimum signal to noise ratio ($SNR_{\min}$) is 10 dB. The minimum RX gain is 89 dB. Apart from the gain achieved by the front end of RX, the baseband needs to provide a gain of more than 60 dB.

In the PGA, the DC offset cancellation is realized by continuous-time feedback (CTF) technique. The CTF technique adopts a low pass filter (LPF) to feedback the DC offset voltage and the low frequency signal and to subtract them from the input signal. Because there is a considerable amount of signal energy near DC in wireless communication systems based on modulation schemes (PSK, ASK), the effective high pass cut-off frequency should be about 0.1% of data rate to avoid significant degradation[7]. Thus, we need to adjust the cut-off frequency of the LPF according to the data rate of each standard and the switching time specification from Tx to Rx. LPFs provide a wide range of cut-off frequencies which not only satisfy multistandards, but also ensure that the receiving signal settles down quickly through switching the cut-off frequency from high to low. According to the 802.11b standard, signal should settle down in less than 10 μs and the cut-off frequency should be set to 10 kHz[7].

3. Circuit analysis and design

3.1. VGA

VGA mainly consists of OTA, flexible op-amp (FOA), resistor R_{a}, resist array $R_{\mathrm{b\text{-}array}}$ and capacity array $C_{\mathrm{c\text{-}array}}$, as shown in Fig. 2. FOA includes some parallel switchable op-amps (SOAs) in a binary scaled array (Fig. 3). Different communication standards need different bandwidth requirements. The bandwidth of a VGA can be programmed by controlling the number of switch-on/off SOAs. At the same time, the power consumption can be optimized. The gain of the VGA depends on the ratio of a resistor array $R_{\mathrm{b\text{-}array}}$ to resistor R_{a}. The SOA is shown is Fig. 4, which consists of a two-stage amplifier, a standard Miller compensated capacitor, and a common mode feedback circuit. SOA is switched on/off through a single bit. Two Miller capacitors arrays $C_{\mathrm{c\text{-}array}}$ are connected at nodes C_{c1A}, C_{c1B}, C_{c2A} and C_{c2B}, and two resistor arrays $R_{\mathrm{b\text{-}array}}$ are connected at the input nodes and output nodes of the FOA, as shown in Fig. 5.

The FOA is the basic active component of a VGA. It provides a reconfigurable gain-bandwidth product (GBW). The power consumption depends on the bandwidth of the VGA. The number N_{on} of SOAs that are switched on in an FOA is determined by a digital control word bit<n:0> and is given by

$$N_{\mathrm{on}} = \sum_{k=0}^{n} \mathrm{Bit}\,\langle k\rangle \cdot 2^k. \tag{1}$$

Therefore, the FOA unity gain frequency can be calculated as follows:

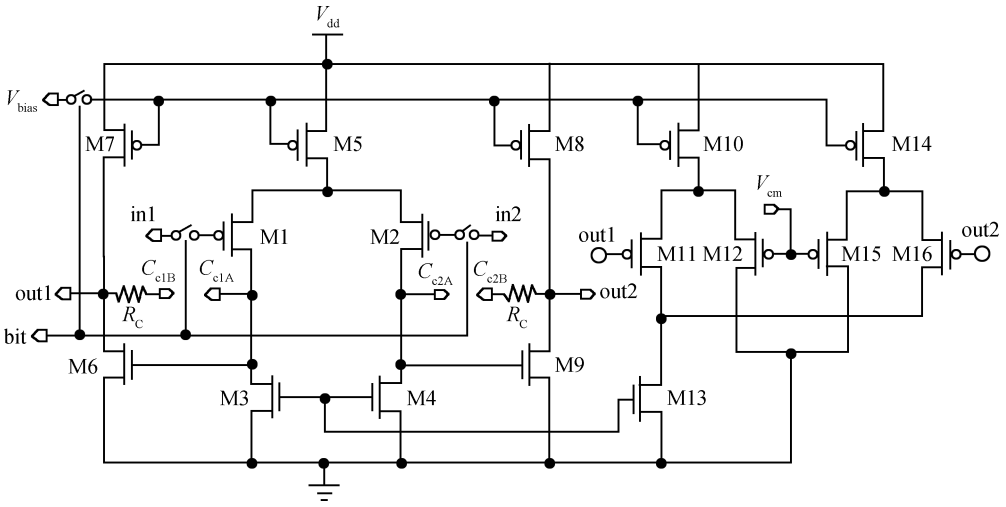

Fig. 4. Circuit structure of the SOA.

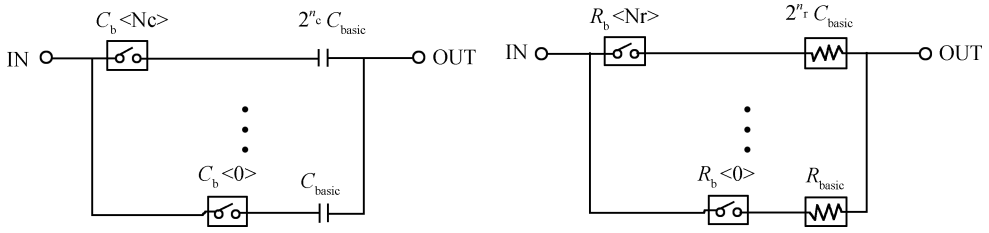

Fig. 5. Capacitor array $C_{c-array}$ and resistor array $R_{b-array}$.

$$\omega_u = \frac{g_{m1}}{C_c} N_{on}, \tag{2}$$

where g_{m1} is the transconductance of the transistors M1 in the input differential pair of SOA and C_c is the dynamic Miller capacitance value set by capacitors arrays $C_{c\text{-array}}$. R_c and C_c create a right half zero which could cancel the non-dominant pole in an SOA[8].

The transfer function of an SOA can be expressed as

$$A = \frac{A_{v1}A_{v2}\left[1 - sC_C\left(\frac{1}{g_{m6,9}} - R_C\right)\right]}{(1 + sr_{o1}A_{v2}C_C)\left(1 + s\frac{C_L}{g_{m6,9}}\right)}, \tag{3}$$

$$A_{v1} = g_{m1}(r_{o1}//r_{o3}), \tag{4}$$

$$A_{v2} = g_{m6}(r_{o6}//r_{o7}), \tag{5}$$

where g_{m1} and g_{m6} are the transconductance of the transistors M1, M6, and r_{o1}, r_{o3}, r_{o6}, r_{o7} are the output resistances of M1, M3, M6, M7. Here, the effect of LPF that follows the output of the VGA can be neglected here. In the numerator of Eq. (3), if we choose the proper value of resistor of R_c, the numerator can be made equal to $A_{v1}A_{v2}$. When the operation frequency is low, the pole created by the Miller capacitor dominates. Equation (3) could be reduced to:

$$A \cong \frac{A_{v1}A_{v2}}{1 + sr_{o1}A_{v2}C_C}. \tag{6}$$

Z_{in} seen in Fig. 2 can be expressed as[8]:

$$Z_{in} = R_b/A + R_a, \tag{7}$$

$$Z_{in} = \frac{R_b}{A_{v1}A_{v2}}\left(1 + \frac{A_{v1}A_{v2}R_a}{R_b} + sr_{o1}A_{v2}C_C\right). \tag{8}$$

Z_o is the active load seen from the output node in Fig. 6. It can be expressed as

$$Z_o = C_{pn}//Z_{in}. \tag{9}$$

The above expressions show that the active load Z_{in} effectively acts like an inductive load in the high frequency region. The effective inductance (L_{eff}) of the active load Z_{in} forms a parallel resonance circuit associated with capacitor (C_{pn}) at the output node of OTA. Because in Eq. (8) the value of C_c could be dynamically changed in $C_{c\text{-array}}$, there is also an array of capacitor C_{pn} corresponding to the capacitor C_c. It is possible to extend –3 dB frequency point to a higher region by adjusting the size of capacitor C_{pn} and boosting the gain at high frequency. The simulation result shows that the maximum bandwidth of the single stage amplifier is boosted to 16 MHz from the original 6 MHz, as shown in Fig. 7. Thus the additional smart OTA technique improves effectively the trade-off between bandwidth and power consumption of the VGA. When the bandwidth (power consumption) of the amplifier is fixed, the technique can reduce/increase the power consumption/bandwidth of the amplifier.

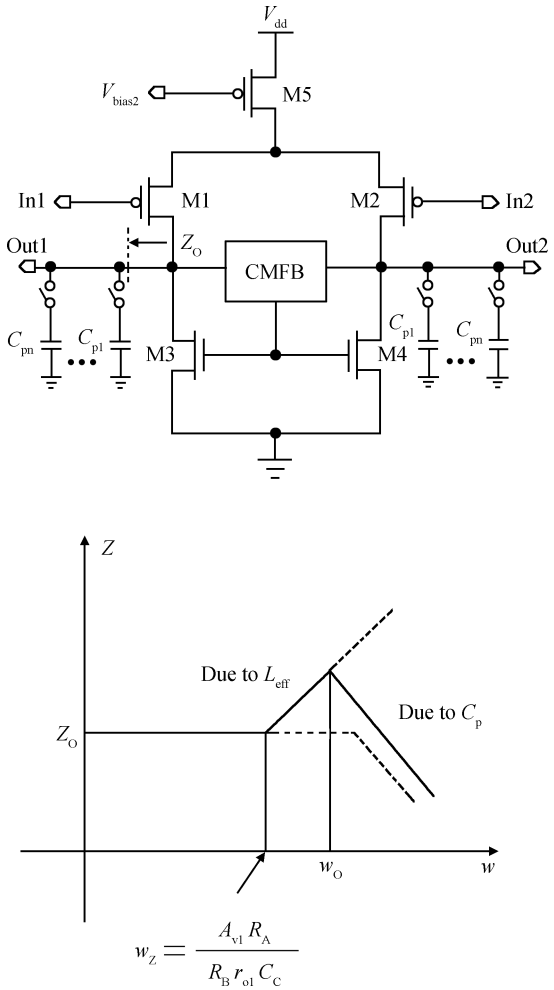

Fig. 6. Circuit structure of OTA and its output impedance.

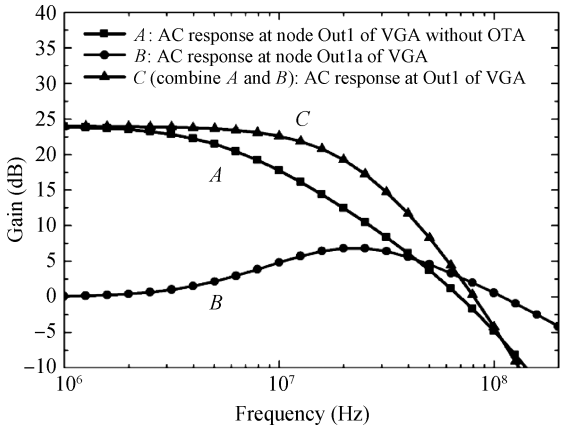

Fig. 7. Effect of bandwidth boosting technique.

3.2. DC offset cancellation circuit

The CTF technique is used to cancel DC offset in the PGA circuit, as shown in Fig. 1. LPF can feedback the DC component in the output voltage of the VGA to its input terminals. The component is subtracted by the circuit from the input signal so that the DC offset voltage can be reduced or canceled. Figure 8 shows the LPF circuit. Resistors are implemented by sub-threshold transistors (MOS-resistors). Cascaded sub-threshold

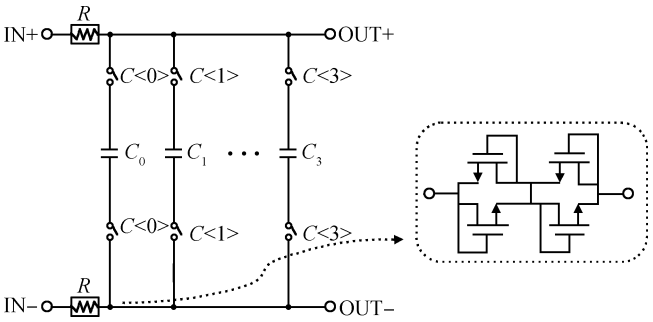

Fig. 8. Structure of the high pass filter and the low pass filter.

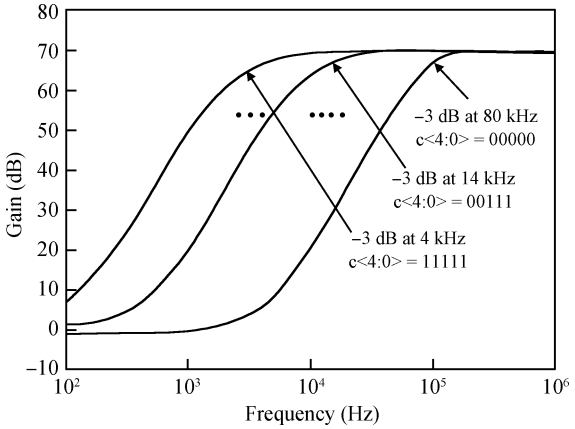

Fig. 9. Frequency responses of the DC offset canceller.

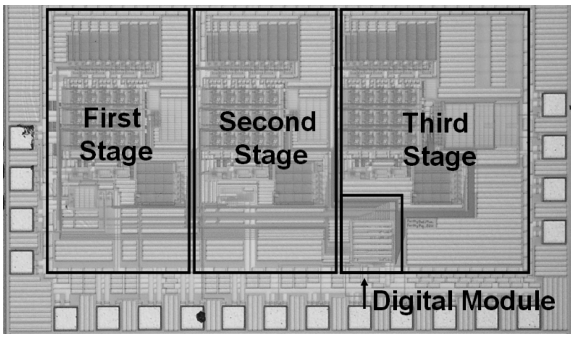

Fig. 10. Microphotography of chip.

transistors[9] minimize distortion at low frequencies. Considering that sub-threshold resistance changes with technology and temperature variations, redundant capacitors and MOS-resistors are implemented in LPF. The cut-off frequency of the CTF technique can be programmed widely. It not only satisfies multistandards, but also ensures that the receiving signal settles down quickly through switching the cut-off frequency from high to low. The simulated frequency responses of the DC offset cancellation circuit are illustrated in Fig. 9. It shows that the effective cut-off frequency can be programmed from 4 to 80 kHz by changing the value of capacitance. It provides a roll off rate about 60 dB per decade to reduce DC offset.

Table 2. Comparison of PGA performance.

Parameter	Ref. [10]	Ref. [5]	Ref. [2]	This work
Technology (μm)	0.35	0.18	0.13	0.13
Voltage (V)	3	1.8	1.2	1.2
Power (mA)	13	1.35	0.3–11.2	0.85–3.2
Gain range (dB)	–8 to 80	–10 to 20	0 to 39	–5 to 60
Bandwidth (MHz)	112	30	0.18–200	1–10
OIP3 (dBm)	11.5	29	NA	14

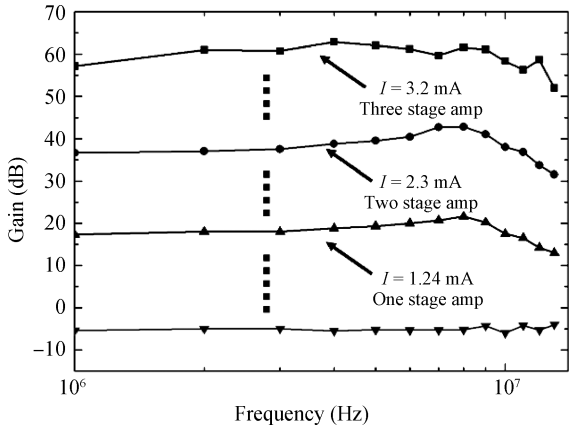

Fig. 11. Frequency responses of the PGA.

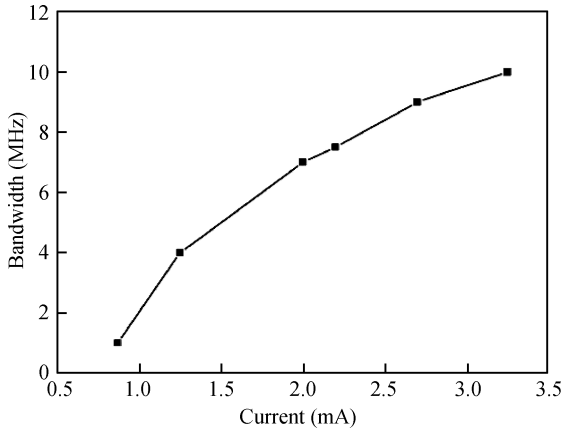

Fig. 13. Programmable bandwidth of the PGA.

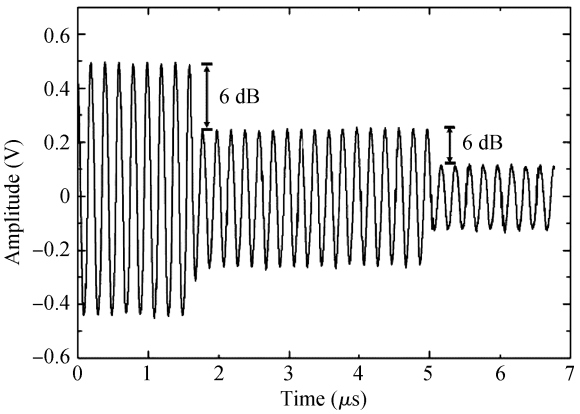

Fig. 12. Output signal of the PGA with 6 dB step change.

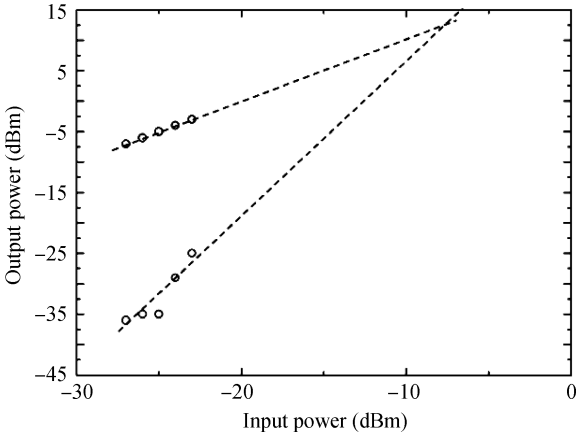

Fig. 14. Measured in-band OIP3 result.

4. Experimental results

The flexible PGA is implemented in 0.13 μm CMOS technology. Its chip microphotography is shown in Fig. 10. The chip area is about 1 mm^2. Figure 11 shows the gain and the bandwidth of the three-stage PGA. The gain could be digitally programmed from –5 to 60 dB in a 2 dB step minimally. Figure 12 shows the output signal of PGA changes with time in 6 dB step, and the switching time is less than 100 ns. The PGA also provides a bandwidth tuning range between 1 and 10 MHz, while the corresponding current consumption ranges from minimally 850 μA to maximally 3.2 mA (Fig. 13). Figure 14 shows the in-band OIP3 result for a two-tone signal (at 6 and 7 MHz). This corresponds to 14 dBm in-band OIP3. Table 2 shows the test results of the PGA and makes some comparisons with other papers.

5. Conclusion

We presented an efficient solution to design programmable gain amplifier circuits, in which we mainly utilize a new bandwidth boost technique to reduce the power consumption. The PGA chip with an area of 1 mm^2 implemented in a 130-nm standard CMOS process demonstrated our proposal. Both its gain and bandwidth could be programmed. Moreover, the design has built-in DC-offset correction based on using subthreshold transistors as a resistor.

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