Substrate-bias effect on the breakdown characteristic in a new silicon high-voltage device structure*

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Abstract: A novel silicon double-RESURF LDMOS structure with an improved breakdown characteristic by substrate bias technology (SB) is reported. The P-type epitaxial layer is embedded between an N-type drift region and an N-type substrate to block the conduction path in the off-state and change the distributions of the bulk electric field. The substrate bias strengthens the charge share effect of the drift region near the source, and the vertical electric field peak under the drain is decreased, which is especially helpful in improving the vertical breakdown voltage in a lateral power device with a thin drift region. The numerical results by MEDICI indicate that the breakdown voltage of the proposed device is increased by 97% compared with a conventional LDMOS, while maintaining a low on-resistance.

Key words: substrate bias; breakdown voltage; diode; on-resistance
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1. Introduction

Power integrated circuits typically combine devices such as a lateral double diffused MOS transistor (LDMOS) with control circuits on the same chip. The drift region of an LDMOS transistor, which supports high voltages, is realized through the implementation of a reduced surface field (RESURF) principle[1, 2]. Double RESURF is one of the most utilized methods in designing a high voltage device with a low on-resistance. The breakdown voltage (BV) is determined by the lesser one of the lateral BV and the vertical BV, thus optimizing electronic field distributions and enhancing breakdown characteristics are the way to achieve a higher BV. In order to be feasibly isolated from low-voltage devices, LDMOS needs a thin drift region, so the vertical BV is the critical element limiting the device's blocking capability[3−6]. Recently, Cheng has proposed and optimized the use of a floating buried layer in the substrate, and the vertical BV is increased thanks to an increase in the depletion layer in the substrate[7]. Duan has designed the reduced the bulk field device with an N^+-floating layer embedded in the high-resistance substrate, which caused a redistribution of the bulk electric field in the drift region and the substrate supported more bias[8]. The back-gate is an effective technology to improve vertical breakdown behaviour, but is only used in silicon-on-insulator (SOI) devices because a vertical conduction path exists in the silicon device in the off-state[9−11].

In this work, a novel silicon high-voltage double-RESURF LDMOS structure with improved BV characteristics and on-resistance due to a substrate bias is proposed. When a positive substrate voltage is applied, the vertical junction formed by the epitaxial layer and the substrate is reverse biased, which changes the bulk electric field distribution and makes the depletion under the source sustain more potential. The dependence of the BV on the substrate bias is discussed. Also, double-RESURF is adopted to obtain uniform surface electric field and lower on-resistance.

2. Device structure

Figure 1 shows the schematic cross-section of the proposed SB double-RESURF LDMOS and conventional LDMOS. For SB double-RESURF LDMOS in Fig. 1(a), there is a P-type epitaxial layer between the N-type substrate and drift region, which is distinguished from the conventional device structure in Fig. 1(b). L_d, t_d and N_d are the length, thickness and doping concentration of the drift region, respectively. Two connected back-to-back diodes D1 and D2 are formed by the substrate, P-type epitaxial layer and drift region. V_{sub} and V_D are the voltages applied to the substrate and the drain, respectively. When D2 is reversely biased by positive V_{sub}, the voltage sustained by D1 under drain decreased, and part of V_D is supported by the junctions of D1 and D2 under the source. The modulation of bulk electric field by V_{sub} results in the improvement of vertical BV, which is especially important to a power device with a thin drift region. A P-top region is introduced at the surface to increase the optimal N_d and decrease the on-resistance of the device, whose effect is similar to the counterpart of the conventional double RESURF device[2], and P_t and t_t are the doping concentration and thickness of P-top region, respectively. The N-type substrate doping concentration is N_{sub}. P_{se} and t_{se} are the P-type epitaxial layer doping concentration and thickness, respectively. The P-top region at the surface and the P-type epitaxial layer in the substrate are not in electrical contact and are floating in potential. The substrate bias is lower than the

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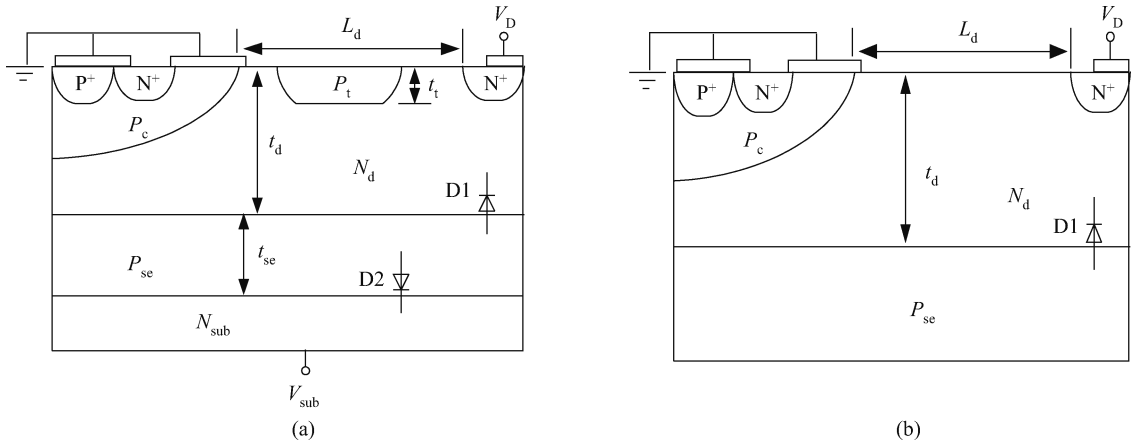

Fig. 1. Cross-section of (a) SB double RESURF LDMOS and (b) conventional LDMOS.

drain bias, so in a practical application, the substrate bias can be obtained from the drain bias by resistors in series.

3. Results and discussions

The results are obtained by a semiconductor simulator MEDICI using physical models of "IMPACT.I", "CONMOB", "AUGER", "FLDMOB" and "BGN" mainly. The NEWTON solution method is used with two types of carriers and the parameters of DAMPED and ICCG. Figures 2(a) and 2(b) show potential contour distributions at breakdown of the SB double RESURF LDMOS and optimal conventional LDMOS with the same length of drift region and substrate concentration, and the drift region is doped according to the RESURF principle to achieve a maximum BV. The depletion region mainly extended under the drain and equal-potential contours crowded around the drain. The BV of conventional LDMOS is limited to 385 V due to electric field crowding at the drain. When a positive substrate bias $V_{sub} = 750$ V is applied in SB double RESURF LDMOS, the equal-potential lines are evenly spaced and distribute more under the source electrode and the thickness of the depletion region in the substrate is increased significantly. The junction between the P-type epitaxial layer and the N-type substrate is fully depleted like a parallel planar junction. Figure 2(c) shows the surface electric field distributions. It is clear that a new electric field peak is brought in SB double RESURF LDMOS due to the electric field modulation effect by a P-top region in comparison to conventional LDMOS. This new field peak rises with the increase of the substrate bias and pulls down the height of the electric field peak near the drain. The potential of SB double RESURF is distributed linearly across most of the drift region, but the potential distribution of conventional LDMOS shows a large curvature in the whole drift region, leading to a non-uniform surface field profile that may cause a degradation of the breakdown voltage. The vertical electric field and potential distributions near the drain $x = 68$ μm is shown in Fig. 2(d). There is only one electric field peak and the drain bias is sustained completely by D1 for conventional LDMOS. There is one more triangle-shaped electric field peak at the D2 in SB double RESURF LDMOS, and the drain bias is sustained by two junctions of D1 and D2. Though the drain biases of the SB double RESURF LDMOS are much larger than that of conventional LDMOS, the maximum electric field under the drain is almost the same for both devices. The vertical electric field and potential distributions near the source $x = 21$ μm is shown in Fig. 2(e). There are two electric peaks in SB double RESURF LDMOS and the strength and the area of electric field distribution under the source are much larger than that of conventional LDMOS, which results from the depletion layer spreading into the source region. A large portion of reverse drain bias is sustained by D2 under the source and this is why the breakdown voltage of SB double RESURF LDMOS is higher than that of a conventional device. The BV of SB double RESURF LDMOS reaches 760 V compared with 385 V of conventional LDMOS.

The breakdown voltage as a function of the substrate bias V_{sub} for different P-type epitaxial layer thickness t_{se} is shown in Fig. 3(a). Maximal breakdown voltage and the optimal V_{sub} values increase with an increase in t_{se} due to the charge share effect of the drift region. The breakdown voltage has a clear optimum. For higher V_{sub}, the drift region cannot be depleted fully and thus a premature breakdown happened, so the breakdown voltage is smaller. In general, the lower the P_{se} or the larger the t_{se}, the higher the breakdown voltage. The dependence of BV on N_d concentration and V_{sub} are illustrated in Figs. 3(b) and 3(c). V_{sub} has an optimum for different N_d when the RESURF condition is satisfied. V_{sub} weakens the charge share effect of the drift region by P-type epitaxial layer, thus the optimum V_{sub} increases with a decrease in N_d. The higher the V_{sub}, the more the voltage is sustained by D2, thus the maximum BV increases with a decrease in N_d. The influence of t_d on the BV is shown in Fig. 3(d). The optimum N_d increases with a decrease in t_d.

Figure 4(a) shows the dependences of breakdown voltages and on-resistance on concentrations of the drift region in conventional LDMOS and SB double RESURF LDMOS. The concentration of the drift region has an optimum for each structure. However, the optimum N_d of SB double RESURF LDMOS is much higher than that of a conventional device thanks to the auxiliary depletion effect by substrate bias, which causes the on-resistance of SB double RESURF device to be reduced in comparison to conventional LDMOS, and the BV is improved by 97%. Breakdown voltages as a function of drift region length are shown in Fig. 4(b). It is apparent that the curve is characterized by both the linear and saturation regions. The longer the drift region length, the higher the BV will be, and

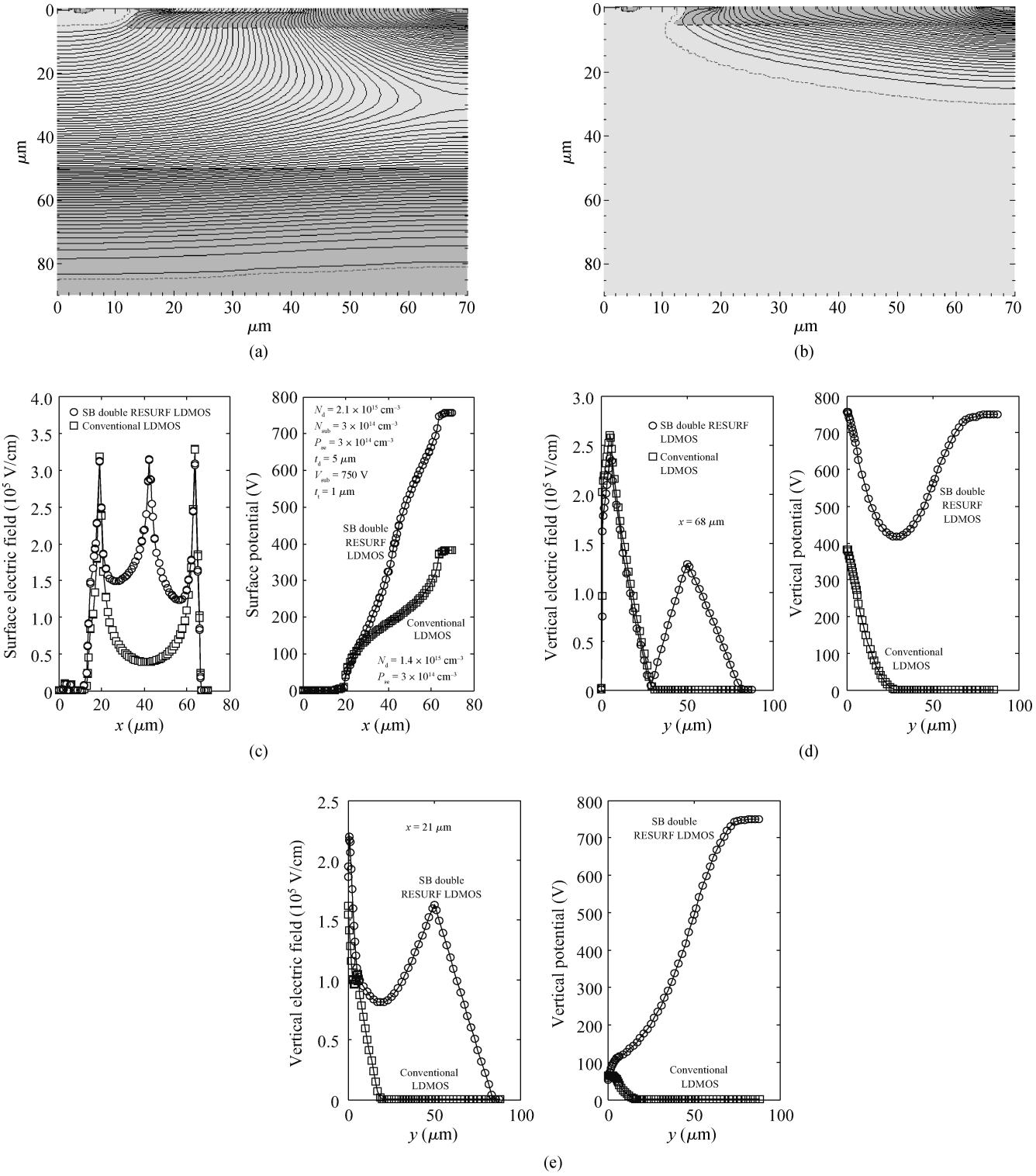

Fig. 2. Potential distribution of (a) SB double RESURF LDMOS (BV = 760 V) and (b) conventional LDMOS (BV = 385 V). The electric field and potential distributions (c) along the surface, (d) along the vertical direction near drain $x = 68$ μm, and (e) along the vertical direction near source $x = 21$ μm.

BV would also saturate due to the saturation of the vertical BV. Saturated BV increases with a decrease in substrate doping concentration and an increase in t_{se}.

4. Conclusion

A novel thin drift region power MOSFET with a diode embedded in a substrate has been designed. It combines the features that are helpful to isolation technology and are beneficial to a high-breakdown voltage due to the electric field modulation effect by substrate bias. Simulation results have shown that a higher breakdown voltage and impurity concentrations are obtained than those in conventional LDMOS resulting from transfer of the drain bias and enhancement of charge sharing in

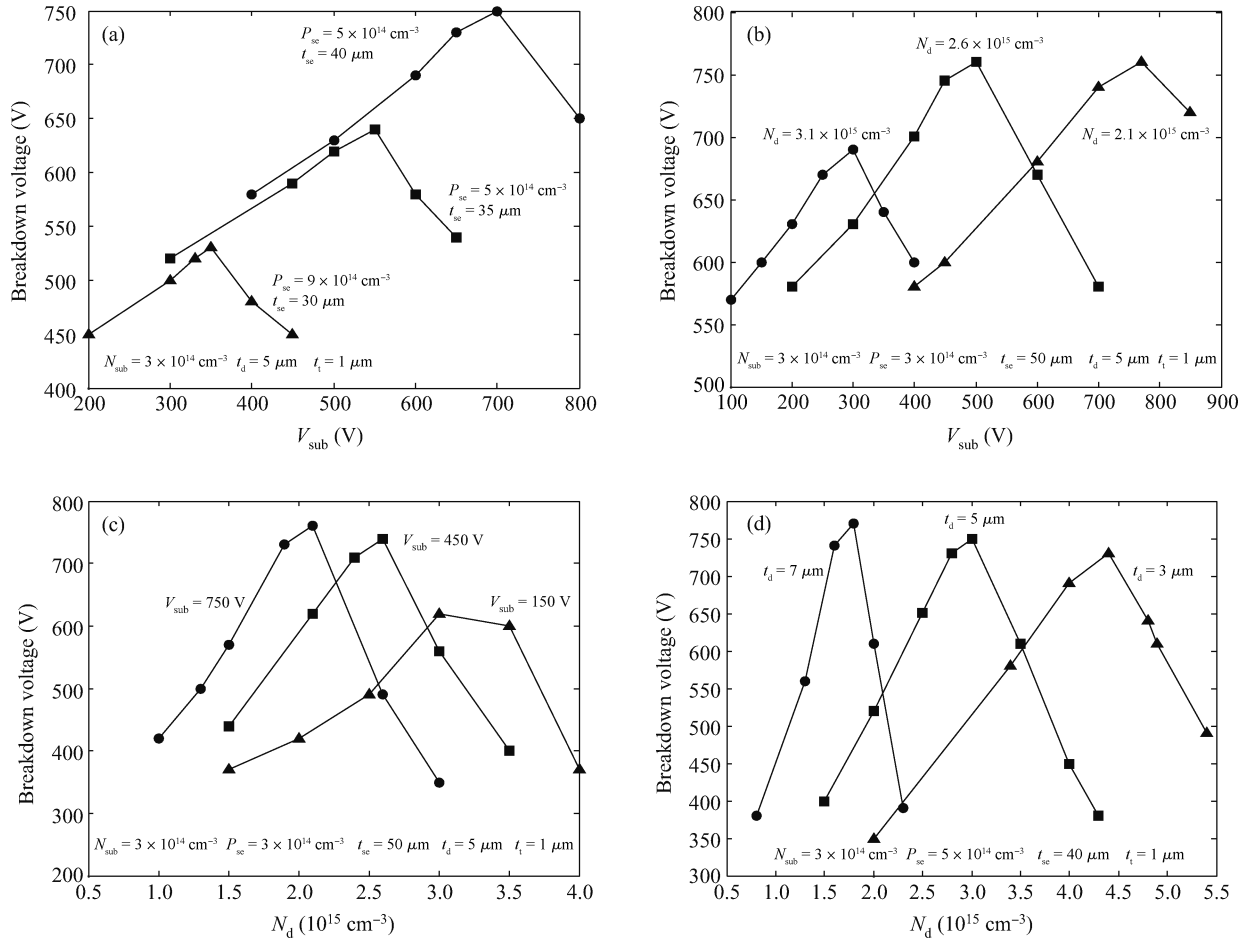

Fig. 3. Breakdown voltage as a function of (a) V_{sub} with different t_{se}, (b) V_{sub} with different N_d, (c) N_d with different V_{sub}, and (d) N_d with different t_d.

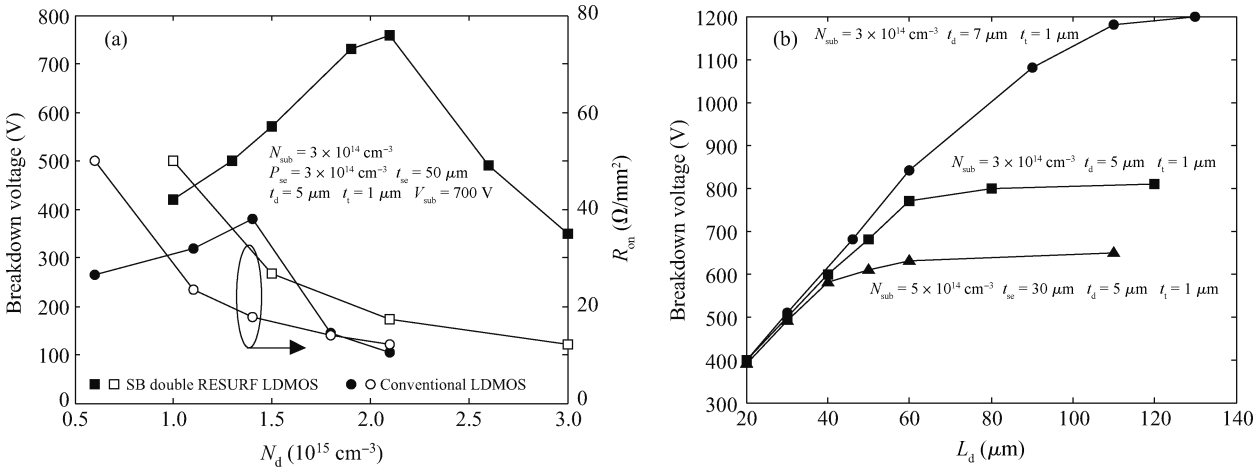

Fig. 4. Breakdown voltage and on-resistance as a function of (a) N_d and (b) L_d.

the drift region, respectively.

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