Novel SOI double-gate MOSFET with a P-type buried layer*

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Abstract: An ultra-low specific on-resistance ($R_{on,sp}$) integrated silicon-on-insulator (SOI) double-gate triple RESURF (reduced surface field) n-type MOSFET (DG T-RESURF) is proposed. The MOSFET features two structures: an integrated double gates structure (DG) that combines a planar gate with an extended trench gate, and a p-type buried layer (BP) in the n-type drift region. First, the DG forms dual conduction channels and shortens the forward current path, so reducing $R_{on,sp}$. The DG works as a vertical field plate to improve the breakdown voltage (BV) characteristics. Second, the BP forms a triple RESURF structure (T-RESURF), which not only increases the drift doping concentration but also modulates the electric field. This results in a reduced $R_{on,sp}$ and an improved BV. Third, the extended trench gate and the BP linked with the p-body region reduce the sensitivity of the BV to position of the BP. The BV of 325 V and $R_{on,sp}$ of 8.6 m$\Omega\cdot$cm^2 are obtained for the DG T-RESURF by simulation. $R_{on,sp}$ of DG T-RESURF is decreased by 63.4% in comparison with a planar-gate single RESURF MOSFET (PG S-RESURF), and the BV is increased by 9.8%.

Key words: SOI; double gates; specific on-resistance; RESURF; breakdown voltage
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1. Introduction

SOI technology has been widely concerned owing to its high-speed, low power loss and superior isolation[1−3]. In a conventional single RESURF[4, 5] MOSFET, the current path is restricted to the device surface, which hampers it from further reducing $R_{on,sp}$ and results in a Si-limit as $R_{on} \propto BV^{2.5}$. Trench gate MOSFETs have successfully demonstrated a further reduction in $R_{on,sp}$ by increasing the channel density and spreading the current into the bulk of the device[6−8].

A planar gate bulk Si MOSFET with a buried layer in the drift region is proposed[9], which can decrease $R_{on,sp}$[10, 11]. However, if the idea is used in an SOI MOSFET directly, i.e. a planar-gate triple RESURF SOI MOSFET (PG T-RESURF), the main problem we encounter is the sensitivity of the BV to the position of the BP. To address the issue, DG T-RESURF based on SOI technology is proposed in this work. The blocking characteristics, on-state characteristics and thermal characteristics are researched by simulation. Moreover, compared with the properties of PG S-RESURF, $R_{on,sp}$ reduces by 14.9 m$\Omega\cdot$cm^2, the BV increases by 29 V, and the maximal junction temperature (T_{jmax}) decreases by 17.5 K.

2. Structure and mechanism

Figure 1 shows the schematic cross sections of DG T-RESURF, PG T-RESURF, and PG S-RESURF, respectively. A p-type buried layer is placed in the drift region in Figs. 1(a) and 1(b). T_{bp} and L_{bp} represent the thickness and length of the BP, respectively. D_1 is the distance from the surface to the top interface of the BP. D_2 is the distance from the left end of the BP to the left border of the device for PG T-RESURF. Lateral field plate technology is used in all structures. These structures have the identical thicknesses of top silicon ($T_{si} = 6\ \mu$m) and buried oxide layer ($T_{ox} = 2\ \mu$m), and length of drift region ($L_d = 18.6\ \mu$m) as well. Other parameters take their own optimum values.

Although the BP structure takes up the conduction area of the drift region in the on-state, the optimal drift region concentrations of DG T-RESURF and PG T-RESURF are about triple that of PG S-RESURF in theory[9, 10]. The p-body, n-type drift region and p-type buried layer form two adjacent PN junctions in PG T-RESURF, as shown in Fig. 1(b). In the blocking state, two adjacent PN junctions and the planar gate field plate result in premature breakdown at point A near the p-body region if the theoretical drift region concentration is kept. The BV of PG T-RESURF is very sensitive to the position of the BP. Therefore, an optimized drift region concentration should decrease in order to keep a high BV, which limits the decrease in the $R_{on,sp}$.

In DG T-RESURF, the combination of double gates and a BP structure can solve the problems mentioned above. The extended trench gate is like a vertical field plate, which releases the high electric field at the edge of the p-body region. The

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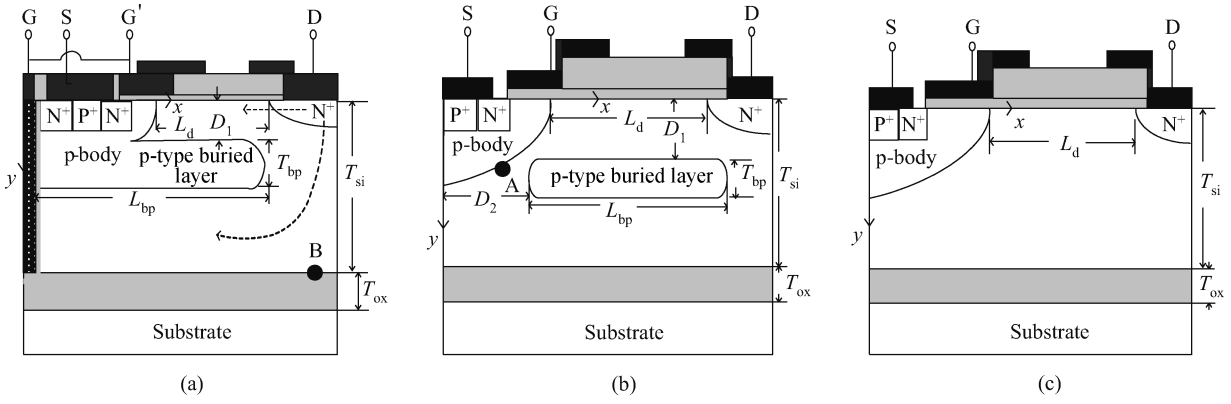

Fig. 1. Schematic cross section of (a) DG T-RESURF (proposed), (b) PG T-RESURF, and (c) PG S-RESURF.

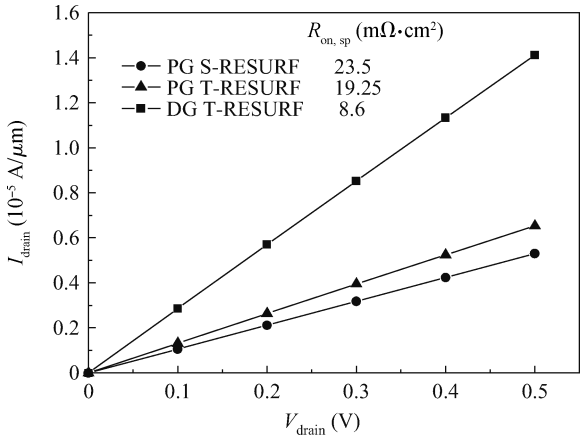

Fig. 2. I_{drain}–V_{drain} curve at $V_{GS} = 15$ V for PG S-RESURF, PG T-RESURF and DG T-RESURF.

BP and p-body region are linked together to further reduce the sensitivity of the BV on the location of the BP. In the on-state, part of the current from the surface channel of the planar gate flows through the n-drift region above the BP, and the rest of the current from the vertical channel of the trench gate flows through the n-drift region below the BP, which extends the conduction region and shortens the current path. Therefore, the $R_{on, sp}$ is further reduced. Moreover, the new structure can be easily isolated because the trench gate can be used as an isolation trench between the high-voltage device and low-voltage circuitry, which reduces the complexity and cost of the isolation process.

3. Results and discussion

The on-state output characteristic at a low drain voltage is shown in Fig. 2. It can be seen that the $R_{on, sp}$ of DG T-RESURF is the smallest. Compared with PG S-RESURF and PG T-RESURF, the $R_{on, sp}$ of 8.6 mΩ·cm^2 for DG T-RESURF is reduced by 63.4% and 55.3%, respectively. The reduction of $R_{on, sp}$ in DG T-RESURF is due to the increased doping concentration of the drift region, dual conduction channels, and shortened forward current path. Two-dimensional current line distributions for three structures are given in Fig. 3, which also demonstrates the same as the results in Fig. 2.

Figure 4(a) gives the optimal surface electric field, which reflects the lateral BV characteristics. The lateral electric field distribution in DG T-RESURF is more uniform than those of the other devices, and the middle electric field peaks are raised while the electric field peaks at the source/drain sides are reduced. Figure 4(b) shows the optimal vertical electric field distributions in the y-direction under the drain regions, which reflects the vertical BV characteristics. In DG T-RESURF, the electric field peak Q_2 on the interface of Si/buried oxide layer increases, and the electric field peak Q_1 near the drain region decreases. This causes the breakdown point to shift from the surface in PG S-RESURF to point B in DG T-RESURF, as shown in Fig. 1(a). The BV value is determined by a smaller value between the lateral BV and the vertical BV, so the proposed DG T-RESURF can obtain the largest BV. The BP in the drift region works as a T-RESURF structure and the trench gate is like a vertical field plate. The two structures modulate and reshape the electric field distribution so improving the BV characteristics. The reverse I–V characteristics curve for the three structures are given in Fig. 5, in which the BV value of DG T-RESURF increases by 9.8% as compared with that of PG S-RESURF.

For the three types of SOI devices shown in Fig. 1, maximal junction temperatures (T_{jmax}) occur in the surfaces by simulation. Temperature distributions in the surface are given in Fig. 6. It can be seen that the surface temperature of DG T-RESURF is the smallest. Compared with PG S-RESURF and PG T-RESURF, T_{jmax} of 308 K for DG T-RESURF is reduced by 17.5 K and 21.7 K, respectively. The value of T_{jmax} is mainly influenced by the power loss, the thermal resistance, and the distribution of the on-state current. The reduction of T_{jmax} in DG T-RESURF is mainly due to the decreased on-state power loss, and the increased uniformity of the on-state current distribution.

The influence of D_1 and D_2 on the BV and $R_{on, sp}$ for DG T-RESURF and PG T-RESURF are shown in Fig. 7, where L_{bp} remains 22 μm and T_{bp} remains 1 μm. For DG T-RESURF, the values of the BV and $R_{on, sp}$ keep almost constant. For PG T-RESURF, $R_{on, sp}$ drops as D_1 increases because more current lines flow via the planar gate with a shorter current path, while the BV almost remains constant; As D_2 increases, the BV falls significantly, wherein premature breakdown happens at point A near the p-body region, while $R_{on, sp}$ decreases because more

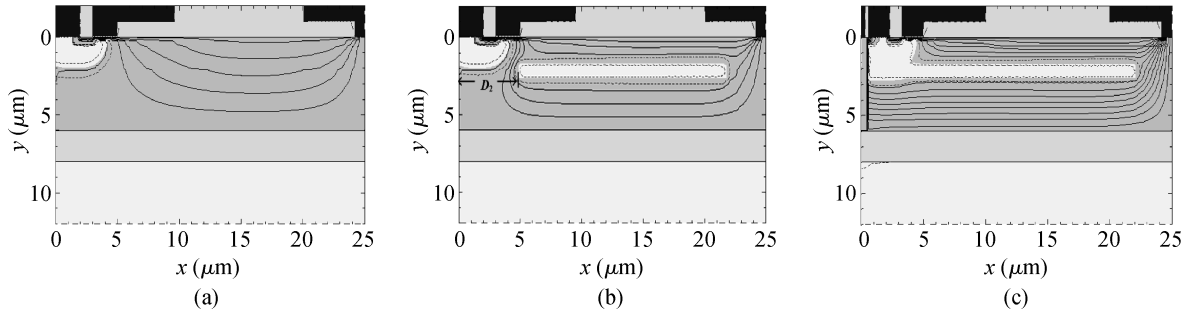

Fig. 3. Two-dimensional current line contours for (a) PG S-RESURF, (b) PG T-RESURF and (c) DG T-RESURF (1×10^{-6} A·μm^{-1}/contour and $V_{GS} = 15$ V, $V_{drain} = 0.5$ V).

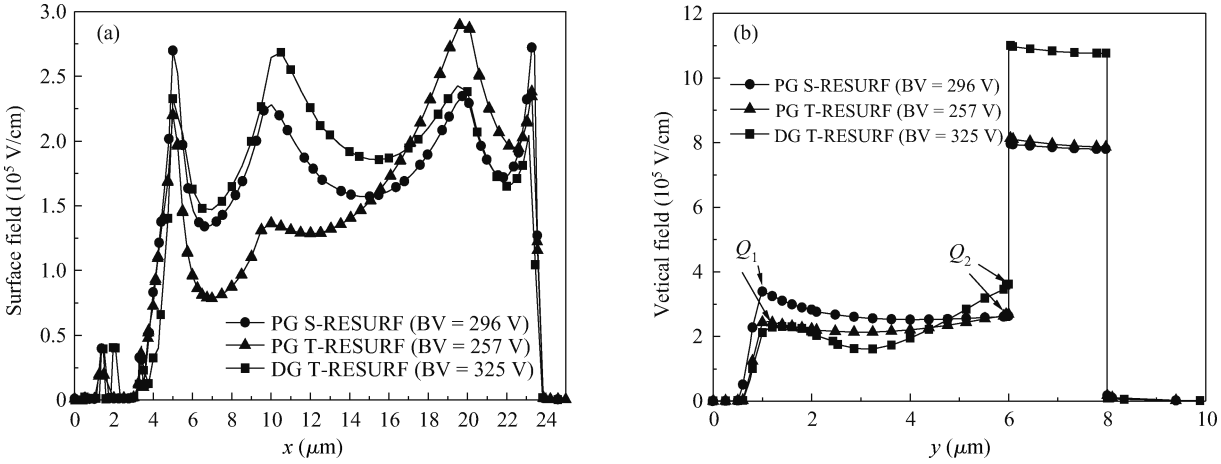

Fig. 4. Field distributions in the (a) surface and (b) y-direction under the drain ($T_{si} = 6$ μm, $T_{ox} = 2$ μm, $L_d = 18.6$ μm).

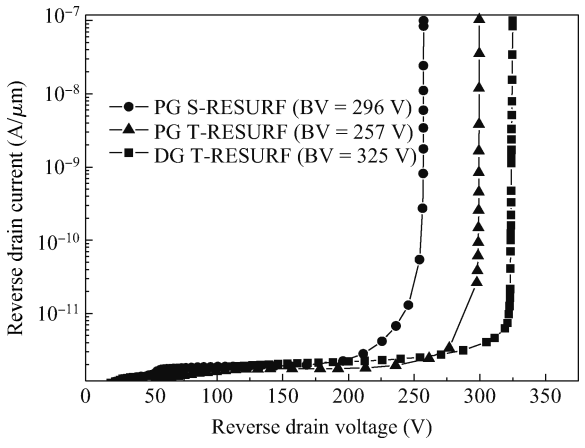

Fig. 5. Reverse I–V characteristics curve at $V_{GS} = 0$ V for PG S-RESURF, PG T-RESURF and DG T-RESURF.

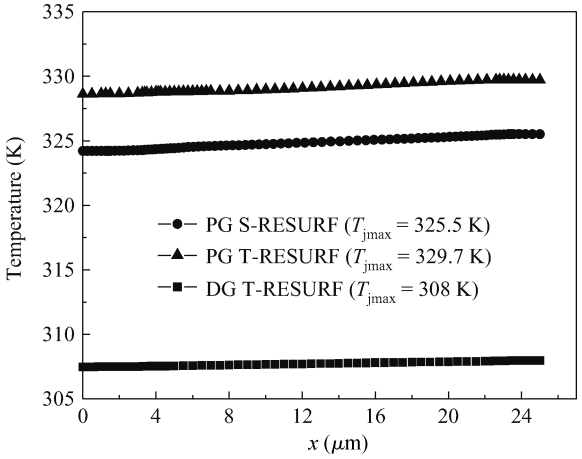

Fig. 6. Temperature distributions in the surface for PG S-RESURF, PG T-RESURF and DG T-RESURF ($V_{GS} = 15$ V and $I_d = 5 \times 10^{-5}$ A/μm).

current lines can flow through the n-drift region below the BP and then via the planar gate channel. So, the problem that the BV is sensitive to the position of the BP (the problem encountered in PG T-RESURF) can be solved in DG T-RESURF.

Figure 8 shows influences of L_{bp} and T_{bp} on the BV and $R_{on,sp}$ for DG T-RESURF. The BV rises as L_{bp} increases and T_{bp} decreases, due to the enhanced modulation effect of the BP; $R_{on,sp}$ also rises with the increasing L_{bp} and T_{bp} values because the current path is narrowed.

The values of the half-cell pitch, L_d, BV, $R_{on,sp}$, T_{jmax}, and FOM (figure of merit, FOM = BV^2/$R_{on,sp}$) for DG T-RESURF, PG T-RESURF, PG S-RESURF are given in Table 1. Compared with the properties of other structures, $R_{on,sp}$ of DG T-RESURF is the smallest, the BV is the largest and the FOM is the highest, due to the influence of the DG and BP structures. T_{jmax} decreases by 17.5 K and 21.7 K by comparison with PG S-RESURF and PG T-RESURF, which is because DG

Table 1. BV, T_{jmax} and $R_{on,sp}$ for the three structures (Note: $R_{on,sp}$ at $V_{GS} = 15$ V).

Device type	Half-cell pitch (μm)	L_d (μm)	BV (V)	$R_{on,sp}$ (m$\Omega\cdot$cm^2)	FOM (MW/cm^2)	T_{jmax} (K) ($I_d = 5\times10^{-5}$A/μm)
DG T-RESURF	25	18.6	325	8.6	12.3	308
PG S-RESURF	25	18.6	296	23.5	3.73	325.5
PG T-RESURF	25	18.6	257	19.25	3.43	329.7

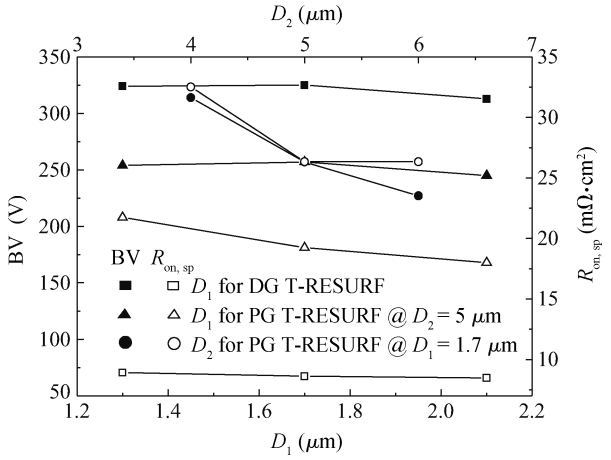

Fig. 7. Dependences of the BV and $R_{on,sp}$ on D_1 and D_2 for DG T-RESURF and PG T-RESURF ($L_{bp} = 22$ μm, $T_{bp} = 1$ μm).

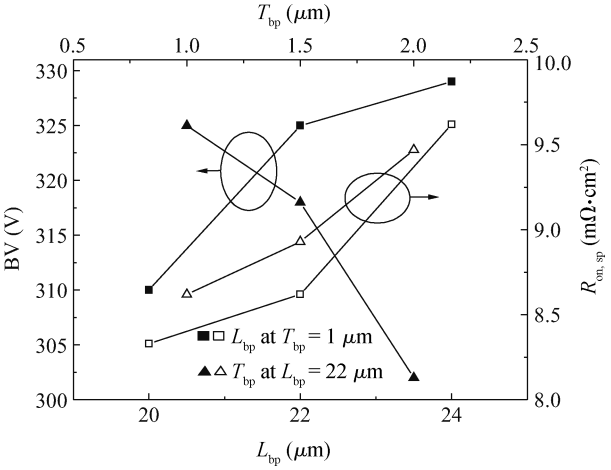

Fig. 8. Dependences of the BV and $R_{on,sp}$ on L_{bp} and T_{bp} for DG T-RESURF ($D_1 = 1.7$ μm).

T-RESURF has lower $R_{on,sp}$ and more uniform current distribution.

4. Conclusion

In this work, a novel SOI double-gate MOSFET with a p-type buried layer is proposed, in which a higher BV, lower $R_{on,sp}$, and smaller T_{jmax} can be obtained. Moreover, the new structure is easily isolated, and the BV is not sensitive to the position of the BP. These advantages make the new structure have good prospects in the field of low power loss.

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