Failure mechanisms and assembly-process-based solution of FCBGA high lead C4 bump non-wetting*

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Abstract: This paper studies the typical failure modes and failure mechanisms of non-wetting in an FCBGA (flip chip ball grid array) assembly. We have identified that the residual lead and tin oxide layer on the surface of the die bumps as the primary contributor to non-wetting between die bumps and substrate bumps during the chip-attach reflow process. Experiments with bump reflow parameters revealed that an optimized reflow dwell time and H_2 flow rate in the reflow oven can significantly reduce the amount of lead and tin oxides on the surface of the die bumps, thereby reducing the non-wetting failure rate by about 90%. Both failure analysis results and mass production data validate the non-wetting failure mechanisms identified by this study. As a result of the reflow process optimization, the failure rate associated with non-wetting is significantly reduced, which further saves manufacturing cost and increases capacity utilization.

Key words: non-wetting; C4 bump; bump reflow; FCBGA
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1. Introduction

Flip chip (FC) packaging technology has been widely used in semiconductor packaging assembly for high-speed, high I/O count and high-performance ICs. It offers the unique advantages of high density routing, high electrical performance, and cost savings over wire bonding for high I/O ICs. Flip chip packaging has found wide-spread applications for high speed devices, such as CPU, chipset and high-speed networking and telecommunication chips. It is believed that FC technology is also becoming a mainstream assembly technology as silicon technology advances beyond 45 nm and as the cost of FC constantly lowers. At present, two similar FCBGA (flip chip ball grid array) processes are widely applied in the semiconductor manufacturing field. The major difference between the two processes is that one requires printing eutectic solder paste on a substrate bump pad before the chip-attach process, while another needs flux printing at the substrate bump area. The flux printing based FCBGA process is sensitive to flux thickness and flux coverage of the substrate bump area. Less flux or inadequate flux coverage will cause open failure, and too much flux will result in a die float problem at the chip-attach reflow stage. A solder paste printing based process has been extensively used for low I/O ICs and devices for the consumer market; and the flux printing based process dominates high I/O and fine bump pitch IC assembly because it does not change the bump volume and can successfully avoid the bump bridge problem that is seen in another FCBGA process. Figure 1 illustrates the cross-sectional view of an FCBGA package structure at the chip-attach stage, which is flux printing process based.

Before starting the chip-attach stage, wafers with high lead (Pb95%/Sn5%) C4 (control collapse chip connection) bumps have to go through a bump-reflow process first so as to reduce or remove the oxides on the bump surface as well as to make all of the bumps a regular spherical shape with the same height. Figure 2 provides the bump reflow thermal profile and schematically shows the C4 bump structure and bump shape change before and after the bump-reflow process. Here, the peak temperature and dwell time of the standard profile are 398 ℃ and 1100 s, respectively, and the H_2 flow rate is 5 cu.ft/s. As a result of the bump reflow, all mushroom-like bumps are changed into spherical bumps in H_2 ambient with the thermal profile.

At chip-attach, flux will be printed on the substrate bump area first and then die is attached onto the substrate with very fine alignment control, then the die and substrate go through the chip-attach reflow oven together, where high lead C4 bumps and eutectic substrate bumps form solder joints under the defined thermal profile with the presence of flux. With the reflow profile shown in Fig. 3, Senju sparkle flux 385 becomes active so that can further remove oxides at the bump surface and help

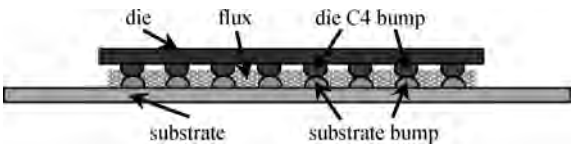

Fig. 1. Cross-sectional view of FCBGA package at chip-attach stage.

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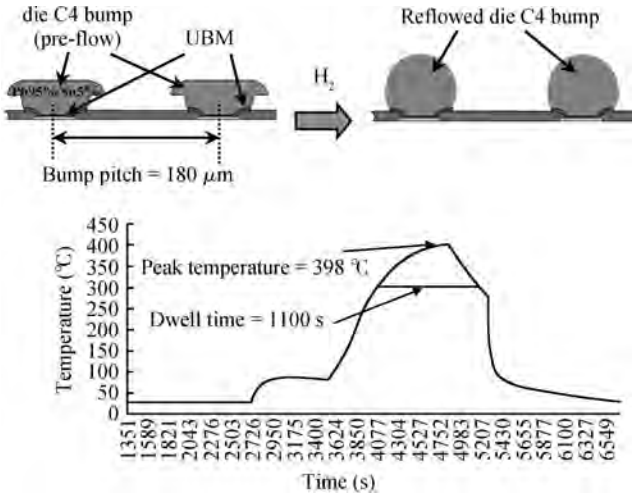

Fig. 2. Die C4 bump structure, shape change and bump-reflow thermal profile.

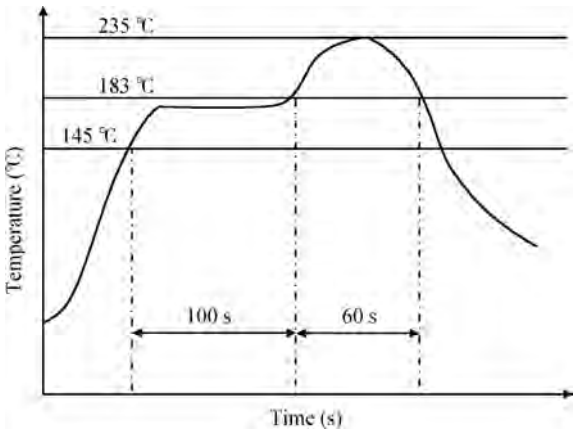

Fig. 3. Chip-attach reflow thermal profile.

to form a solder joint between die bumps and substrate bumps.

It is apparent that FC solder joints are much shorter than conventional wire bond assemblies. Despite the many advantages of FC technology, there are some issues associated with the manufacture of FC assemblies. One major defect encountered in FC assembly is the improper solder joint between die C4 bumps and substrate bumps, which causes a high open failure rate and potential reliability problems[1].

High assembly yield loss due to the non-wetting of C4 bumps is a fairly common issue in many FC assembly factories. As an example, the open failure rate can increase by more than ten times when converting from a QFP (quad flat package) package to an FCBGA package for the same device. Some companies mandate the scrap of an entire batch when its open failure rate exceeds a prescribed level to prevent the risk of disastrous reliability failures in field application. Therefore, non-wetting in an FC reflow process not only results in direct product and production time waste, but also impairs the quality and reliability of the FCBGA products. A better insight into the failure mode and mechanism of non-wetting in FC reflow is very important for FC assembly yield enhancement, cost reduction and quality improvement.

2. Theoretical background and experimental methods

C4 bumps on the die are the primary subject in this study. Specifically, the material composition and structure at the C4 bump surface are analyzed by using multiple methods to the determine factors that influence non-wetting and the failure mechanism associated with them. In addition to optical visual inspection, SEM (scanning electron microscopy) was used to study the details of the non-wetting interface and the C4 bump surface before and after the bump-reflow process; EDX (energy dispersive X-ray) was used to analyze the chemical composition of the C4 bump surface; and the stoichiometry of the bump surface chemicals was quantified by micro-Raman spectroscopy.

The analytical results revealed a layer of lead and tin oxides on the C4 bump surface that plays a critical role in hindering the formation of good solder joints between C4 and substrate bumps during the chip-attach reflow process. C4 bump reflow is part of the flip chip assembly front end process, and its purpose is to reduce or remove the oxides on the bump surface, protect the molten solder from re-oxidation so that good solder joints can be formed with the bumps on the substrates during the chip-attach reflow process. These are achieved through a carefully designed thermal reflow profile and the use of H_2 atmosphere. In the case of high lead solder (Pb95%/Sn5%) C4 bumps, the reduction reaction of lead and tin oxides during bump reflow can be written as below:

$$\mathrm{Pb}_x\mathrm{Sn}_y\mathrm{O}_z + z\mathrm{H}_2 \rightarrow x\mathrm{Pb} + y\mathrm{Sn} + z\mathrm{H}_2\mathrm{O}. \qquad (1)$$

In a mass production environment, there always exists a probability that the lead and tin oxides on C4 bumps cannot be completely reduced/removed during bump-reflow. This is the case for various reasons, such as excessive oxides on the C4 bump surface or improper process parameter settings. Therefore, it is very beneficial to develop an effective method to reinforce the complete reduction/removal of the surface oxide layer at bump-reflow. In this study, the influence of some key process parameters of both bump-reflow and chip-attach processes on the properties of lead and tin oxides are studied. H_2 flow rate in the reflow oven and dwell time are identified as two major process parameters that affect the lead and tin oxide reduction/removal. A 9-leg DOE (design of experiment) was conducted centered around the standard settings. Based on the DOE results, new optimal parameter ranges and target settings of the two parameters were determined to give rise to the lowest open failure rate. The effectiveness of the new process was evaluated by subsequent validation lots. The new process was implemented in mass production following the positive results from the validation lots. As a result of this process change, the open failure rate of FCBGA products was reduced by ~90% versus historic baseline data from mass production. This further supported the proposed non-wetting failure mechanisms in C4 bump reflow found in this study and the effectiveness of the new reflow process developed herein.

3. Results and discussions

The location of the non-wetting bump in open failure units can be readily identified by X-ray inspection. Then, a cross sec-

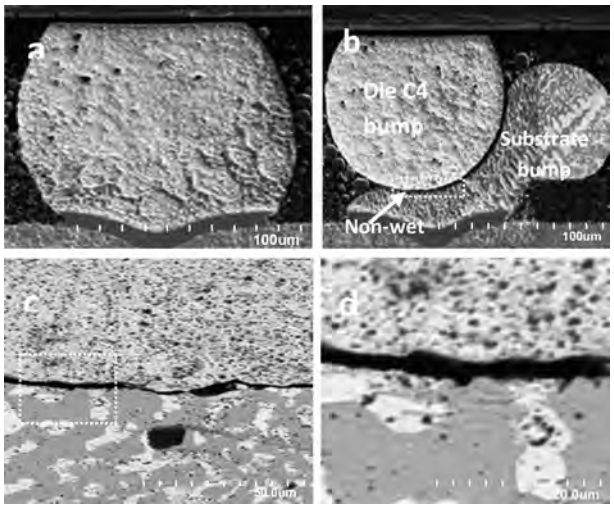

Fig. 4. Die C4 bump and substrate bump interconnection: (a) good wetting, (b) non-wetting, (c) and (d) non-wetting interface.

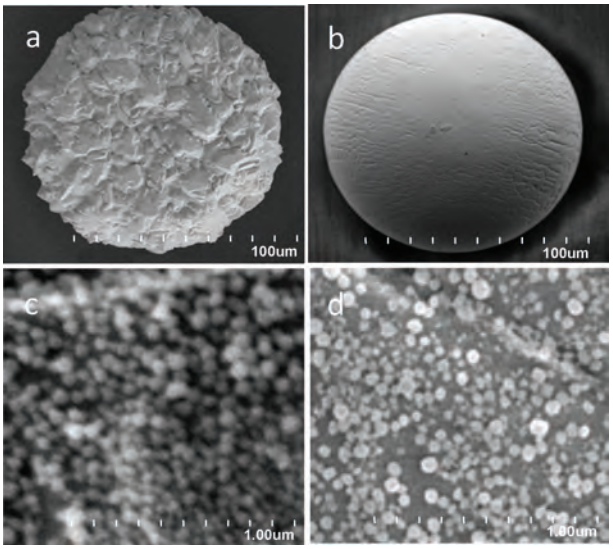

Fig. 5. SEM images of C4 bump and particles on bump surface: (a) pre-reflow bump and (b) post-reflow bump; particles on (c) pre-reflow bump surface and (d) post-reflow bump surface.

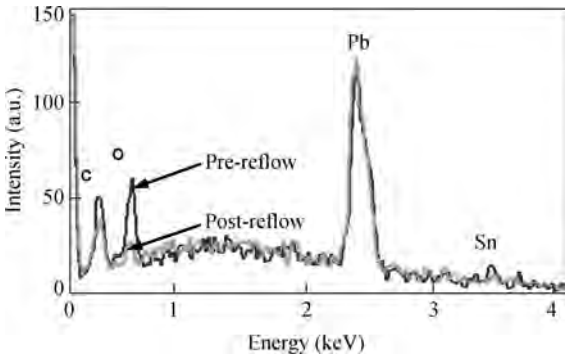

Fig. 6. EDX spectra of particles on pre-reflow and post-reflow bumps.

tion is performed along the center line of the non-wetting C4 bump. Figures 4(a) and 4(b) are SEM pictures of C4 solder joints with good wetting and non-wetting, respectively.

It is apparent that no or very weak solder joints are formed in the non-wetting case of Fig. 4(b). High-resolution SEM photos of non-wetting interface in Figs. 4(c) and 4(d) reveal a clear gap between the C4 bump and the substrate bump. These non-wetting bumps are correlated to open failures after reflow and/or subsequent reliability failures in reliability tests or field service. The composition of the substrate bump is typically Sn–Pb eutectic solder (Pb37%/Sn63%). It possesses good fluidity in the molten state during the chip-attach reflow process (see Fig. 4(b)). Surface oxides on the molten eutectic solder substrate bumps are typically reduced fairly completely and fresh metal surfaces are protected by the liquid flux from re-oxidation. So, this study focused primarily on die C4 bumps, which are suspected to have the most incomplete oxide reduction/removal.

To further analyze the chemical composition at the C4 bump surface, SEM photos were taken of the die bumps before and after the bump-reflow process. Figures 5(a) and 5(b) are images of pre-reflow and post-reflow C4 bumps, respectively. It is very clear that the surface of the post-reflow bump is smoother than that of the pre-reflow bump, and that the post-reflow bump has a well-defined spherical shape as a result of complete melting during the bump-reflow process.

It was also interesting to find, during high magnification SEM examination, that there exists a surface layer of nanometer-sized granular particles on the pre-reflow bumps, which became fewer in quantity and lower in surface coverage after bump reflow, as can be seen in Figs. 5(c) and 5(d).

EDX analyses were performed on the chemical composition of the particles. Usually EDX analysis is used as a semi-quantitative method because the EDX spectrum can just reflect the element content at the focus point rather than the whole bump surface. To fully study and confirm the difference of chemical composition and content at the surface of both pre- and post reflowed bumps, EDX analyses were randomly performed on the bump surface of 60 dies from different lots, 30 pre-reflowed dies and 30 post-reflowed dies, the results are similar to the EDX spectra shown in Fig. 6. Besides lead and tin (the two main elements in the high lead C4 bump) an oxygen peak also appeared in the EDX spectra. Moreover, the oxygen content is lower after bump reflow as compared to pre-reflow. This is evidence that these nano granular particles are lead and tin oxides in nature. This EDX result is also consistent with our anticipation that the bump-reflow process reduces the surface tin and lead oxides through the reaction with H_2 during the thermal process of bump reflow. As a consequence, fewer granular particles were observed on the surface of C4 bumps post reflow. Nevertheless, both the SEM images and EDX spectra indicate the existence of some residual lead and tin oxide particles on the bump surface post-reflow. The incomplete reduction/removal of surface oxides of tin and lead can be attributed to either the chemical inertness of the surface oxides, or the inadequacy of the bump-reflow process, or a combination of both. So, it is necessary and important to further study the properties of the surface oxides and the effect of the bump-reflow process on surface oxides.

Optical inspection on the post-reflow C4 bumps indicates that some surface areas of reflowed C4 bumps are smoother and shinier than other areas, despite the fact that the bump

Table 1. Melting points of 95%Pb/5%Sn and lead/tin oxides.

Material	PbO	Pb_3O_4	PbO_2	SnO	$SnO_{1.33-1.5}$	SnO_2	95%Pb/5%Sn	Eutectic Pb/Sn
Melting points (℃)	888	830	290	1080	—	1127, 1630	300	183

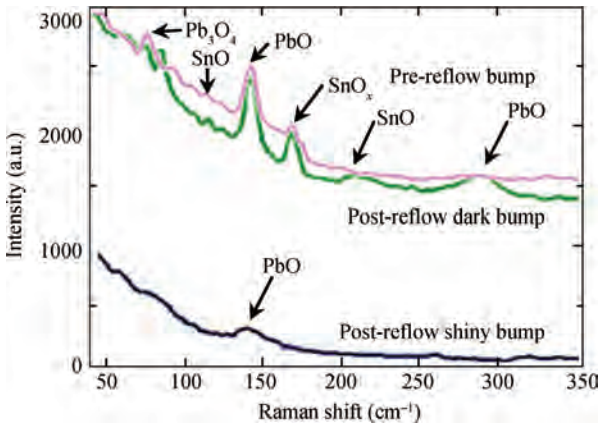

Fig. 7. Raman spectra of pre- and post-reflow C4.

surface is in general smoother and shinier after reflow when compared to the pre-reflow bump surface as a result of oxide reduction by H_2 during the bump-reflow process. Micro-Raman spectroscopy was employed to examine the stoichiometry of the oxides on the bump surfaces pre- and post-reflow. All measurements were performed by using the line of wavelength 514.532 nm from an argon-ion laser with a beam diameter of 1.5 μm and an output power of 10 mW. Raman spectra of the examinations in Fig. 7 were obtained after a series of experiments. Based on the results from previous studies[2−12], tin and lead oxides were marked at the peaks of the spectra in Fig. 7. It is shown that pre-reflow bumps and bumps with less smooth and shiny surfaces after reflow are still covered by some Pb_3O_4, PbO, SnO and other tin oxides (SnO_x, $x \approx 1.33$–1.5); while only PbO was detected on the surface of smooth and shiny bumps post reflow.

It is well known that lead and tin exist in their oxides with the two valences of II and IV. However, no PbO_2 or SnO_2 peaks are observed in the Raman spectra in Fig. 7. This can be due to one of the following.

(1) No PbO_2 and SnO_2 formed during the C4 bump electroplating and subsequent processes.

(2) PbO_2 and/or SnO_2 indeed formed during the processes. However, they were transformed into other types of lead and tin oxides in the during the time between bump electroplating and micro-Raman analysis, such as Pb_3O_4 and SnO_x, $x \approx 1.33$–1.5, or were reduced to lead and tin metals or their monoxides during the bump-reflow process.

(3) PbO_2 and SnO_2 were not detected due to the small laser beam diameter or the limits of micro-Raman spectroscopy detection.

In fact, PbO_2 is not a very stable oxide and can readily lose oxygen to give rise to Pb_3O_4 in ambient air, and Pb_3O_4 can further lose oxygen to give rise to PbO, i.e. the degradation pathway is $PbO_2 \longrightarrow Pb_3O_4 \longrightarrow$ PbO (litharge) $\longrightarrow$ PbO (massicot)[11]. After bump electroplating at a C4 factory, it takes several days to transfer the wafers in a dried air package to an assembly factory, hence there is sufficient time and proper conditions for PbO_2 to degrade to other lead oxides. So, it is logical and understandable that no PbO_2 peak shows up in the Raman spectra.

Table 2. Key process parameters of bump reflow.

Parameter	Dwell temperature	Peak temperature	Dwell time at > 300 ℃	H_2 flow rate
Setting	300 ℃	398 ℃	1100 s	5 cu.ft/s

Table 3. Key parameters of the chip-attach reflow profile.

Parameter	Dwell temperature	Peak temperature	Dwell time at > 183 ℃	Rising time at 145–183 ℃
Setting	183 ℃	235 ℃	60 s	100 s

SnO_2 is a stable oxide in air at room temperature. Its fundamental Raman peaks are at 474, 632, and 774 cm^{-1}, corresponding to its different vibration modes[5, 8, 11], which are out of our micro-Raman limit.

In effect, Pb_3O_4 can be regarded as a compound of PbO_2 and PbO; while SnO_x ($x \approx 1.33$–1.5) normally represents a variable mixture of Sn_2O_3 and Sn_3O_4, both, in turn, are compounds of SnO_2 and SnO. Therefore, the valences of Pb and Sn in all oxides detected in the Raman spectra in Fig. 7 are still of II or IV, which is consistent with the previous theory[3, 5, 9, 11].

In summary, the results of SEM, EDX, optical inspection and micro-Raman confirmed the following predictions:

(1) Lead and tin oxides exist on C4 bump surfaces.

(2) A current bump-reflow process can remove some lead and tin oxides, but it is not effective enough to remove them all.

(3) The residual lead and tin oxides on the C4 bump surface can cause non-wetting failure and introduce reliability risks.

In order to gain better insight into the specific types of lead/tin oxides that are causing non-wetting failures in the chip-attach process, their properties during bump-reflow and chip-attach processes were studied. The melting points of Sn–Pb eutectic solder, lead and tin oxides, and the key parameters of both the bump-reflow and the chip-attach processes are listed in Tables 1, 2 and 3, respectively.

Most lead and tin oxides are expected to be reduced/removed by the bump-reflow process under the standard thermal condition with the presence of H_2. However, there is a chance that a significant amount of oxides will survive the reflow process and form a thin surface layer on the C4 bumps as a result of improper parameter setting or inadequate control of the reflow process and reflow oven.

The melting point of PbO_2 is 290 ℃, lower than the bump reflow dwell temperature of 300 ℃. So, PbO_2 will melt during reflow and should not result in a rough surface appearance of the C4 bumps post reflow. Furthermore, PbO_2 tends to transform into Pb_3O_4 during the dwell time[11]. In contrast,

Table 4. Bump-reflow DOE matrix.

DOE leg	1	2	3	4	5	6	7	8	9
H_2 flow rate (cu.ft/s)	3.5	3.5	3.5	5	5	5	6.5	6.5	6.5
Dwell time (s)	900	1100	1300	900	1100	1300	900	1100	1300

the melting points of the other lead and tin oxides are all above the peak temperature of the bump-reflow process and will remain in a solid state throughout the reflow. As a result, these oxides can form a surface layer of either a thin crust or granular particles on the C4 bumps post reflow and incomplete oxide reduction occurs for various reasons. This surface layer of oxides can prevent the formation of a good solder joint during the chip-attach process. In this case, the surface layer of the oxides floats on the molten C4 bump surface when the C4 bump reflow temperature is above the bump melting point of 300 ℃, resulting in a rough and dull surface after the solidification of the solder bumps. The surface layer of the oxides is thin enough, however, to allow for the formation of the spherical shape of the bumps with minimum surface energy.

After bump-reflow, a die with C4 bumps goes through the chip-attach process, where the peak temperature is only 230 ℃, lower than the melting points of all lead and tin oxides and Pb95%/Sn5% solder itself, but higher than the melting point of Sn–Pb eutectic solder of 183 ℃. As a result, the shape and morphology of C4 bumps will not change any further during chip attach reflow. Only substrate bumps will melt during the chip attach reflow to form the solder joints. The use of flux during the chip-attach process can further disrupt and dissolve some lead and tin oxides at the surfaces of both C4 and substrate bumps in addition to facilitate heat transfer. However, if too many oxides are present on the C4 bump surface after the bump-reflow process, a complete reduction/removal of the surface oxides might not be practical. As a result, no or weak solder joints between the C4 and substrate bumps become a possibility.

To remove the oxides on the C4 bump surface more effectively, it is necessary to revisit the key process parameters of the bump-reflow and chip-attach processes. According to the Pb–Sn phase diagram, the dwell temperature and peak temperature of both processes are adequate for solder melt and reshaping. High-lead C4 bumps and substrate Sn–Pb eutectic bumps can fully melt at the temperatures reached during the two processes, respectively. Therefore, we direct our attention to the thermal budget and H_2 concentration for effective oxide removal. H_2 flow rate and dwell time in a bump-reflow process were studied through a DOE in Table 4.

Open failure rate data of the samples in each DOE leg were collected and analyzed by using the process window selection method. According to the open bin rate contours on the plane of H_2 flow rate and dwell time in Fig. 8. Based on this DOE, H_2 flow rate should be retargeted to 4.5 cu.ft/s from a standard setting of 5 cu.ft/s; and the center setting of the bump-reflow dwell time needs to be adjusted to 1250 s from 1100 s for optimal oxide removal.

It is usually thought that a longer bump-reflow dwell time will benefit the removal of lead and tin oxides at the bump surface, but the lower H_2 flow rate may not help. In fact, there is no pre-heat system in a bump reflow furnace, thus cold H_2 causes convection heat loss at the area close to the H_2 inlet. As a result, the wafers there do not have adequate thermal budget to complete the reaction to completely remove lead and tin oxides. Our baseline data also shows that the wafers positioned in the slots near the H_2 inlet have higher non-wetting failure. By retargeting the H_2 flow rate to 4.5 cu.ft/s from 5 cu.ft/s, the convection heat loss will be less so that the wafers close to H_2 inlet can gain more thermal budget for lead and tin oxide reduction.

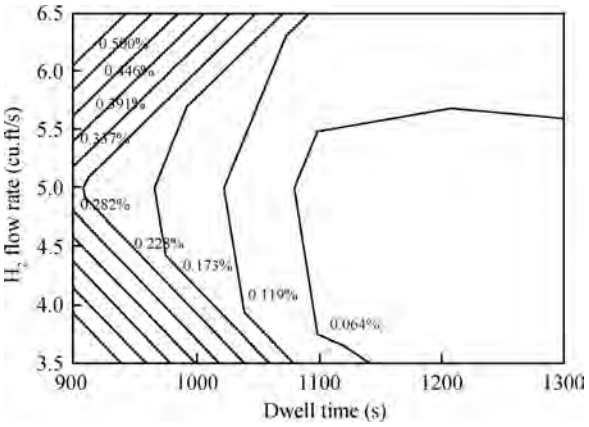

Fig. 8. Bump-reflow DOE analysis result.

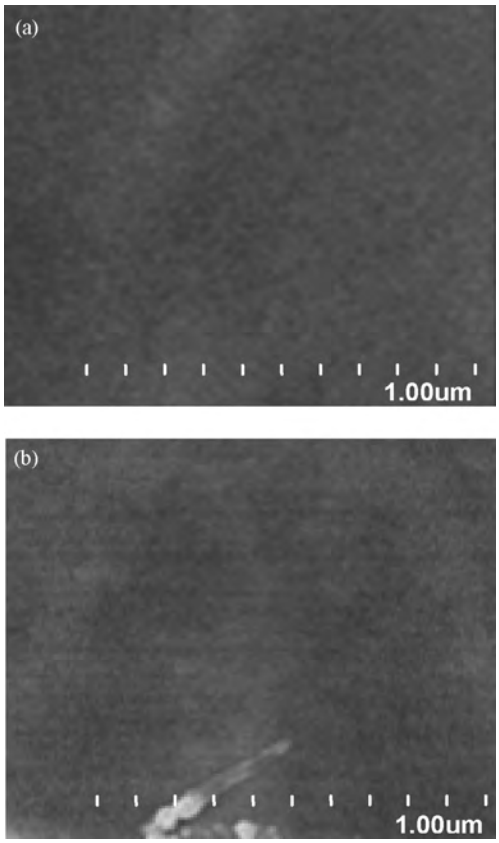

Fig. 9. SEM images of C4 bumps reflowed under optimized bump-reflow process: (a) no oxide grain or (b) very few oxide grains on bump surface.

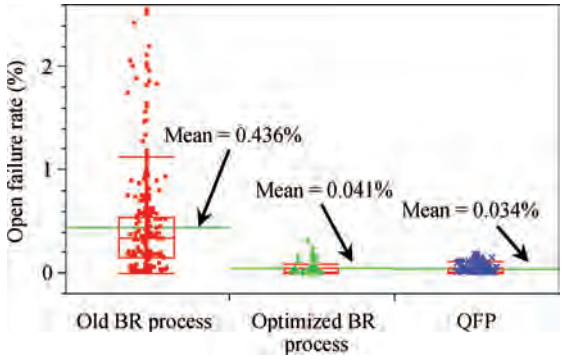

Fig. 10. Open failure rate comparison.

To verify and validate the effectiveness of the new bump-reflow process, SEM photos of C4 bumps were taken after reflow with the optimized settings of H_2 flow rate and dwell time. Most of the C4 bump surfaces are very clean and smooth, with only very few oxide particles being observed (Fig. 9). Obviously, C4 bumps with such clean surfaces would benefit the formation of good solder joints with substrate bumps. The minor residue of surface oxide particles can be readily reduced/removed by flux during the chip-attach process, with a diminishing detrimental effect on solder joint quality and reliability. It is interesting to compare the images of the bump surface conditions in Figs. 5 and 9. The improvement in bump surface oxidation by optimization of the C4 bump-reflow process is apparent.

The optimized settings of the bump-reflow process parameters were also further validated by pilot lots and mass production. Test results of the pilot and production lots showed that the open bin rate was reduced from 0.436% to 0.041%, comparable to that of the QFP package, as seen in Fig. 10.

4. Conclusion

In summary, multiple analytical techniques, including SEM, EDX and micro-Raman spectroscopy were employed in this study of the surface lead and tin oxides nanoparticles on C4 bumps. It was identified that the surface oxides of lead and tin on C4 bumps are the primary causes of non-wetting during the chip-attach reflow process, which, in turn, causes open failure and/or reliability failure of FCBGA products. The presence and amount of lead and tin oxides on the C4 bumps and their behavior during the C4 bump reflow and chip-attach reflow processes are affected by many process parameters and conditions. Although lead and tin oxides form naturally in air at room temperature, most of the oxides on the C4 bump surface are formed during the bump electroplating process and when bumped wafers are exposed to elevated temperatures with the presence of oxygen. The effective reduction/removal of lead and tin oxides from the bump surface during the C4 bump-reflow process is very critical to the quality and reliability of flip-chip solder joints. A 9-leg DOE was performed on the C4 bump-reflow process with the objectives of gaining a better understanding of the influence of process parameters on the amount of surface lead and tin oxides and their effect on non-wetting in chip-attach reflow. The results indicated that with an optimized H_2 flow rate of 4.5 cu.ft/s and dwell time of 1250 s, most of the lead and tin oxides on a C4 bump surface can be effectively removed, leading to lower open failure rate after the chip-attach process. Production data also showed that the open bin failure rate was drastically reduced by about 90%, on a par with that of mature QFP packages. Overall, through this study, not only a better understanding of the surface lead and tin oxides and their effects on non-wetting of flip chip solder joints were achieved, but also an optimized C4 bump-reflow process was developed and implemented in mass production that effectively reduces the surface lead and tin oxides on C4 bumps and improves the open failure rates during chip-attach-reflow process.

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