A fast combination calibration of foreground and background for pipelined ADCs*

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Abstract: This paper describes a fast digital calibration scheme for pipelined analog-to-digital converters (ADCs). The proposed method corrects the nonlinearity caused by finite opamp gain and capacitor mismatch in multiplying digital-to-analog converters (MDACs). The considered calibration technique takes the advantages of both foreground and background calibration schemes. In this combination calibration algorithm, a novel parallel background calibration with signal-shifted correlation is proposed, and its calibration cycle is very short. The details of this technique are described in the example of a 14-bit 100 Msample/s pipelined ADC. The high convergence speed of this background calibration is achieved by three means. First, a modified 1.5-bit stage is proposed in order to allow the injection of a large pseudo-random dithering without missing code. Second, before correlating the signal, it is shifted according to the input signal so that the correlation error converges quickly. Finally, the front pipeline stages are calibrated simultaneously rather than stage by stage to reduce the calibration tracking constants. Simulation results confirm that the combination calibration has a fast startup process and a short background calibration cycle of 2×2^{21} conversions.

Key words: background calibration; capacitor mismatch and gain calibration; digital calibration; foreground calibration; pipelined analog-to-digital converter; signal-shifted correlation

DOI: 10.1088/1674-4926/33/6/065007 **EEACC:** 2570

1. Introduction

The performance of pipelined ADC is mainly limited by the nonlinearity resulting from capacitor mismatch and finite opamp gain in the MDAC. In order to eliminate these non-ideal factors, the self-calibration of an ADC in the digital domain has been proposed. By measuring and computing the non-ideal transfer characteristics of analog circuits in the digital domain, the calibrated output code can be obtained through the inverse of actual transfer function.

The digital calibration techniques for pipelined ADC are mainly categorized into either foreground[1] or background[2−17] calibration schemes, by whether the calibration process interrupts the normal conversion. Foreground calibration inherently requires the injection of a known sequence of voltage signals at the calibrated stage input in order to measure the non-ideal transfer characteristics of the calibrated stage. During the normal conversion period, the calibrated output code can be obtained by the inverse transfer function of the calibrated stages. Although the foreground calibration is faster and more accurate than the background algorithm in Refs. [2–11], the drawback is that every time calibration is carried out, the operation has to be interrupted. Thus, the foreground calibration cannot track the device and environmental variations.

Correlation-based background calibration has been used in pipelined analog-to-digital converters (ADCs) for measuring and correcting capacitor mismatch and finite opamp open-loop errors[2−11]. This method injects a pseudo-random noise (PN) sequence modulated dithering into the signal path of MDACs in the analog domain and then demodulates the output of MDACs with the same PN sequence in the digital domain to extract the errors and cancel code errors in the conversion. However, correlation-based background calibration has two limitations. One is the fact that the correlation converges slowly, due to a strong interference from the input signal to the calibrated stage. The other is the injected PN dithering magnitude constraint, since the signal plus PN dithering injection should not saturate the next stage.

To inject PN dithering into the signal path of the calibrated stage, PN dithering is injected only in a certain range of the input full-scale range[2, 3] so that the output range of the calibrated stage can be confined within the input range of the next stage. This means that more than half of the conversions cannot be utilized for calibration, when assuming that the input signal of each calibrated stage is uniformly distributed within the input range. Several correlation-based background calibration schemes split the sample capacitors into a certain number of fragments to inject PN dithering into the signal path of the calibrated stage without saturating the next stage[2, 4, 5]. However, these schemes increase the number of mismatch capacitors that need to be measured[4, 5] or unnecessarily introduce extra noise due to mismatch between the split capacitors[2]. Moreover, in previous papers the calibration proceeds from the rear stages to the front repeatedly, thus for one calibration cycle it takes the summation of the correlation time of each calibrated stage. Take a correlation-based background calibration for 15-bit pipelined ADC as an example[4], it needs 40×2^{28} samples to complete one calibration cycle.

A parallel background calibration with signal-shifted correlation scheme is proposed to improve the drawback of the correlation-based background calibration mentioned above by taking the following measures. First, a modified 1.5-bit stage

* Project supported by the National Key Project, China (No. 2008zx010200001).

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Received 6 November 2011, revised manuscript received 28 December 2011

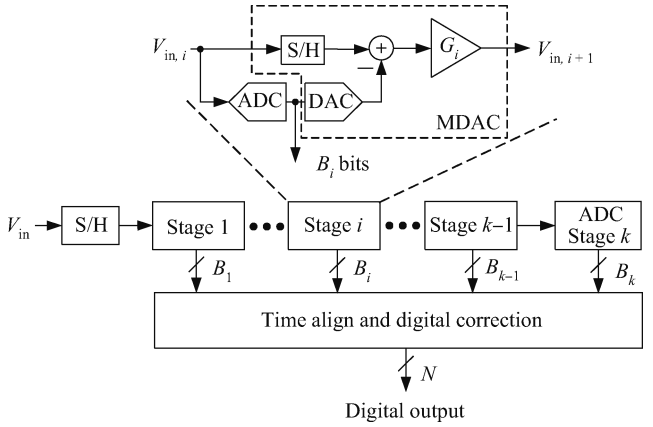

Fig. 1. Block diagram of a pipelined A/D converter.

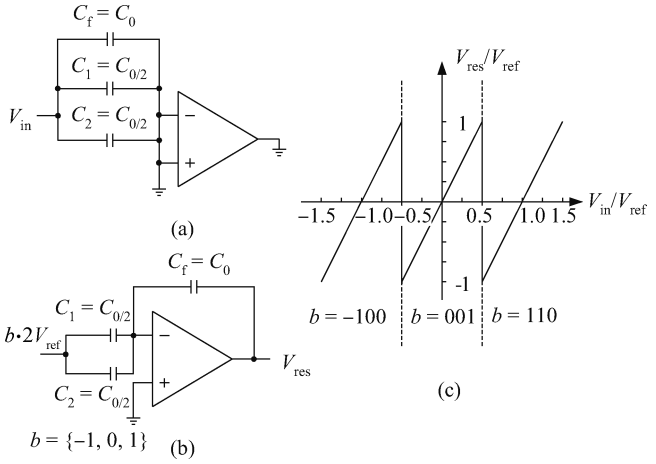

Fig. 2. Modified tri-level MDAC. (a) Sampling phase. (b) Amplification phase. (c) Residue plot.

is introduced in order to allow the injection of a large pseudo-random dithering without missing code, and as a result the signal-to-dithering ratio[2] can be minimized and thereby the measurement time of the calibrated stage is relieved. Second, before correlating the output of the calibrated stage with PN, it can be shifted according to the input signal so that the interference from the input signal to the calibrated stage can be reduced, and therefore the correlation converges quickly. Finally, the front pipeline stages are calibrated simultaneously rather than stage by stage to reduce the calibration tracking time constant. When the calibrated stage is 1.5-bit and its input range is divided into 34 sub-ranges, the nonlinear error resulting from capacitor mismatch and finite opamp gain in the modified MDAC is measured with 14-bit accuracy within a theoretical number of 2×2^{21} conversions for one measurement cycle. If the front six stages are calibrated, then the startup process of the proposed calibration needs $6 \times 2 \times 2^{21}$ conversions, which means a slow calibration startup.

In this paper, a combination calibration scheme is proposed for a 14-bit 100 Msample/s pipelined ADC to improve the limitations of both the foreground and background calibration techniques. The realization of the system is as follows: a foreground calibration is carried out at startup, and then background calibration is turned on during the normal conversions. It takes $6 \times 7 \times (32 + 32)$ conversions to complete the foreground calibration. Therefore, the calibration parameter can be extracted immediately at startup through the foreground calibration and then continuously updated rapidly to adapt to device and environment changes by the background calibration, without interrupting the normal A/D conversion.

2. Error source and digital calibration

2.1. Modified 1.5-bit/stage pipelined ADC and flash ADC

A general block diagram of a pipelined A/D converter is shown in Fig. 1. It consists of a sample and hold stage, several low-resolution stages, and time align and digital correction logic. Each stage comprises a sub-analog-to-digital (sub-ADC) and an arithmetic unit called the multiplying digital-to-analog converter (MDAC). Figure 2 shows a tri-level MDAC of a modified 1.5-bit pipeline stage in two phases, where "00, 01, 10" is the sub-ADC output. In ideal pipelined ADC, during the amplification phase, the sample input is multiplied by a gain of 2. The residue plot of V_{res} is shown in Fig. 2(c), where the comparator thresholds of the sub-ADC are set to $\pm V_{ref}/2$. Assuming that the ADC is ideal, the analog output of each stage is given by

$$V_{res} = 2V_{in} - b \cdot 2V_{ref}. \quad (1)$$

As for the typical 1.5-bit pipeline stage with RSD (redundant sign digit) technique, proposed by Ginetti and Jespers in 1988[18], the error resulting from comparator threshold offset can be canceled by introducing a redundant bit and setting the comparator thresholds at $\pm V_{ref}/4$, so that a certain amount of output range margin is left when the input signal is at the threshold point. Unlike the typical 1.5-bit pipeline stage, which confines the output within the range $[-V_{ref}, +V_{ref}]$ to not exceed the input range of the next stage, the modified 1.5-bit pipeline stage cancels its comparator threshold offset errors by extending the input range of the next stage to $[-1.5V_{ref}, +1.5V_{ref}]$. Even if the output of a 1.5-bit pipeline stage exceeds the range of $[-V_{ref}, +V_{ref}]$, as long as it is still in the range of $[-1.5V_{ref}, +1.5V_{ref}]$, then the error due to comparator threshold offset can be canceled without missing code. The input range of the whole pipelined ADC is $[-1.5V_{ref}, +1.5V_{ref}]$. One purpose of modifying the typical 1.5-bit pipeline stage is to inject a large PN dithering to the signal path so as to reduce measurement time during a background calibration cycle[2]. Another purpose is to add PN dithering in most input signal range rather than only in a small input range[2, 3], thus most conversions can be used for calibration.

Since the output of the modified 1.5-bit pipeline stage may exceed the range $[-V_{ref}, +V_{ref}]$, two additional comparators with the threshold set at $\pm V_{ref}$ should be added in the last flash ADC stage so that the input range of the flash ADC can be extended and the output has a redundant bit. A 2.5-bit flash ADC with one redundant bit is shown in Fig. 3, where $\{b_{i,2}, b_{i,1}, b_{i,0}\}$ is the binary output of the 2.5-bit flash ADC. Assuming that the corresponding decimal code of the output of the 2.5-bit flash ADC is D_i, then the transfer function for an input $V_{in,i}$ ($-1.5V_{ref} \leqslant V_{in} \leqslant +1.5V_{ref}$) is expressed as

$$V_{in,i} = D_i V_{ref}/2 - 1.25V_{ref} + \varepsilon_{q,i}, \quad (2)$$

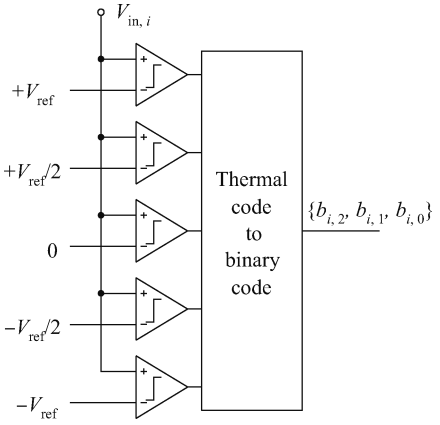

Fig. 3. A 2.5-bit flash ADC.

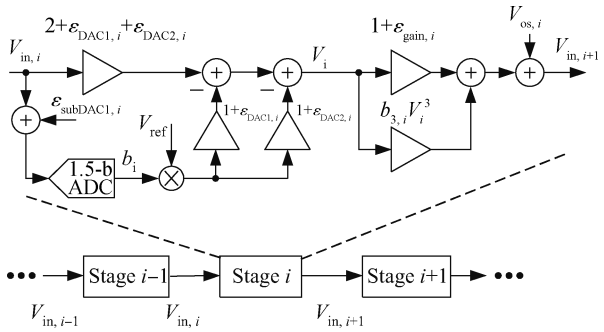

Fig. 4. Model of a pipelined ADC with non-ideal factors.

where $\varepsilon_{\text{q},i}$ is the flash ADC quantization noise, $\varepsilon_{\text{q},i} \in [-V_{\text{ref}}/4, +V_{\text{ref}}/4]$, and $D_{\text{i}} \in \{0, 1, 2, 3, 4, 5\}$.

2.2. Nonlinearity error of the 1.5-bit pipeline stage

The pipeline stage model with non-ideal factors is presented in Fig. 4. $\varepsilon_{\text{subADC},i}$ represents the sub-ADC comparator threshold offset, which can be corrected in this modified 1.5-bit stage as discussed above. $\varepsilon_{\text{DAC1},i}$, $\varepsilon_{\text{DAC2},i}$ represent the error caused by the mismatch between C_{f}, C_1 and C_2, which can be calibrated by the proposed digital calibration in this paper. $\varepsilon_{\text{gain},i}$ and $b_{3,i}$ represent the finite opamp gain error and opamp third-order nonlinearity coefficients of stage i, where they can be expressed as[19]

$$1+\varepsilon_{\text{gain},i} = \frac{1}{1+\dfrac{1}{A_i f_i}}, \tag{3}$$

$$b_{3,i} \propto \frac{a_{3,i}}{(1+f_i A_i)^4}, \tag{4}$$

where coefficients A_i, $a_{3,i}$ and f_i represent the open-loop amplifier gain, third-order distortion and closed-loop feedback factor of stage i, respectively. In this paper, for a 14-bit pipelined ADC, it is assumed that the open-loop amplifier gain A_i is sufficiently large, thus the third-order closed-loop nonlinearity coefficient $b_{3,i}$ is negligibly small and not calibrated. The error resulting from finite open-loop opamp gain A_i can be calibrated by the proposed digital calibration in this paper. As the opamp offset $V_{\text{os},i}$ only results in an overall offset to the pipelined ADC, which has no impact on the dynamic performance, the opamp offset is not calibrated.

2.3. Digital calibration concept

We assume that only capacitor mismatch errors $\varepsilon_{\text{DAC1}}$, $\varepsilon_{\text{DAC2}}$ for sample capacitors C_1 and C_2, and finite opamp gain error $\varepsilon_{\text{gain}}$ exist in pipelined ADC. According to the structure of MDAC, as shown in Fig. 2, the transfer function of the practical 1.5-bit MDAC is:

(1) when $V_{\text{in}} < -0.5V_{\text{ref}}$,

$$V_{\text{res}} = GV_{\text{in}} + K_1 V_{\text{ref}} + K_2 V_{\text{ref}}, \tag{5}$$

(2) when $-0.5V_{\text{ref}} \leqslant V_{\text{in}} \leqslant +0.5V_{\text{ref}}$,

$$V_{\text{res}} = GV_{\text{in}}, \tag{6}$$

(3) when $V_{\text{in}} > +0.5V_{\text{ref}}$,

$$V_{\text{res}} = GV_{\text{in}} - K_1 V_{\text{ref}} - K_2 V_{\text{ref}}, \tag{7}$$

where the coefficients G, K_1 and K_2 are

$$G = \frac{2(C_1+C_2)}{\dfrac{C_1+C_2+C_{\text{f}}}{A}+C_{\text{f}}} = (1+\varepsilon_{\text{gain}})(2+\varepsilon_{\text{DAC1}}+\varepsilon_{\text{DAC2}}), \tag{8}$$

$$K_1 = \frac{2C_1}{\dfrac{C_1+C_2+C_{\text{f}}}{A}+C_{\text{f}}} = (1+\varepsilon_{\text{gain}})(1+\varepsilon_{\text{DAC1}}), \tag{9}$$

$$K_2 = \frac{2C_2}{\dfrac{C_1+C_2+C_{\text{f}}}{A}+C_{\text{f}}} = (1+\varepsilon_{\text{gain}})(1+\varepsilon_{\text{DAC2}}), \tag{10}$$

in which A is the finite opamp open-loop gain. An equivalent transformation of a pipelined ADC is shown in Fig. 5. Figure 5(a) represents the functional diagram of a pipeline ADC with finite opamp gain error and capacitor mismatch error, where

$$\alpha_i = \varepsilon_{\text{DAC1},i} + \varepsilon_{\text{DAC2},i}, \tag{11}$$

$$\beta_i = \varepsilon_{\text{gain},i}. \tag{12}$$

If we change closed-loop gain G to 2, we need to add a gain factor of $(2+\alpha_i)(1+\beta_i)/2$ before the pipeline stage input, and a gain factor of $2/[(2+\alpha_i)(1+\beta_i)]$ to the sub-ADC signal path. Then we simply redefine the stage's input and output so that each stage's input gain factor is merged into its previous stage's output gain factor, thus an equivalent block diagram as shown in Fig. 5(b) is obtained. Now, we could merge each stage's output gain factor into the stage $i-1$ input gain factor. The resulting equivalent ADC is shown in Fig. 5(c). Note that the error resulting from closed-loop gain slope coefficient G can be decomposed into errors in sub-ADC, sub-DAC and the overall ADC gain slope error. The errors in sub-ADC can be regarded as the comparator threshold offset, which can be canceled by the RSD technique as discussed above. The overall ADC gain slope error is a constant and does not deteriorate the performance of the pipelined ADC as it is equivalent to changing the amplitude of the input signal by multiplying a constant

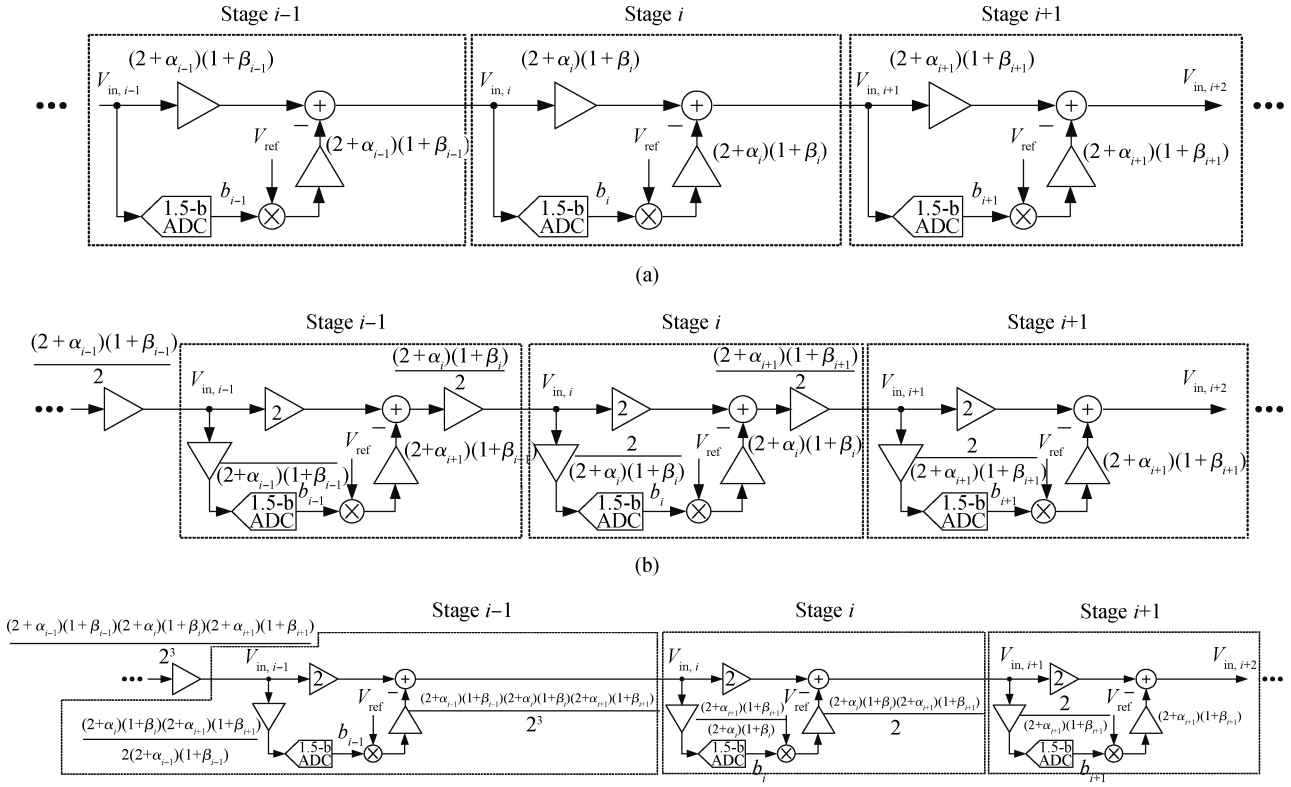

Fig. 5. Equivalent transformation of a pipelined ADC.

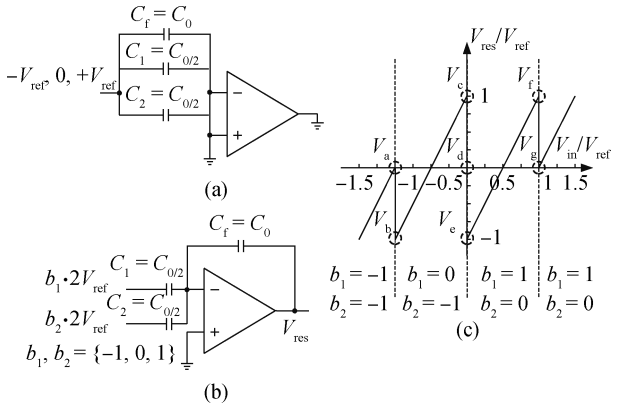

Fig. 6. MDAC during foreground calibration. (a) Sampling phase. (b) Amplification phase. (c) Residue plot.

factor, thus it is not necessary to correct this error. The error that needs to be calibrated is in the sub-DAC of each pipeline stage. There is no harm in assuming that the closed-loop gain G of each stage equals 2 in the following parts of this paper, according to Fig. 5(c), and the errors in the sub-DAC due to the closed-loop gain deviation together with capacitor mismatch error and finite opamp gain error can be regarded in terms $K_1V_{\rm ref}$ and $K_2V_{\rm ref}$. The digital calibration concept measures the terms $K_1V_{\rm ref}$ and $K_2V_{\rm ref}$, respectively. While these terms are subtracted in the MDAC, their digital values are added back instead of the ideal digital value of $V_{\rm ref}$.

3. Digital foreground calibration

In this work, the 14-bit pipelined ADC consists of 14 modified 1.5-bit pipeline stages and a 2.5-bit flash ADC with a redundant bit. The two extra bits are used for minimizing the quantization during digital calibration. Since ADC linearity is mainly determined by the front stages, the errors due to capacitor mismatch and finite opamp gain are corrected by using a recursive digital calibration algorithm from the sixth stage to the first stage. Assuming the closed-loop gain G equals 2, a simplified residue transfer function of the pipeline stage is expressed as

$$V_{\rm res} = 2V_{\rm in} - b_1K_1V_{\rm ref} - b_2K_2V_{\rm ref}, \tag{13}$$

where in the ideal case both K_1 and K_2 are equal to 1. The b_1 and b_2 are –1, 0, or 1 depending on the region where the input $V_{\rm in}$ lies, and $-V_{\rm ref}$, 0 and $+V_{\rm ref}$ are injected, respectively, as the stage analog input, as depicted in Fig. 6.

When calibrating a single stage, the calibration requires seven conversions, given in Eqs. (14)–(20). According to Eq. (13), the output of the calibrated stage can be expressed as:

(1) when $V_{\rm in} = -V_{\rm ref}$, $b_1 = -1$ and $b_2 = -1$,

$$V_{\rm a} = 2 \times (-V_{\rm ref}) + K_1V_{\rm ref} + K_2V_{\rm ref}, \tag{14}$$

(2) when $V_{\rm in} = -V_{\rm ref}$, $b_1 = 0$ and $b_2 = -1$,

$$V_{\rm b} = 2 \times (-V_{\rm ref}) + K_2V_{\rm ref}, \tag{15}$$

(3) when $V_{\rm in} = 0$, $b_1 = 0$ and $b_2 = -1$,

$$V_{\rm c} = 2 \times (0) + K_2V_{\rm ref}, \tag{16}$$

(4) when $V_{\text{in}} = 0$, $b_1 = 0$ and $b_2 = 0$,

$$V_{\text{d}} = 2 \times (0), \tag{17}$$

(5) when $V_{\text{in}} = 0$, $b_1 = +1$ and $b_2 = 0$,

$$V_{\text{e}} = 2 \times (0) - K_1 V_{\text{ref}}, \tag{18}$$

(6) when $V_{\text{in}} = +V_{\text{ref}}$, $b_1 = +1$ and $b_2 = 0$,

$$V_{\text{f}} = 2 \times (+V_{\text{ref}}) - K_1 V_{\text{ref}}, \tag{19}$$

(7) when $V_{\text{in}} = +V_{\text{ref}}$, $b_1 = +1$ and $b_2 = +1$,

$$V_{\text{g}} = 2 \times (+V_{\text{ref}}) - K_1 V_{\text{ref}} - K_2 V_{\text{ref}}, \tag{20}$$

where V_{a}, V_{b}, V_{c}, V_{d}, V_{e}, V_{f} and V_{g} are the residual output voltages at each conversion point, as shown in Fig. 6(c). These seven conversion points are obtained by fixing the calibrated stage input at 0 and $\pm V_{\text{ref}}$, respectively, and controlling the output value of DAC in MDAC. The calibration parameters are now defined as $K_{1,\text{est,fore}} V_{\text{ref}} = (V_{\text{a}} - V_{\text{b}} + V_{\text{d}} - V_{\text{e}})/2$, $K_{2,\text{est,fore}} V_{\text{ref}} = (V_{\text{c}} - V_{\text{d}} + V_{\text{f}} - V_{\text{g}})/2$. During foreground calibration, for each conversion point, the first 32 samples were dropped due to pipeline delay and 32 samples were accumulated and averaged to eliminate the noise influence. Since the first six stages are calibrated, it takes $6 \times 7 \times (32 + 32)$ conversions to complete the foreground calibration.

For each pipeline stage, the backend pipeline stages can be regarded as a pipelined ADC. By using Eqs. (1), (2) and (13) recursively from the last stage to the first stage, all calibration parameters in calibrated stages can be expressed by backend stage digital outputs and the quantization noise in the last flash ADC, as does the input signal of the first pipeline stage. Now, we define the infinite resolution of digital output, D_{infinite}. Since the input range of the whole pipelined ADC is $[-1.5V_{\text{ref}}, +1.5V_{\text{ref}}]$, the relationship between D_{infinite} and the first stage input signal can be expressed as

$$D_{\text{infinite}} = (V_{\text{in},1} + 1.5V_{\text{ref}})/\text{LSB} - 0.5, \tag{21}$$

where $\text{LSB} = 1.5V_{\text{ref}}/2^{N-1}$, and $N = 16$ in this 14-bit pipelined ADC example. The two extra bits are used to reduce the quantization error in the calibration parameters.

The digital signal can be processed in digital circuits. In Eq. (21), the error due to last flash ADC quantization noise can be viewed as the quantization of pipelined ADC. After truncating the last two bits, there are 14-bit digital calibrated outputs.

4. Proposed digital background calibration

4.1. Principle of correlation-based background calibration

Similar to the foreground calibration concept, and in order to estimate the terms $K_1 V_{\text{ref}}$, $K_2 V_{\text{ref}}$, a correlation-based background calibration is utilized in this work. Figure 7 shows this term measurement scheme via PN1 dithering, where the terms K_1 and K_2 are regarded as the same variable K for simplicity, but in real implementation they are measured separately. To measure the term K, a PN1-modulated calibration signal is added to the signal path, V_{sig}. The PN1 is a zero-mean sequence of 1 and –1. The amplitude of the PN1-modulated calibration

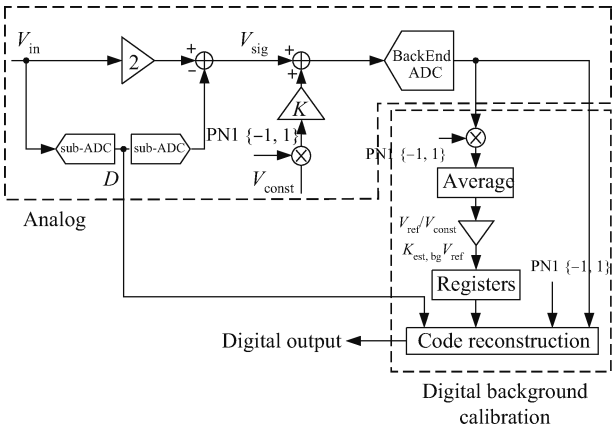

Fig. 7. The background term "$K V_{\text{ref}}$" measurement.

signal is a constant V_{const}, where V_{const} equals $V_{\text{ref}}/2$. $K_{\text{est, bg}}$ is the estimation of the term K and can be induced from the block diagram as follows:

$$K_{\text{est, bg}} V_{\text{ref}} = \frac{1}{M} \sum_{i=1}^{M} \left(\frac{V_{\text{sig}}[i]}{V_{\text{const}}} V_{\text{ref}} \text{PN1} \right) + K V_{\text{ref}} \text{PN1}^2, \tag{22}$$

where M is the number of averaging samples, and V_{sig} is uncorrelated to PN1. Since $\text{PN1}^2 = 1$, the first term in Eq. (22) could be regarded as the measurement error, and after averaging a large number of samples, it can converge to a negligibly small value. It is obvious that the ratio of $V_{\text{sig}}/V_{\text{const}}$ should be as small as possible so that the measurement error can converge quickly. After the accumulator averages a large number of samples, the value of $K_{\text{est, bg}}$ is obtained and stored in registers for digital calibration.

4.2. Signal-shifted correlation

In order to shorten the averaging time and improve the measurement accuracy, the signal-to-dithering ratio $V_{\text{sig}}/V_{\text{const}}$ should be as small as possible. There are two approaches to achieve this goal. One way is to inject a large PN dithering into the signal path to increase the value of V_{const}. As for the modified 1.5-bit pipeline stage proposed in this paper, the amplitude of dithering is equivalent to a $0.5V_{\text{ref}}$ fixed-amplitude dithering. Another way is to minimize the variation range of V_{sig}, thus a signal-shifted correlation scheme is proposed as shown in Fig. 8. V_{sig} belongs to the range $[-0.5V_{\text{ref}}, +0.5V_{\text{ref}}]$. In the ideal case, V_{sig} can be expressed as

$$V_{\text{sig}} = 2V_{\text{in}} + 2.5V_{\text{ref}} - DV_{\text{ref}} \in [-0.5V_{\text{ref}}, +0.5V_{\text{ref}}], \tag{23}$$

where $D = 1, 2, 3, 4$, and $V_{\text{in}} \in [-V_{\text{ref}}, +V_{\text{ref}}]$. The signal-shifted algorithm is as follows:

as for $V_{\text{in}} \in [-V_{\text{ref}} + 0.0625nV_{\text{ref}}, -0.9375V_{\text{ref}} + 0.0625nV_{\text{ref}}]$,

$$V_{\text{sig}} + (DV_{\text{ref}} - 9V_{\text{ref}}/16 - nV_{\text{ref}}/8) \in [-V_{\text{ref}}/16, +V_{\text{ref}}/16], \tag{24}$$

where $n = 0, 1, 2, \ldots, 31$. The equivalent fixed-amplitude PN dithering is shown in Fig. 8(b). It is obvious that after shifting the signal, the variation range of V_{sig} reduces from [–$0.5V_{\text{ref}}$,

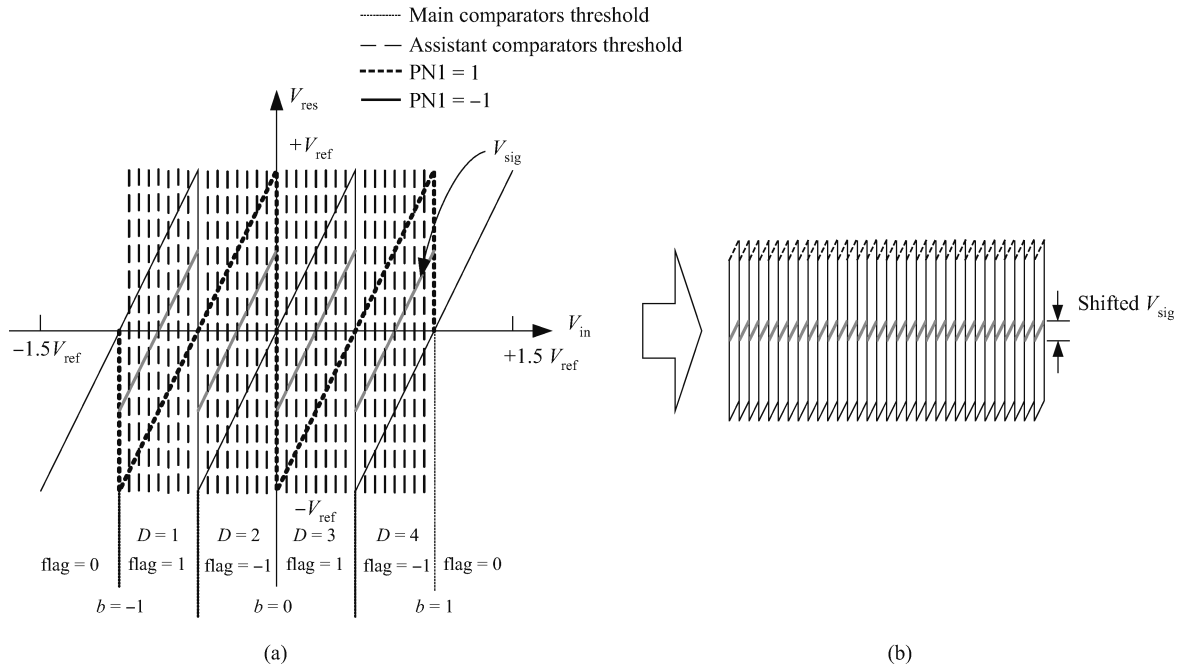

Fig. 8. Dithering for signal-shifted correlation. (a) 34 sub-range. (b) Equivalent fixed-amplitude PN dithering.

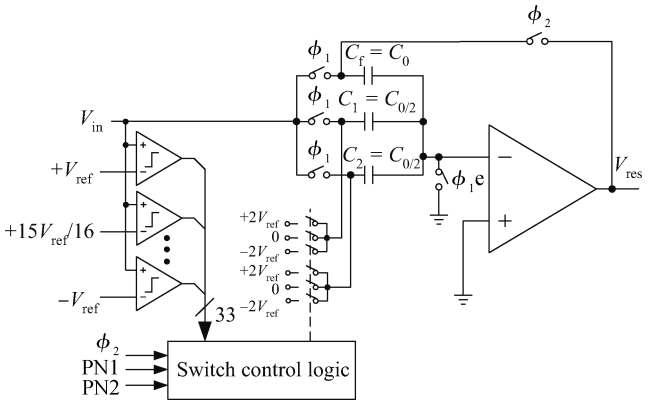

Fig. 9. The background calibrated pipeline stage.

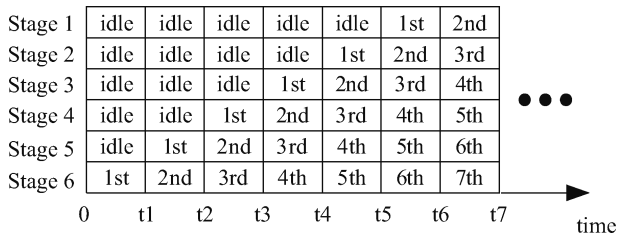

Fig. 10. The parallel background calibration process of a six calibrated stage system.

$+0.5V_{ref}$] to [$-0.0625V_{ref}$, $+0.0625V_{ref}$], resulting in a reduction in measurement time. When the calibrated stage input signal is outside the range [$-V_{ref}$, $+V_{ref}$], no dithering is added and errors in MDAC are not measured.

4.3. Capacitor mismatch and gain error measurement

Figure 9 shows the 1.5-bit calibrated pipeline stage, which is modified from "charge transfer" architecture by adding 33 comparators. The threshold voltages of the comparators and the residual plot of the calibrated stage are shown in Fig. 8(a). The comparators, whose threshold voltages are set at $\pm V_{ref}$, $\pm V_{ref}/2$ and 0, are main comparators which determine the residual plot. The remaining comparators are assistant comparators, which are used for shifting the signal before correlation. ϕ_1 and ϕ_2 are the sample phase and amplification phase, respectively. The switch controlled by ϕ_{1e} is off before the switches controlled by ϕ_1 in order to diminish the charge injection effect, but they are on at the same time. PN1 is a pseudo-random noise sequence and PN1 $\in$ {–1, 1}. Another pseudo-random noise sequence, PN2, as seen in Fig. 9, is required in the calibrated stage to decide which capacitor is used for the injection, so that the capacitors C_1 and C_2 are equally monitored, where PN2 $\in$ {1, 2}. Another variable flag is introduced in Fig. 8(a) in order to decide whether to inject PN dithering and the polarity of the injection. The residual plot of the calibrated stage is shown in Fig. 8(a) and the transfer function is:

$$V_{res} = 2V_{in} - bK_1V_{ref} - bK_2V_{ref} - \text{flag}(\text{PN1} + 1)K_{\text{PN2}}V_{ref}/2. \quad (25)$$

When flag equals 0, no dithering is added into the signal path of the calibrated stage. Pay attention to the last term of Eq. (25), because it contains the sub-DAC error, which results from capacitor mismatch and finite opamp gain. If flag $\neq$ 0, then flag^2 = 1 and PN1^2 = 1. When flag $\neq$ 0, Equation (25) is added with ($DV_{ref} - 9V_{ref}/16 - nV_{ref}/8$), where n = 0, 1, 2, …, 31, and then multiplies with (–2 × flag × PN1), as in the signal-shifted correlation technique discussed above, and calibration parameter K_1V_{ref} and K_2V_{ref} can be obtained by accumulating Eq. (26) separately:

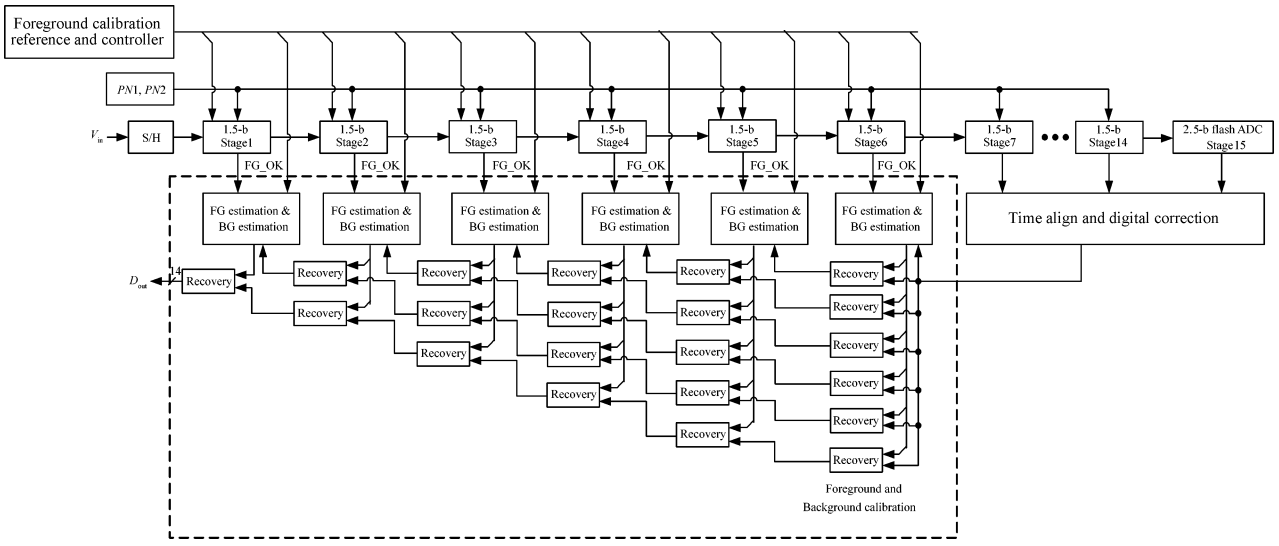

Fig. 11. Architecture of a 14-bit pipelined ADC with foreground and parallel background calibration.

$$[-2 \times \text{flag} \times \text{PN1} \times (V_{\text{res}} + DV_{\text{ref}} - 9V_{\text{ref}}/16 - nV_{\text{ref}}/8)] = K_{\text{PN2}}V_{\text{ref}} + \theta \times \text{PN1}, \quad (26)$$

where flag $\neq 0$ and

$$\theta = (-2 \times \text{flag}) \times (2V_{\text{in}} - bK_1V_{\text{ref}} - bK_2V_{\text{ref}} - \text{flag} \times K_{\text{PN2}}V_{\text{ref}}/2 + DV_{\text{ref}} - 9V_{\text{ref}}/16 - nV_{\text{ref}}/8). \quad (27)$$

Here $\theta \in [-V_{\text{ref}}/8, +V_{\text{ref}}/8]$. As discussed in Section 3, K_1V_{ref}, and K_2V_{ref} are measured separately. According to Eq. (26), it can found that:

(1) When PN2 = 1, flag $\neq 0$,

$$K_{1,\text{est,bg}}V_{\text{ref}} = \frac{1}{M}\sum_{i=1}^{M}(K_1V_{\text{ref}} + \theta[i] \times \text{PN1}[i]) = K_1V_{\text{ref}} + \sigma_1, \quad (28)$$

(2) When PN2 = 2, flag $\neq 0$,

$$K_{2,\text{est,bg}}V_{\text{ref}} = \frac{1}{M}\sum_{i=1}^{M}(K_2V_{\text{ref}} + \theta[i] \times \text{PN1}[i]) = K_2V_{\text{ref}} + \sigma_2. \quad (29)$$

Here, $\sigma_{1,2} = \frac{1}{M}\sum_{i=1}^{M}(\theta[i] \times \text{PN1}[i])$.

Since θ is uncorrelated with PN1, after accumulating and averaging a large number of $\theta[i] \times \text{PN1}[i]$, $\sigma_{1,2}$ converges to 0.

As soon as the measurement of $K_{1,\text{est.back}}V_{\text{ref}}$ and $K_{2,\text{est.back}}V_{\text{ref}}$ is completed, by replacing the ideal V_{ref} with $K_{1,\text{est.back}}V_{\text{ref}}$ and $K_{2,\text{est.back}}V_{\text{ref}}$ in the code reconstruction, the calibrated digital output of ADC is obtained. In the ideal case, the output range of the pipeline stage is within $[-V_{\text{ref}}, +V_{\text{ref}}]$, as shown in Fig. 8, which equals the calibration input range of the next stage. This means that most of the conversions can be used for background calibration, rather than the conversions of a certain calibrated stage input range[2].

4.4. Parallel background calibration

The parallel background calibration scheme is proposed as another way to reduce the background calibration tracking time by measuring the parameters of the calibrated stages simultaneously. Unlike the background calibration in Refs. [2, 4], which proceeds from the rear stage and works its way toward the front repeatedly, the calibration parameters in all the calibrated stages are continuously measured and updated in a concurrent moment as a pipeline rather than in sequential fashion. Upon the background calibration startup process, however, the calibration parameters are measured and stored from the rear stage to the front stage, in a sequential fashion. Figure 10 shows the background calibration process, where 1st, 2nd, …, represents the 1st calibration cycle, 2nd calibration cycle, …, respectively. As for one calibration cycle, the $i-1$ stage begins to measure the calibration parameters only after the calibration parameters of stage i have been determined.

The highlight of parallel background calibration is that the time for one calibration cycle is equivalent to the time for calibrating one stage and no longer dependent on the number of calibration stages.

5. Simulation results and discussion

Figure 11 shows the architecture of a 14-bit pipelined ADC with the combination calibration of foreground and parallel background. It has one S/H, 14 1.5-bit stages, and a 2.5-bit flash ADC. The two extra stages are required to reduce the quantization errors in the calibration parameters. Before generating output, the two extra bits are truncated from the A/D conversion result, and thus a 14-bit ADC whose quantization error is less than 0.5 least significant bit (LSB) is realized.

In Fig. 11, the foreground calibration reference provides the reference voltages of $\pm V_{\text{ref}}$ and 0 for the foreground calibrated stages. The foreground calibration controller selects

the foreground calibrated stage input signal from either the foreground calibration reference voltages or the output of the front stage and decides its DAC output in MDAC as shown in Fig. 1. Thus the seven conversion points, V_a–V_g, as shown in Fig. 6(c), can be estimated, respectively. Before A/D conversion begins, the foreground calibration is carried out first and FG (foreground) estimation block begins to estimate the calibration parameters, known as K_1V_{ref} and K_2V_{ref}. Due to the fast speed of foreground calibration, the calibration parameters can be obtained immediately. After the foreground calibration is completed, the FG_OK signal turns on the background calibration and BG (background) estimation block begins to estimate and update these calibration parameters during the normal conversions. The recovery blocks perform the code reconstruction function to obtain the A/D conversion of each stage input signal. A pseudo-random number generator generates PN1 and PN2. In order to extract the calibration parameters of each calibrated stage simultaneously, six BG (background) estimation blocks, performing signal shifting and correlation function, are required in this parallel background calibration scheme.

Since the non-ideal factors in the back-end stages are less critical, the 7–14 stages are not calibrated to reduce the number of accumulators and code reconstruction paths, which may increase the area of the digital circuit. However, in order to obtain good performance of the SFDR, the DEM (dynamic element matching) technique[3], was adopted in the back-end stages, but the calibration parameters in the back-end stages are not extracted. Since there are 33 comparators in the calibrated stage and five comparators in the uncalibrated stages, the sub-ADC outputs in the calibrated and uncalibrated stages are 6 and 3 bits, respectively.

The background calibration process in this paper is slower and less accurate than the foreground algorithm. The main reason for this is the error resulting from the correlation between θ and PN1, as the second term in Eqs. (28) and (29). The θ PN1 variation term is caused by the perturbation of the shifted residual signal of the calibrated stage and PN1. Assuming that this variation term is uniformly distributed between $-V_{ref}/8$ and $+V_{ref}/8$, its average power can be approximated to ${V_{ref}}^2/192$. The number of accumulating and averaging samples can reduce the effect of this perturbation power by a factor of M. Thus, the variation of $\sigma_{1,2}$ can be expressed as

$$\sigma_{1,2}^2 = \frac{1}{M}\frac{V_{ref}^2}{192}. \tag{30}$$

By calculating the inverse function of Eq. (25), the input of the first calibrated stage can be expressed as

$$V_{in,1} = \frac{V_{in,2}}{2} + \frac{K_1V_{ref} + K_2V_{ref}}{2}b + \text{flag}\frac{(\text{PN1}+1)K_{PN2}V_{ref}}{4}. \tag{31}$$

According to Eqs. (28) and (29), K_1V_{ref} and K_2V_{ref} contain the calibration noise term $\sigma_{1,2}$. Now we define the code reconstruction noise $N_{bg,cali}$ as the error factor in $V_{in,1}$ due to the background calibration noise term $\sigma_{1,2}$. When $b = \pm 1$ and PN1 = –1, it is the worst case for $N_{bg,cali}$. The average power of $N_{bg,cali}$ can be approximated to

$$N_{bg,cali} = 2\sigma_{1,2}^2\sum_{j=1}^{6}\frac{1}{2^{2j}} \approx \frac{2}{3}\sigma_{1,2}^2. \tag{32}$$

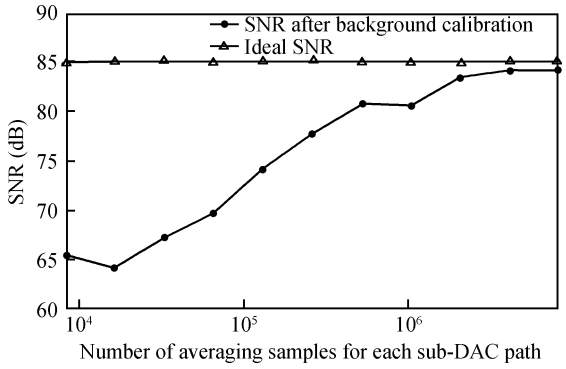

Fig. 12. The SNR value of a digital background calibrated pipelined ADC without capacitor mismatch as a function of M for sine input.

To determine the required value of M, let $N_{bg,cali}$ be less than the average power of the ADC's quantization noise. For an N-bit ideal ADC with input range $(-V_{ref}, +V_{ref})$, its average quantization noise power is $(2V_{ref}/2^N)^2/12$. Thus, the required value for M is

$$M \geqslant \frac{2}{3}\times 2^{2N-6} \geqslant 2^{2N-7}. \tag{33}$$

For a 14-bit pipelined ADC, one can choose $M = 2^{22}$, so that $N_{bg,cali}$ could be less than the quantization noise power.

The ADC model was simulated in a Matlab Simulink environment. The architecture of a 14-bit pipelined ADC has one S/H, 14 1.5-bit stages and a 2.5-bit flash ADC. It contains both foreground and background calibration. Two extra bits are added to reduce the digital calibration quantization noise, and only the first six stages are calibrated. The DEM technique is applied in this design in order to increase SFDR at the cost of a little reduction in SNR.

Simulations show that background calibration with $M = 2^{21}$ can also achieve 14-bit resolution and has a shorter calibration time. When there is no capacitor mismatch, opamp open-loop gain in the first three and remaining stages are 120 dB and 100 dB, respectively. Simulation results show the value of SNR after background calibration, as a function of M, as shown in Fig. 12, where M varies from 2^{13} to 2^{23}. The amplitude of the sinusoidal signal is $10^{(-1/20)}V_{ref}$. The change in SNR can be regarded as the behavior of correlation convergence. In the ideal case, the SNR would be

$$\text{SNR}_{ideal} = 10\lg\frac{(10^{-1/20}V_{ref})^2/2}{\text{LSB}^2/12} \approx 85\,\text{dB}, \tag{34}$$

where $\text{LSB} = 2V_{ref}/2^{14}$. In Fig. 13, when M is set to 2^{21}, the SNR after background calibration achieves 83.4 dB, which approaches 85 dB, the value of SNR in the ideal case. This proves the feasibility of $M = 2^{21}$ for background calibration in the actual design.

Now, the ADC model was simulated with 1% capacitor mismatch, and the opamp open-loop gain in the pipeline stages was 60 dB. Let PN1 and PN2 be set to constants, thus the DEM is off, and no dithering will be added into the signal path of the pipeline stages. As a result, the sine-wave spectral responses before and after foreground calibration are shown in Fig. 13. Before calibration, the ENOB is 7 bit and SFDR is 49.1 dB

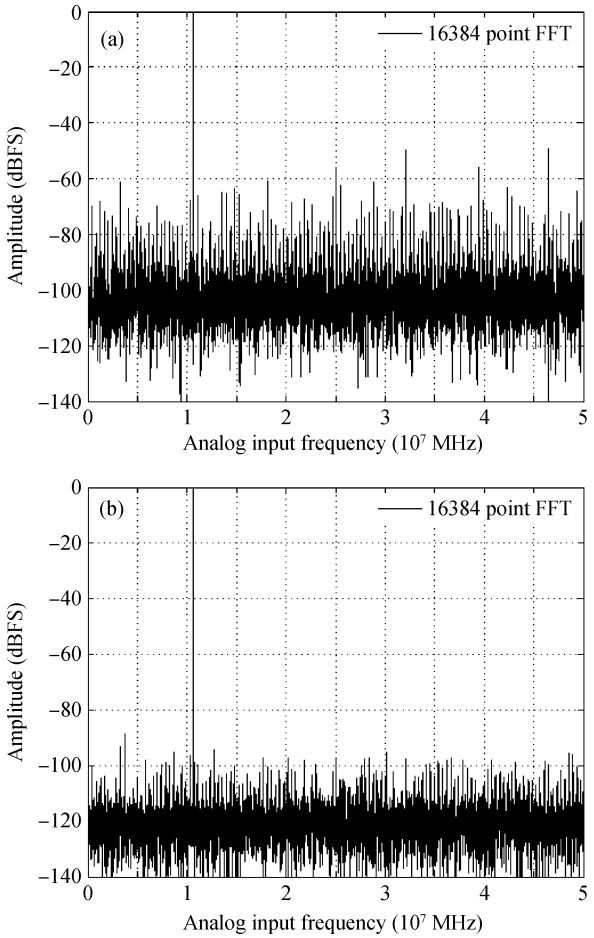

Fig. 13. Sine-wave spectral response with DEM off. (a) Without calibration. (b) After foreground calibration.

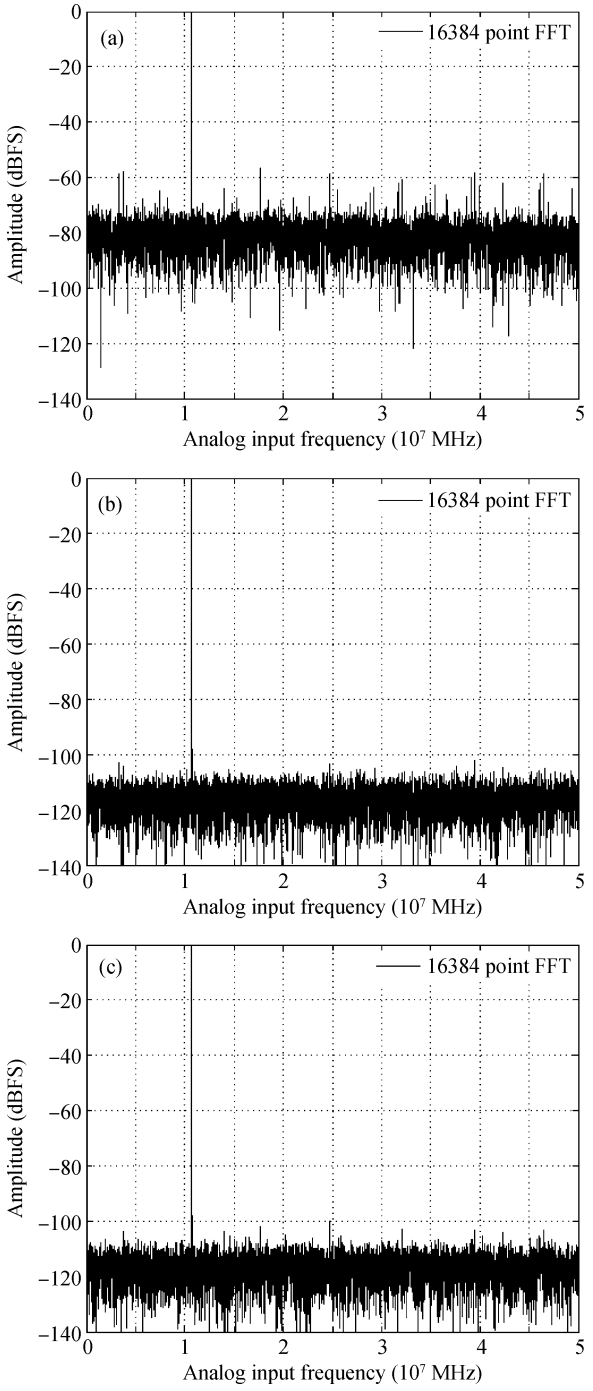

Fig. 14. Sine-wave spectral response with DEM on. (a) Without calibration. (b) After foreground calibration. (c) After background calibration.

due to capacitor mismatch and opamp gain error. After foreground calibration, the ENOB is increased to 12.5 bit and the SFDR is 88.6 dB. When the DEM is on, PN dithering would be added into the signal path of the pipeline stages by PN1 and PN2. In the case where the correlation takes 2^{21} samples for each sub-DAC path, the sine-wave spectral responses without calibration, with foreground and background calibration, are illustrated in Fig. 14. Before calibration, the ENOB is 6.5 bit and SFDR is 57.9 dB due to capacitor mismatch and opamp gain error. After the digital calibration is enabled, the foreground calibration is carried out, and during normal conversion the background calibration is turned on. After foreground calibration, the ENOB is increased to 12.5 bit and the SFDR is 104.2 dB. The improvement in SFDR and reduction in SNR between the foreground calibration with DEM and without DEM is obvious to see. After background calibration startup, the ENOB is 12.6 bit, and the SFDR is 102 dB. The number of averaging samples for one background calibration cycle is 2×2^{21} and it needs to average $6 \times 2 \times 2^{21}$ samples for digital background calibration startup. The degradation of dynamic performance after foreground and background calibration from an ideal ADC is mainly due to capacitor mismatch and opamp finite gain in the backend stages; these are not calibrated.

If parallel and signal-shifted correlation are not applied in this work, assuming that the variation term $V_{\rm sig}$, as shown in Fig. 8(a), is uniformly distributed between $-V_{\rm ref}/2$ and $+V_{\rm ref}/2$, its average power can be approximated to ${V_{\rm ref}}^2/12$. By the same means of calculating the value of M, the number of required samples for one background calibration cycle is $6 \times 2 \times 2^{25}$, which is nearly 100 times larger than before.

In each calibrated stage, 33 comparators are required. The current consumption of each main comparator is 180 μA with a 3.3 V power supply, and each main comparator area approximates 17×90 $\mu{\rm m}^2$. Since the assistant comparators are not required to be as fast as the main comparators, the power consumption and area could be relieved to some extent. In sum, due to the 33 comparators in each calibrated stage, the overall

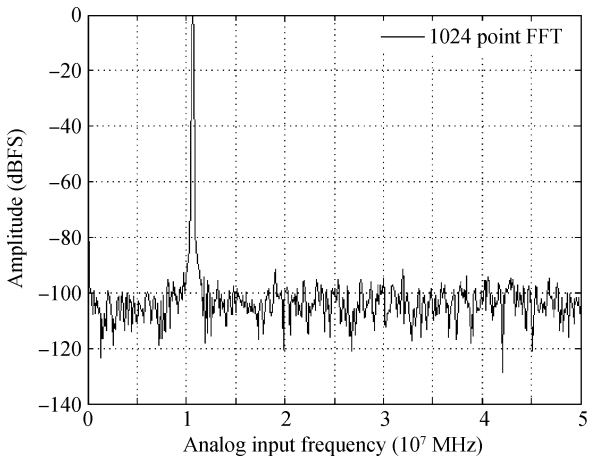

Fig. 15. Sine-wave spectral response with DEM simulated by Spectre.

hardware overhead would increase. Fortunately only the first six stages need to be calibrated, thus this hardware increase is tolerable. Since the amplifier load capacitor value is mainly determined by kT/C noise constraints, those comparators would not seriously increase the total load on the amplifiers. The errors due to main comparator threshold offset could be cancelled by the RSD technique as discussed in Section 2. However, the errors due to assistant comparator threshold offset would decrease the convergence speed of the background calibration. Thus, the assistant comparator threshold offset should be as small as possible, e.g. the comparators consisting of series amplifiers and the latch with offset canceling technique could be utilized in this design.

The feedback factor of the modified 1.5-bit pipeline stage is half that of the conventional 1.5-bit pipeline stage. This means that the power consumptions of the modified 1.5-bit pipeline stage and conventional 1.5-bit pipeline stage are almost the same. However, the output range of the modified MDAC is equal to two-thirds the input range, thus the stress on the opamp dynamic range could be relieved to some extent, and the telescopic cascade opamp is used rather than the folded cascode opamp to save power consumption. The pipelined ADC is simulated by Spectre, and simulation results show that the current consumption is 192 mA with a 3.3 V power supply voltage. The sine-wave spectral response with DEM on is shown in Fig. 15.

6. Conclusion

A fast combination calibration scheme of foreground and background is proposed so that the calibration parameter can be extracted immediately at startup by the foreground calibration and continuously updated rapidly to adapt to device and environment changes by background calibration, without interrupting normal ADC conversion. It takes 2688 conversions to complete the foreground calibration. A parallel background calibration with signal-shifted correlation is also proposed in this paper in order to reduce the background calibration tracking cycle. This technique allows the injection of large dithering when the calibrated stage input signal is within the range of $[-V_{\text{ref}}, +V_{\text{ref}}]$. Moreover, by dividing and shifting the signal, the signal-to-dither ratio is further reduced. At the same time, the front stages are calibrated simultaneously as a pipeline. In the ideal case, the output range of the pipeline stage is within $[-V_{\text{ref}}, +V_{\text{ref}}]$, which equals the calibration input range of the next stage. This means that most of the conversions can be used for background calibration, rather than the conversions of a certain calibrated stage input range[2]. Benefiting from the measures taken in this paper, the tracking and convergence rates are fast. The DEM technique is applied in all pipeline stages to improve the performance of SFDR. Simulation results show that the proposed calibration technique is capable of correcting both capacitor mismatch and opamp finite gain errors of the pipelined ADC.

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