A 680 V LDMOS on a thin SOI with an improved field oxide structure and dual field plate*

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Abstract: A 680 V LDMOS on a thin SOI with an improved field oxide (FOX) and dual field plate was studied experimentally. The FOX structure was formed by an "oxidation-etch-oxidation" process, which took much less time to form, and had a low protrusion profile. A polysilicon field plate extended to the FOX and a long metal field plate was used to improve the specific on-resistance. An optimized drift region implant for linear-gradient doping was adopted to achieve a uniform lateral electric field. Using a SimBond SOI wafer with a 1.5 μm top silicon and a 3 μm buried oxide layer, CMOS compatible SOI LDMOS processes are designed and implemented successfully. The off-state breakdown voltage reached 680 V, and the specific on-resistance was 8.2 $\Omega\cdot$mm^2.

Key words: SOI LDMOS; field oxide; field plate; breakdown voltage
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1. Introduction

High breakdown voltage SOI devices are attractive for use in power ICs due to their excellent isolation and small parasitical effect[1,2]. However, the design and fabrication of high voltage devices exceeding 600 V using the traditional RESURF structure on SOI is difficult due to the restriction of vertical breakdown voltage[3]. The super junction structure[4], membrane high voltage devices[5] and ENDIF principle[6] based devices[7,8] have been reported to realize above 600 V breakdown voltages using an SOI, but all of them are complex to fabricate. Some theoretical and experimental studies have shown that the maximum breakdown voltage of SOI devices depends mainly on the thickness of the top silicon layer and the buried oxide (BDX)[9], as shown in the expression[10,11] below and in Fig. 1 (ignore the interface charges).

$$V_{\mathrm{B,V}} = \left[\frac{9.783\times(21.765-\ln t_{\mathrm{si}})}{3.975+\ln t_{\mathrm{si}}}(\varepsilon_{\mathrm{si}}t_{\mathrm{box}}+0.5\varepsilon_{\mathrm{ox}}t_{\mathrm{si}}) + q\sigma_{\mathrm{in}}t_{\mathrm{box}}\times10^{-4}\right]/\varepsilon_{\mathrm{ox}}. \quad (1)$$

Here $\varepsilon_{\mathrm{si}}$ and $\varepsilon_{\mathrm{ox}}$ are the relative permittivities of silicon and SiO_2 respectively, t_{si} is the thickness of the top silicon layer, t_{box} is the thickness of the buried oxide, and σ_{in} is the interface charge density between the top silicon layer and the buried oxide.

As shown in the Fig. 1, when the BOX is 3 μm or above, realization of 600 V breakdown voltage devices on SOI requires the thickness of the top silicon to be either above 20 μm or below 0.5 μm. For power ICs on a thick top silicon layer (> 20 μm), trench isolation using a dielectric or poly material is complex and costly[12]. However, for SOI wafers with about 1.5 μm of top silicon, it is easy to realize full dielectric isolation by using a trench, and the top silicon can be reduced to less than 0.5 μm during the thick field oxide process in order to support high voltage. It is desirable to have the top silicon layer thicker in the source region of the device, because this improves the source-high performance for high-side applications[13].

The traditional FOX structure (see Fig. 2(a)) for thin SOI high voltage devices has two problems: firstly, it takes very long time to form a thick thermal oxide layer; secondly, the

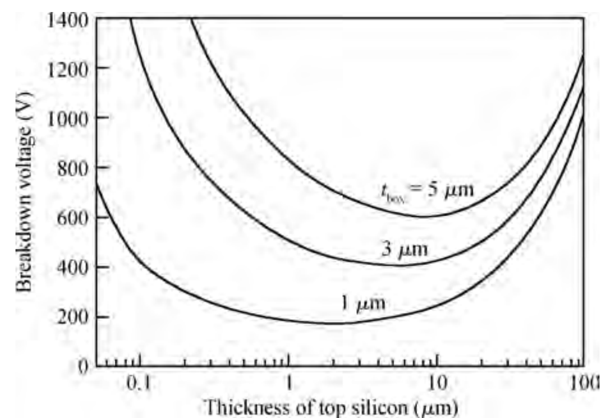

Fig. 1. The maximum breakdown voltage versus the thickness of the top silicon.

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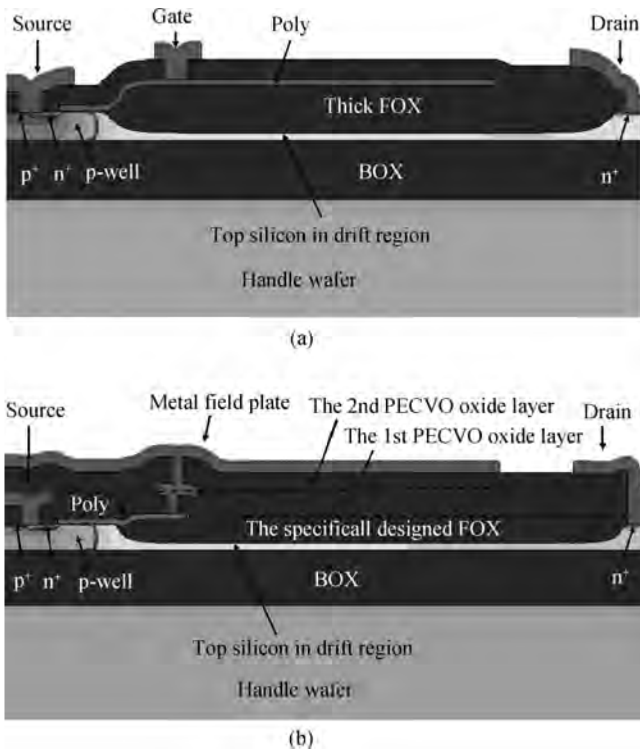

Fig. 2. Device structure of (a) the traditional and (b) the proposed 680 V LDMOS transistors.

Table 1. Four different processes to form FOX.

FOX process	t_1 (min)	t_2 (min)	$t_1 + t_2$ (min)	Δd (μm)
Process 1	760	0	760	1.52
Process 2	100	320	420	0.54
Process 3	170	230	400	0.21
Process 4	220	165	385	0.04

t_1 and t_2 are the first and second oxidation times separately; Δd is the protrusion of the FOX above the surface of the top silicon.

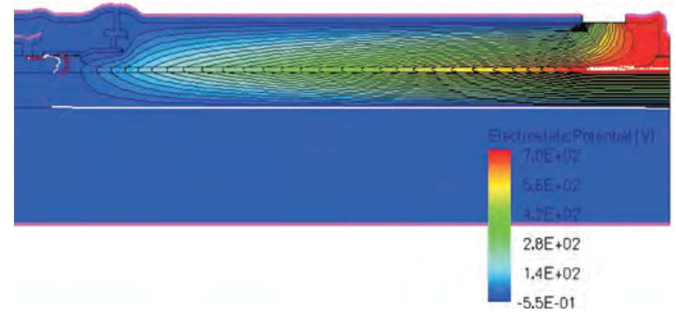

Fig. 3. The equipotential lines distribution at 680 V bias voltage.

protrusion of the thick FOX hinders photolithography alignment afterwards. In this work, we propose a device structure with a new FOX process and dual field plate to optimize the fabrication process and improve device characterization at the same time.

2. Device structure and fabrication process

A Simbond SOI[14–16] wafer with a 1.5 μm top silicon and a 3 μm buried oxide layer was used for SOI LDMOS fabrication in this work. The handle wafers were p-type doped with a resistivity of 15–25 Ω·cm, and the top silicon was p-type doped with a resistivity of 10–20 Ω·cm.

As shown in Fig. 2(b), SOI LDMOS structures in this work were derived from the NXP EZ-HV$^{\rm TM}$ device[13, 17]. The surface lateral electric field in the drift region can be expressed as[18]

$$E_x(x,0) = \frac{q t_{\rm si}}{\varepsilon_{\rm si}\varepsilon_{\rm o}}\left(\frac{t_{\rm si}}{2} + \frac{\varepsilon_{\rm si}}{\varepsilon_{\rm ox}} t_{\rm box}\right)\frac{{\rm d}N(x)}{{\rm d}x}, \tag{2}$$

where $N(x)$ is the impurity concentration in the drift region, and ε_0 is the permittivity of vacuum. In order to achieve a uniform lateral electric field, an optimized 50 μm drift region implant mask was designed to realize a linearly graded doping profile. Phosphorus was implanted into the drift region using this mask and was followed by drive-in annealing at 1200 ℃. The field oxide was grown onto the drift region by using a novel "oxidation-etch-oxidation" process, as described in detail in next paragraph. After this process, the silicon thickness of the drift region was reduced from 1.5 to 0.36 μm. The P-well was formed by using the same implantation of boron for the threshold voltage adjustment. After the gate oxide was grown, polysilicon was deposited by LPCVD and patterned for the gate region. The source, drain and p-body region were formed by high dose implantation followed by RTA activation. Finally, the metal and passivation layers were deposited.

Several FOX processes were studied by simulation as shown in Table 1. The thickness of the top silicon in the drift region is 0.37 μm for all of the FOX process in the table. The first one was the conventional thick field oxide process, and the last one was the optimized novel process, which was formed by following steps. Firstly, a 1.28 μm oxide layer was grown for 220 min at 1100 ℃. Then the oxide layer was removed completely by wet-etching to expose the silicon surface again. Finally, a 1.17 μm oxide layer was grown for 165 min at the same oxidation atmosphere and temperature. In contrast with conventional FOX processing, the novel FOX was thin, with low protrusion above the surface, and took much less time to form. The thin FOX and its low protrusion were helpful for the photolithography alignment afterwards and the reduction of the thermal budget.

A poly-silicon field plate extended 3 μm to the FOX, and a long metal field plate connected with a gate through two VIAs was formed on the PECVD oxide layer to keep a high off-state breakdown voltage and improve the specific on-resistance simultaneously. In order to retain the approximate symmetry of the vertical electric field distribution (see Fig. 3), the two oxide layers formed by PECVD need to make sure that the total oxide thickness on the drift region was slightly above the buried oxide thickness of the SOI substrate.

The process flow and device performance of the designed LDMOS transistor were simulated using the mixed numerical two-dimensional TCAD tool Sentaurus. As shown in Figs. 3 and 4, when the doping concentration in the drift region increased linearly from the channel edge to the drain side, the lateral electric field distribution was uniform and no obvious peak appeared. These indicated that the proposed process flow can realize a linear doping profile and make a lateral electric field

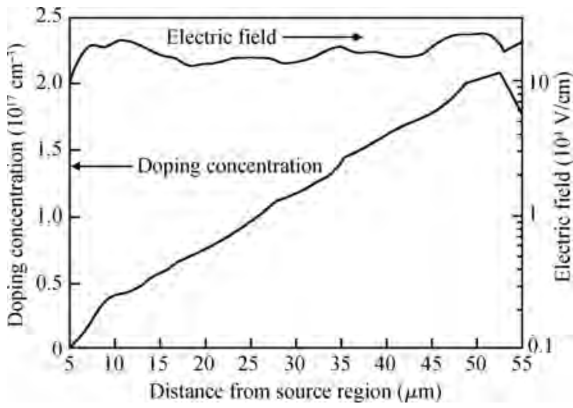

Fig. 4. The doping profile and the electric field distribution in the drift region at 680 V bias voltage.

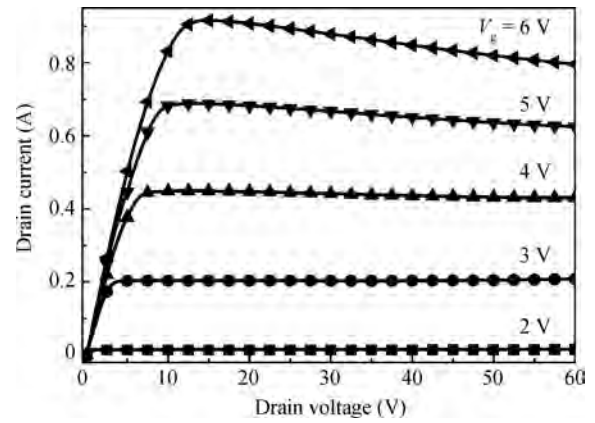

Fig. 6. The measured results of on-state output characteristics.

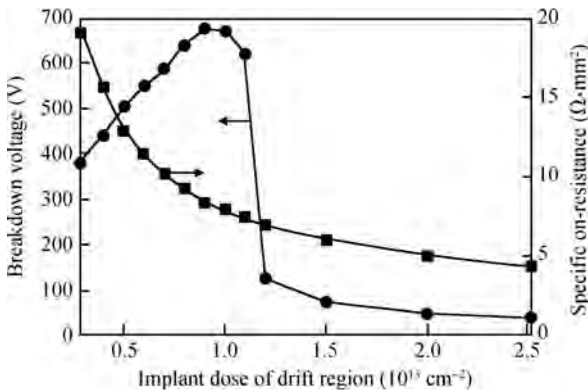

Fig. 5. Breakdown voltage and specific on-resistance at different drift region implant doses.

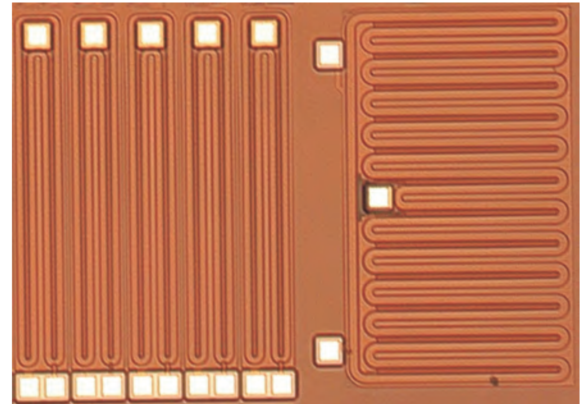

Fig. 7. Micrograph of the proposed SOI LDMOS.

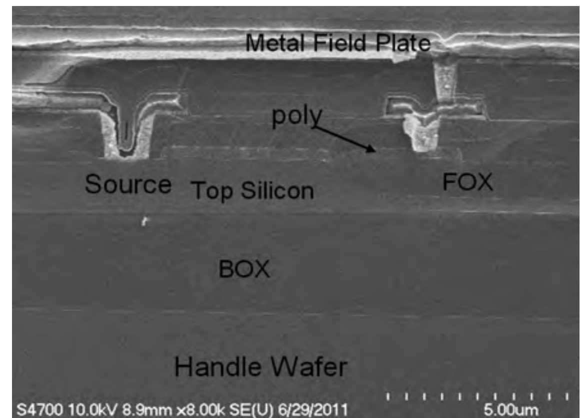

Fig. 8. SEM cross-section of source and gate region.

uniform distribution. The relationship of the breakdown voltage and specific on-resistance with different implant doses of the drift region was also simulated and is illustrated in Fig. 5. At the implant dose of about 9.0×10^{12} cm^{-2}, the device reached the maximum breakdown voltage of 680 V. With the implant dose exceeding this value, the breakdown voltage decreases dramatically.

3. Experimental results

The proposed SOI LDMOS process flow was compatible with conventional CMOS technology, and SOI LDMOS devices were fabricated on a Simbond SOI wafer by the CSMC Corporation. Figure 6 shows the micrograph of the SOI LDMOS test key arrays. The SEM cross-section of channel and gate regions was shown in Fig. 7. The FOX structure and field plate were the same as designed in Fig. 2(b).

In order to measure the large current, several parallel MCUs were adopted to measure the electrical characteristics of the SOI LDMOS. Figure 8 shows the measured results of the off-state breakdown characteristics. The breakdown voltage reached 680 V at the implant dose of 9.0×10^{12} cm^{-2} of the drift region, which is in close agreement with our simulation result, as shown in Fig. 5. The output characteristics are shown in Fig. 9, where the gate bias was changed from 2 to 6 V. The I–V curves were flat at low drain bias, but a self-heating effect[19] was observed with the increase of the drain voltage. The threshold voltage was extracted to be 1.9 V (V_{ds} = 0.1 V), and the specific on-resistance was 8.2 Ω·mm^2 (V_{gs} = 10 V).

Breakdown voltage and specific on-resistance of various devices including some previous work by other researchers and our proposed device are listed in Table 2. The breakdown voltage of our proposed LDMOS was higher than others; the specific on-resistance was only slightly higher than that of the SOCOS LDMOS and lower than that of the graded, thick SOI and

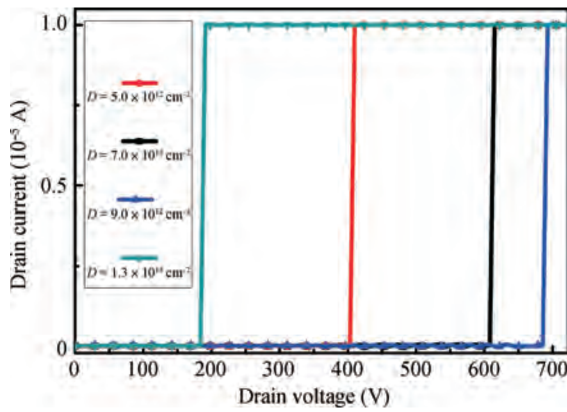

Fig. 9. The measured results of reverse breakdown characteristics.

Table 2. Breakdown voltage and specific on-resistance of various devices.

Device	BV (V)	R_{on} ($\Omega\cdot mm^2$)
Proposed LDMOS	680	8.2
SOCOS LDMOS[13]	600	7.6
Graded LDMOS[20]	620	22
Thick SOI LDMOS[21]	600	20

bulk Si LDMOS.

4. Conclusion

680 V high breakdown voltage LDMOS structures were designed and fabricated on Simbond SOI wafers with a 1.5 μm top silicon and a 3 μm buried oxide layer. A new FOX structure was formed by using an “oxidation-etch-oxidation” process. Dual field plate and optimized drift region implantation for linear-gradient doping was adopted. Experimental results demonstrated that the proposed design not only optimized the fabrication processes but also improved the electrical characteristics of the device.

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