Enhancement-mode InAlN/GaN MISHEMT with low gate leakage current*

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Abstract: We report an enhancement-mode InAlN/GaN MISHEMT with a low gate leakage current by a thermal oxidation technique under gate. The off-state source–drain current density is as low as $\sim 10^{-7}$ A/mm at $V_{GS} =$ 0 V and $V_{DS} = 5$ V. The threshold voltage is measured to be $+0.8$ V by linear extrapolation from the transfer characteristics. The E-mode device exhibits a peak transconductance of 179 mS/mm at a gate bias of 3.4 V. A low reverse gate leakage current density of 4.9×10^{-7} A/mm is measured at $V_{GS} = -15$ V.

Key words: enhancement-mode; InAlN/GaN HEMT; threshold voltage; thermal oxidation; gate leakage
DOI: 10.1088/1674-4926/33/6/064004 **PACC:** 7340N; 7360L

1. Introduction

As an alternative to AlGaN/GaN, InAlN/GaN based devices have recently attracted more attention and are recognized as good candidates for high power[1] and high speed[2] applications. There are two advantages of the InAlN/GaN heterostructure. One advantage is that a stress free interface, which is expected to improve a device's reliability, could be achieved by using a proper indium composition, i.e. $In_{0.17}Al_{0.83}N$/GaN. Another advantage is that much stronger spontaneous polarization existing in an InAlN/GaN heterostructure induces a higher two-dimentional electron gas (2DEG) density in the channel, which means radio-frequency (RF) performances could be much improved by scaling down gate length as well as the InAlN barrier thickness. Lee *et al.*[3] reported an InAlN/GaN HEMT with a very thin barrier of 4.5 nm, which shows an f_T of 245 GHz. Moreover, an InAlN/GaN HEMT with a barrier thickness of as little as 3 nm has been reported, which shows good thermal stability even after a 30-min 1000 ℃ thermal stress[4]. However, the inherent larger gate leakage current limits the application of InAlN HEMTs. The insertion of a thin dielectric layer between the gate metal and the InAlN barrier to form an MIS structure was proven to be a practical approach to effectively reduce gate leakage. Gate dielectric layers of ZrO_2, HfO_2 and Al_2O_3 by using atomic layer deposition (ALD)[4], or metal–organic chemical vapor deposition (MOCVD)[5] and other methods[6, 7] have been demonstrated recently. On the other hand, some applications, such as power switches, require normally-off operation (i.e. E-mode) to simplify circuit topology and guarantee a sufficient safety margin. So far E-mode InAlN/GaN HEMTs have been demonstrated by using a recessed-gate structure[8], a depletion structure with a fluorine-based plasma treatment[9] and so on[10].

In this paper, we show an E-mode InAlN/GaN MISHEMT with a very low reverse gate leakage by using a thermal oxidation technique. The fabricated device has a threshold voltage (V_{TH}) of 0.8 V with a low reverse gate leakage current of 4.9 $\times 10^{-7}$ A/mm @ -15 V.

2. Experiment

In this work, an InAlN/GaN heterostructure was grown on a 2 inch (0001) sapphire substrate by metal–organic chemical vapor deposition (MOCVD). The epitaxial structure consists of a 2-μm-thick GaN epilayer, 1.0-nm-thick AlN spacer and a 7-nm-thick $In_{0.17}Al_{0.83}N$ barrier layer. Hall measurement results show a 2DEG density of 2.1×10^{13} cm^{-2} and electron mobility of 1140 cm^2/(V·s), corresponding to a sheet resistance of 265 Ω/□.

Device processing was initiated by deposition of 150 nm of SiN_x in a PECVD system. Then a 0.3-μm-long gate window was defined by using electron beam lithography followed by reactive ion etching (RIE) in a SF_6/CHF_3/Ar gas mixture. To ensure the SiN_x is removed clearly in the gate window, 20 s over etching was conducted. Then device mesa isolation was formed by two-step dry etching. The first step dry etching of RIE was used to remove 150 nm SiN_x. The second step dry etching of $Cl_2 : BCl_3$ based ICP was used to remove the $In_{0.17}AlN_{0.83}$ layer and $\sim$150 nm GaN buffer. Gate oxidation was performed at 700 ℃ for 60 min in pure ambient oxygen (shown in Fig. 1). Source and drain ohmic contacts were formed by E-beam evaporation of Ti/Al/Ni/Au (20/160/50/100 nm) multilayers followed by a rapid thermal annealing at 750 ℃ for 60 s in N_2. Finally, Ni/Au (50/250 nm) deposition and liftoff were conducted to form the gate metallization and contact pads. The gate length, gate–source spacing and gate–drain spacing are 0.3 μm, 2 μm and 10 μm respectively.

3. Results and discussion

Figure 2 shows the transfer characteristics of the E-mode

* Project supported by the National Natural Science Foundation of China (Nos. 10990102, 60890192, 60876009).
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Received 8 November 2011, revised manuscript received 5 January 2012 © 2012 Chinese Institute of Electronics

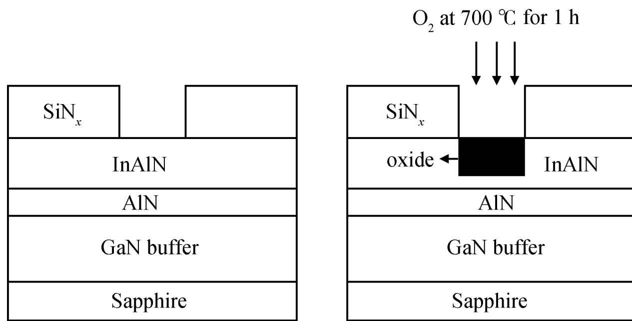

Fig. 1. Schematic cross section of the InAlN/GaN MISHEMT describing the device process.

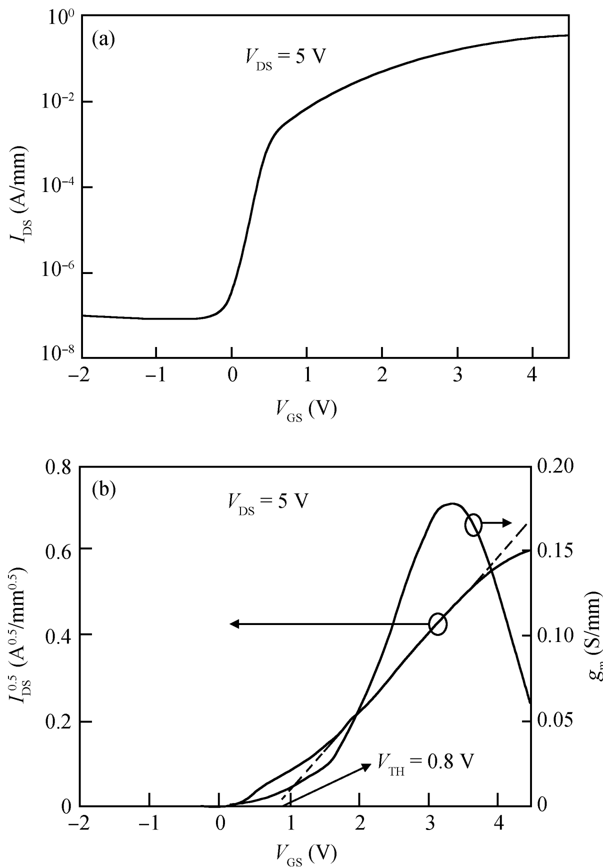

Fig. 2. Transfer characteristics of the E-mode InAlN/GaN MISHEMT shown in (a) logarithmic scale and (b) linear scale.

InAlN/GaN HEMT in semi-logarithmic coordinates. The E-mode device is completely pinched off with a drain current of as little as 3.4×10^{-7} A/mm at $V_{GS} = 0$ V and $V_{DS} = 5$ V, indicating true E-mode operation. According to the definition of the threshold voltage[11], the V_{TH} of the E-mode InAlN/GaN MISHEMTs is extracted to be 0.8 V. The positive threshold voltage is attributed to two reasons, i.e. oxidation and fluorine-based plasma overetching[12]. For this device, part of the InAlN barrier underneath the gate metal has been oxidized to form mixed indium and aluminum oxides, the remaining InAlN barrier layer was thinned down, the spontaneous polarization of InAlN/GaN is weakened, and causes the reduction of 2DEG induced by spontaneous polarization[4]. As described in the section of device fabrication, SF_6-based plasma overetching was conducted to confirm that the SiN_x is clearly removed during gate window opening. Some fluoride ions should be implanted into the InAlN/GaN material, which also results in a positive shift of V_{TH}[10]. The peak transconductance of the E-mode device is measured to be 179 mS/mm at $V_{GS} = 3.4$ V, as shown in Fig. 2. The relatively lower transconductance attributes to degradation of electron mobility during fluorine-based dry etching and thermal oxidation, indicating that further process optimization is needed.

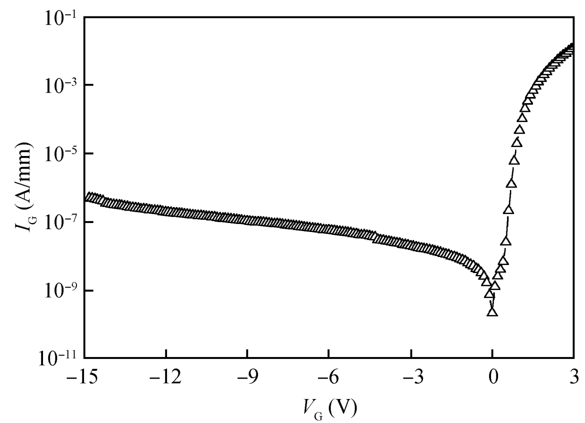

Fig. 3. I_G–V_G characteristics of E-mode MISHEMT fabricated by thermal oxidation at 700 ℃ in an O_2 atmosphere.

Figure 3 shows the I_G–V_G characteristics of E-mode MISHEMT fabricated by thermal oxidation at 700 ℃ in pure O_2 atmosphere. At a gate bias of -15 V, the fabricated E-mode MISHEMT shows a low reverse gate leakage current of 4.9×10^{-7} A/mm. During the 700 ℃ oxidation, the surface defects in the InAlN layer, such as In-pits[12], which are the main gate leakage paths, were passivated. After oxidation, a layer of a mixture of In and Al oxides was formed by partially oxidizing the InAlN barrier layer. The oxide layer has a higher gate barrier height that suppresses defect assisted electron emission[13]. As a result of defect passivation and enhanced barrier height, the gate leakage current density is significantly reduced. Compared to previously published results of E-mode InAlN/GaN HEMTs[9, 14], where 0.1 A/mm and 10^{-4} A/mm were shown respectively at a gate bias of -15 V, the gate leakage of 4.9×10^{-7} A/mm @ $V_{GS} = -15$ V shown in this work is much lower, which implies that thermal oxidation could be an effective approach to suppress reverse gate leakage in InAlN/GaN based devices.

The typical output characteristics of the MISHEMT are shown in Fig. 4. The maximum saturated drain current density is 0.3 A/mm @ $V_{GS} = 4$ V. The linear region of the fabricated device shows nonlinear characteristics, which possibly originates from the nonlinear ohmic contacts. Fluorine-based plasma dry etching was applied to remove the SiN_x layer above the ohmic contacts' windows before deposition of the ohmic metals. To make sure that the SiN_x layer is clearly removed, a fluorine-based plasma over etch was conducted. And so negative charges were implanted into the InAlN/GaN to hold back electron tunneling, which causes nonlinear ohmic contacts. To improve the device performance, process flow should be optimized to minimize ohmic contacts.

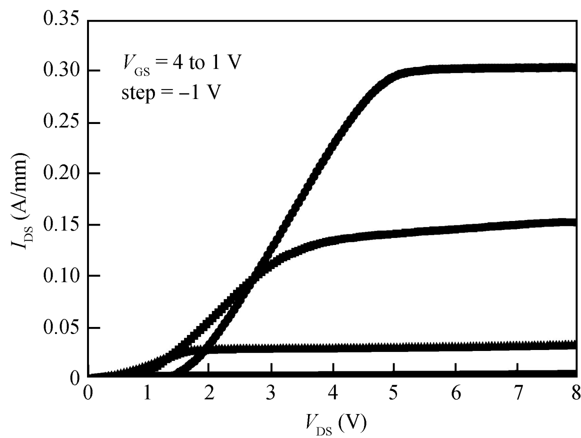

Fig. 4. Typical output characteristics of the E-mode InAlN/GaN MISHEMT.

4. Conclusion

A novel approach to fabricating the enhancement-mode InAlN/GaN MISHEMT has been shown by using thermal oxidation and a fluorine-based plasma treatment. The fabricated E-mode InAlN/GaN HEMT shows a V_{TH} of 0.8 V and an off-state drain current of 10^{-7} A/mm at $V_{GS} = 0$ V and $V_{DS} = 5$ V. In addition, due to the thermal oxidation, the E-mode MISHEMT exhibits a low gate leakage current of 4.9×10^{-7} A/mm at V_{GS} of -15 V. The investigation of this novel approach is just at the beginning, more research work, such as, process optimization, process repeatability and device reliability, should be carried out in the future.

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