High voltage generator circuit with low power and high efficiency applied in EEPROM*

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Abstract: This paper presents a low power and high efficiency high voltage generator circuit embedded in electrically erasable programmable read-only memory (EEPROM). The low power is minimized by a capacitance divider circuit and a regulator circuit using the controlling clock switch technique. The high efficiency is dependent on the zero threshold voltage (V_{th}) MOSFET and the charge transfer switch (CTS) charge pump. The proposed high voltage generator circuit has been implemented in a 0.35 μm EEPROM CMOS process. Measured results show that the proposed high voltage generator circuit has a low power consumption of about 150.48 μW and a higher pumping efficiency (83.3%) than previously reported circuits. This high voltage generator circuit can also be widely used in low-power flash devices due to its high efficiency and low power dissipation.

Key words: CTS charge pump; high efficiency; high voltage generator circuit; low power; EEPROM; oscillation; zero V_{th}

DOI: 10.1088/1674-4926/33/6/065006 **EEACC:** 2570

1. Introduction

With the development of radio frequency identification (RFID), embedded electrically erasable programmable read-only memory (EEPROM) meets the challenge of high speed, large capacity, high density and especially low power consumption, which has become one of the dominant design aspects for EEPROM[1]. High voltage generator circuits consume a non-negligible power in EEPROM, which provides high voltage that is higher than the power supply voltage for erase/write operations. Therefore the purpose of this paper is to design a low power consumption and high efficiency high voltage generator circuit which can be extensively used in low power non-volatile semiconductor EEPROM.

The designed high voltage generator circuit structure with several functional blocks is shown in Fig. 1. The high voltage generator circuit consists of clock driver circuit, which contains an oscillator and a non-overlapping clock, a charge pump and a voltage regulator, which is composed of a divider, a comparator and a bandgap reference.

The on-chip oscillator generates the 5 MHz clock. A non-overlapping clock that produces a two-phase clock is used for the charge pump clock driving signals. The charge pump produces high voltage by pumping charges from the supply voltage to high voltage. The divider and comparator can stabilize high voltage and produce a feedback signal. When V_{DDHV} is more than 14 V, the feedback signal will be higher than V_{ref}, so the comparator output will be high and go through the logic control, which will make the non-overlapping clock stop working. Similarly, when V_{DDHV} is less than 14 V, the feedback signal will be lower than V_{ref}, so the comparator output will be low and go through the logic control, causing the non-overlapping clock to continue working and drive the charge pump.

The charge pump is the critical module in the system. Most charge pump circuits are based on Dickson's design, which uses capacitance to transfer the charges from one stage to the next. However, the efficiency of a Dickson charge pump is low because of the body effect and V_{th} limiting the pumping gain[2].

In recent decades, several modifications of Dickson's charge pump have been proposed, such as the floating-well charge pump[3], the four-phase clock charge pump[4], and the dynamic bulk charge pump[5]. However, the floating-well charge pump can generate body current; the four-phase clock generator is complex in realization; and the dynamic bulk charge pump easily generates the latch-up problem.

In this paper, a zero V_{th} MOSFET can reduce the effect of V_{th} and the charge transfer switch technique can eliminate the feedback current; thus the pumping efficiency is sharply increased. Furthermore, a capacitance divider is utilized to reduce the power. Combined with a voltage regulator, the V_{DDHV} can be stable and the fluctuation range is 21 mV. In addition, when the charge pump output is V_{DDHV}, the clock and charge pump turn off and power dissipation is also decreased.

2. High voltage generator

2.1. Oscillator

In this paper, a voltage control oscillator is proposed. The schematic of the oscillator is shown in Fig. 2. The basic principle is as follows: MN1/MP1 constitutes an inverter; MN2/MP2 is the mirror current source which limits the current flowing through MN1/MP1. MN0/MP0 has the same drain current, which is controlled by the input voltage and is mirrored to each level.

The frequency of the oscillator is given by the equation:

$$f = \frac{1}{NT_D} = \frac{I_D}{NC_{equ}V_{DD}}, \quad (1)$$

* Project supported by the National Natural Science Foundation of China (No. 61072010).

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Received 14 November 2011, revised manuscript received 9 January 2012

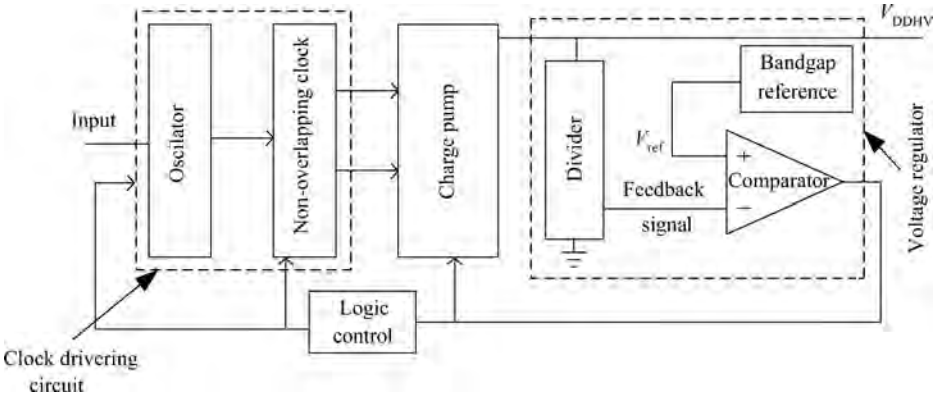

Fig. 1. High voltage generator circuit structure.

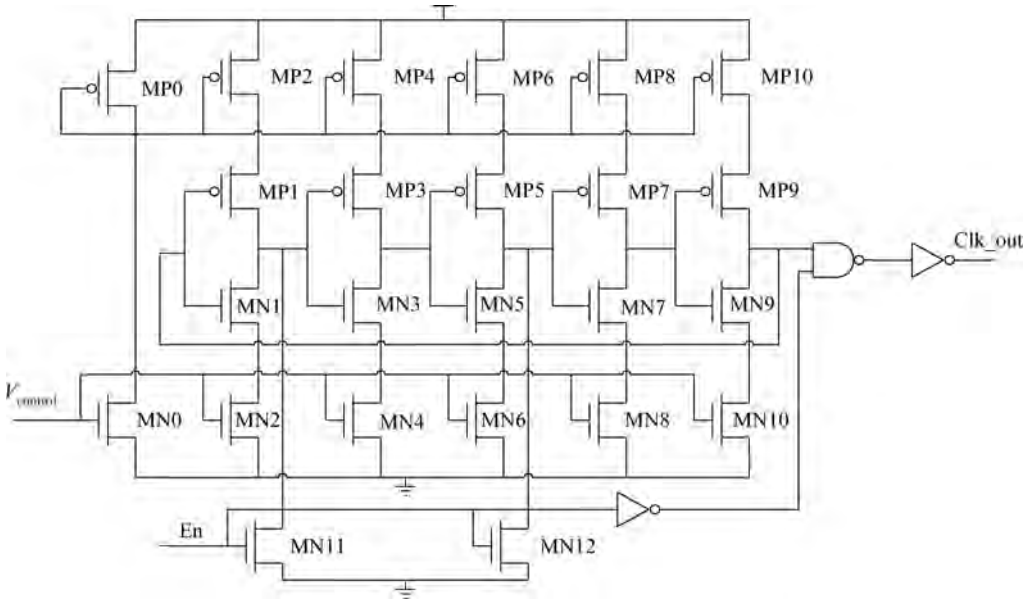

Fig. 2. Oscillator schematic.

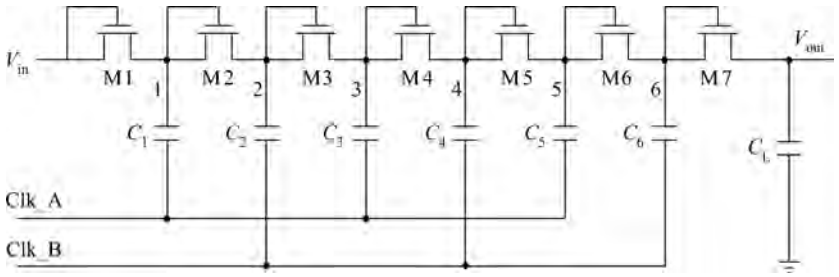

Fig. 3. Dickson charge pump.

where N is the stage number, T_D is the delay, C_{equ} is the single-stage output equivalent capacitance, and V_{DD} is the supply voltage.

2.2. Zero V_{th} charge pump

As illustrated in Fig. 3, the Dickson charge pump is composed of the diode-connected MOSFETs M1–M7, the pumping capacitors C_1–C_6 and the load capacitor C_L. It pumps the voltage from the input V_{DD} to output V_{DDHV} controlled by non-overlapping clock signals Clk_A and Clk_B. The output voltage is presented in Eq. (2)[6].

$$V_{out} = V_{DD} + N\left[\frac{C}{C+C_S}V_{DD} - V_{th} - \frac{I_{Load}}{f(C+C_S)}\right], \quad (2)$$

where V_{th} is the threshold voltage, C is the pumping capacitance, C_s is the parasitic capacitance, f is the clock frequency, and I_{Load} is the output current.

From Eq. (2), to increase pumping efficiency, eliminating the threshold voltage drop and decreasing the load current are

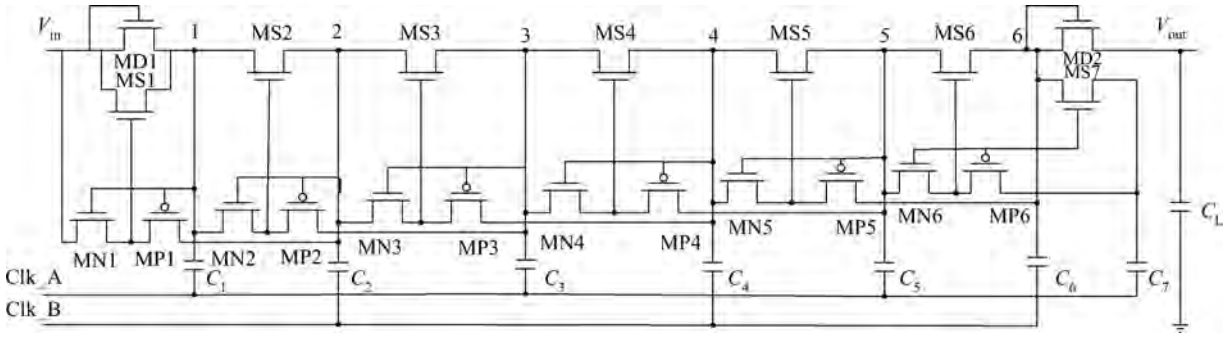

Fig. 4. Improved CTS charge pump schematic.

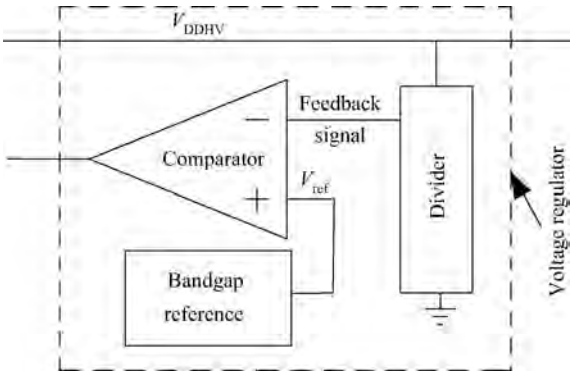

Fig. 5. Voltage regulator architecture.

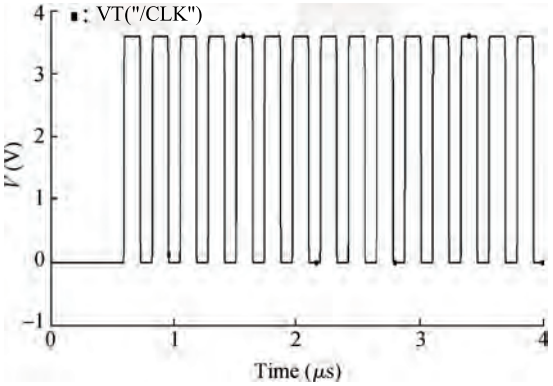

Fig. 6. Simulated oscillator waveform.

critical. In this paper, an improved CTS charge pump is presented. The schematic is shown in Fig. 4.

In order to understand how the high pumping efficiency is implemented, we describe the operation of the improved CTS charge pump with the second stage as an example. When Clk_A is high and Clk_B is low, MN2 is off and MP2 is on, the gate voltage of charge transfer switch MS2 is V_{DD}, so MS2 turns on completely. In addition, MS2 is a zero V_{th} MOSFET, thus the node2 voltage is V_{DD}. When Clk_A is low and Clk_B is high, MN2 is on and MP2 is off, the gate voltage of charge transfer switch MS2 is 0 V, so MS2 turns off completely. And the charge cannot be fed back. Similarly the voltage pumps from one stage to next stage.

There are two advantages of the improved CTS charge pump. A zero V_{th} MOSFET is adopted to conquer the V_{th} drop at every node. Moreover, the charge transfer switches can turn on/off completely and feedback current is reduced. Therefore pumping efficiency is enhanced.

Pumping efficiency can be defined as[7]:

$$\eta = \frac{I_{\text{Leak}} V_{\text{DDHV}}}{I_{\text{Power}} V_{\text{DD}}} = \frac{V_{\text{DDHV}}}{(N+1)V_{\text{DD}}}, \tag{3}$$

where V_{DDHV} is the output voltage and V_{DD} is the supply voltage. The charge pump can operate at 5 MHz frequency with 1 pF pumping capacitance. Simulated by SPECTRE 0.35 μm EEPROM CMO process, the pumping efficiency reaches 83.3%.

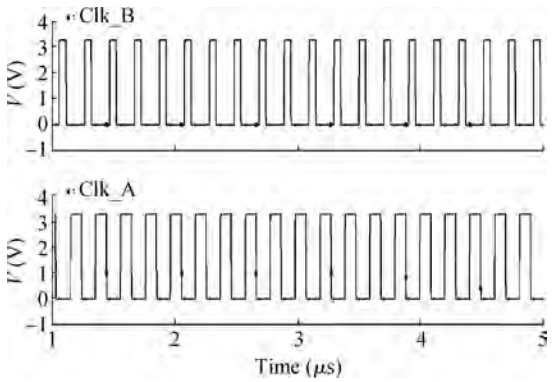

Fig. 7. Simulated non-overlapping clock waveform.

2.3. Voltage regulator

To stabilize the high voltage and reduce the power consumption, a voltage regulator is used and illustrated in Fig. 5. When the feedback signal produced by the bandgap reference reaches higher than V_{ref}, the comparator and logic control circuit work together to turn off the clock. Similarly, the when feedback signal is lower than V_{ref}, the comparator and logic control circuit work together and continue driving the clock and charge pump. V_{ref} is determined by V_{DDHV} and the value is 1.5 V. By controlling the on/off of clock and charge pump, low power is obtained. Furthermore, when a capacitance divider is applied, there is no current dissipation.

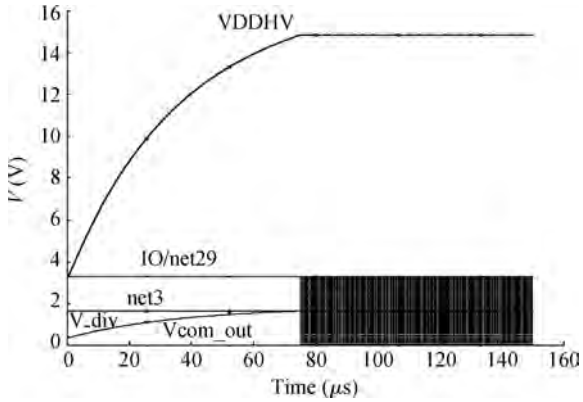

Fig. 8. Simulated waveform of the high voltage generator circuit.

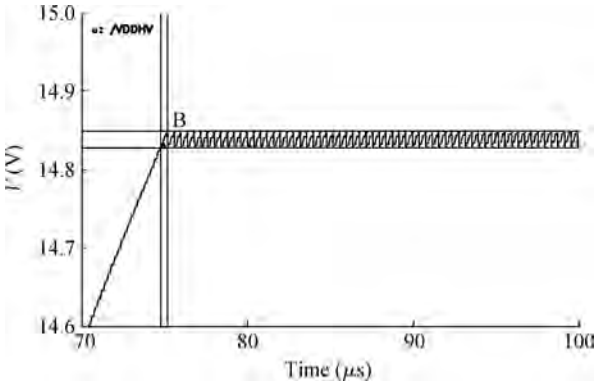

Fig. 9. Simulated waveform of high voltage fluctuation.

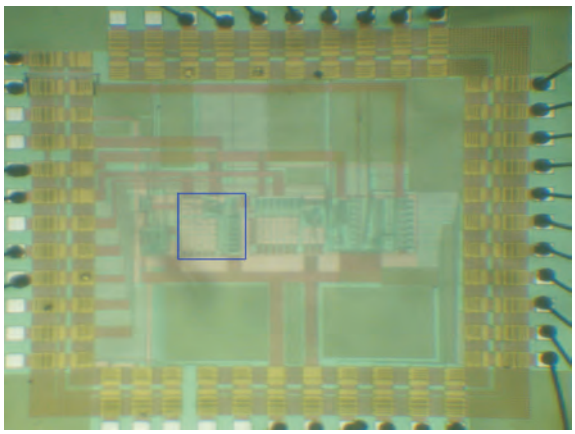

Fig. 10. Micrograph of the test chip.

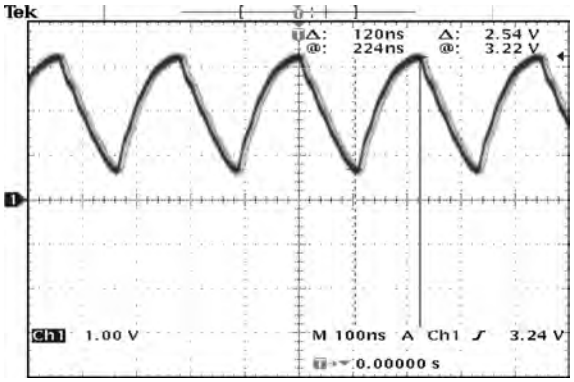

Fig. 11. Measured oscillator waveform.

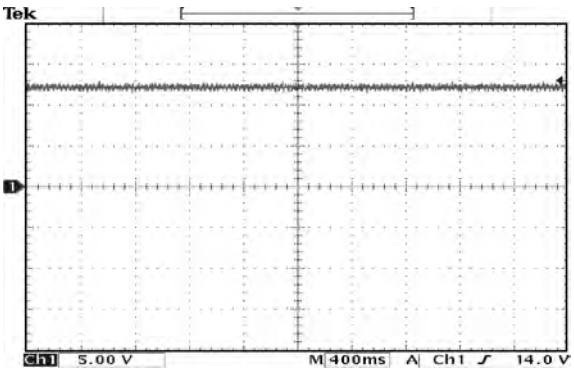

Fig. 12. Measured waveform of the proposed high voltage generator circuit.

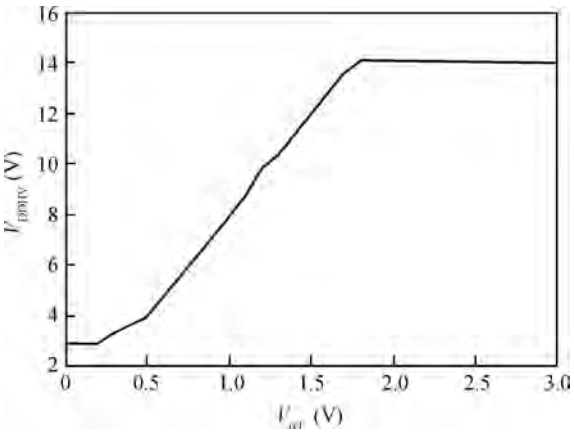

Fig. 13. Measured result of the high voltage generator circuit with $V_{\rm ref}$.

3. Experimental results

3.1. Simulation results

We examined the performance of the presented high voltage generator circuit by simulation with SPECTRE based on a 0.35 μm EEPROM CMOS process. Figure 6 shows the simulated oscillator waveforms with $V_{\rm in} = 1.5$ V. The simulation result of the non-overlapping clock is shown in Fig. 7.

The high voltage generator circuit with 3.3 V supply voltage, 5 MHz clock frequency and a capacitor load of 40 pF is shown in Fig. 8. Moreover, EEPROM requires 14 V high voltage for write/erase operations according to the process model, a voltage regulator controls the high voltage stably at 14 V with a small ripple. Figure 9 exhibits the fluctuation of the high voltage.

3.2. Measured results

The high voltage generator circuit is part of an EEPROM that has been fabricated in a 0.35 μm EEPROM CMOS process. Figure 10 shows the microscopic image of the test chip. The proposed high voltage generator circuit is shown in the box.

Table 1. Comparison of the high voltage generator circuits.

Parameter	Structure in Ref. [3]	Structure in Ref. [4]	Proposed structure
Process (μm)	0.5	0.35	0.35
Supply power (V)	2	1.8	3.3
High voltage generator method	Floating well	Four-phase clock	Improved CTS
V_{DDHV} (V)	15	15	14
Power consumption (μA)	121 @ 5 V	68 @ 15 V	150.48 @ 15 V
Number of stage	10 stage	—	6 stage

Compared with the simulation result, Figure 11 shows an oscillator with 1.4 V input voltage. Due to the limitation of oscilloscope load capacitance (16 pF), the measured result is not a square wave but the frequency can be adjustable, which conforms to the design requirement. Figure 12 shows the high voltage generator output voltage waveform. A high voltage of up to 13.6 V can be reached, which meets the erase/write requirement in EEPROM. Measurement results of the high voltage generator circuit with a V_{ref} wave input are shown in Fig. 13. Table 1 lists the comparison results of the proposed high voltage generator circuits with other circuits.

4. Conclusion

In this paper, a high voltage generator circuit with an on-chip oscillator, a charge pump and a voltage regulator has been implemented and investigated. Measured results show that the presented charge pump system has better performance in efficiency (83.3%) and power dissipation (150.48 μW). The results show good accordance with the simulation. It is suitable for embedded EEPROM with low power and low voltage.

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