A 2.5 mW 370 mV/pF high linearity stray-immune symmetrical readout circuit for capacitive sensors

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Abstract: A stray-insensitive symmetrical capacitance-to-voltage converter for capacitive sensors is presented. By introducing a reference branch, a symmetrical readout circuit is realized. The linear input range is increased, and the systematic offsets of two input op-amps are cancelled. The common-mode noise and even-order distortion are also rejected. A chopper stabilization technique is adopted to further reduce the offset and flicker noise of the op-amps, and a Verilog-A-based varactor is used to model the real variable sensing capacitor. Simulation results show that the output voltage of this proposed readout circuit responds correctly, while the under-test capacitance changes with a frequency of 1 kHz. A metal–insulator–metal capacitor array is designed on chip for measurement, and the measurement results show that this circuit achieves sensitivity of 370 mV/pF, linearity error below 1% and power consumption as low as 2.5 mW. This symmetrical readout circuit can respond to an FPGA controlled sensing capacitor array changed every 1 ms.

Key words: capacitance-to-voltage converter; chopper stabilization; high linearity; low power
DOI: 10.1088/1674-4926/33/6/065001 **EEACC:** 1285; 11801; 11824

1. Introduction

Capacitive sensors are widely used in a variety of measuring and controlling systems, such as accelerometers, pressure meters and positioners, which convert physical, chemical or mechanical quantities into capacitance change. Currently, the microsensor market is rapidly growing as more and more microsensors are integrated into portable electronic products to meet customers' needs. Capacitive microsensors have become very attractive due to high sensitivity, a simple structure, inherently low temperature sensitivity and low power consumption[1].

A certain capacitive microsensor system consists of two main parts: a capacitive sensor and a readout circuit. The capacitive sensor is generally composed of a fixed component and a variable portion which changes responding to an excitation. The readout circuit often plays a critical role because it limits the overall system performance. There are mainly four different topologies for capacitance-to-voltage converter (CVC): an AC-bridge with a voltage amplifier, a transimpedance amplifier, a transcapacitance circuit and a switched-capacitor circuit[2]. Several non-ideal factors are the challenges in circuit design. The first of these are the stray capacitors, which lie in the microsensors and input readout circuits. Stray capacitors might be even larger than under-test capacitance and fluctuate in value. Second is the offset of op-amps, both systematic and random, which directly affects the output voltage of the circuit. Third is the low frequency noise of the op-amps, which degrades the dynamic range and limits resolution.

Several research groups have already developed a CVC sensor interface circuit. Firstly, the basic capacitance readout circuit based on charge transfer is put forward in Ref. [3]. Its linear range is limited by the base capacitance of under-test capacitive sensors, and the op-amp offset also directly affects its accuracy. A modified interface circuit is proposed in Ref. [4]. This only measures the difference capacitance, which can apply to a small changing range with a large base capacitance. The op-amp offset problem still affects the accuracy. A differential measuring circuit has been implemented in Ref. [5]. This uses the offset cancellation scheme to improve its accuracy. However, the linear range is still limited by the base capacitance. A differential stray-immune interface circuit with reference branch is proposed in Ref. [6]. The circuit architecture is too complicated and consumes more power, and the resolution is limited by the dominated flicker noise of the op-amp.

In this paper, a stray-immune symmetrical transimpedance CVC is designed to measure capacitive sensors, especially single-ended capacitive sensors. All the mentioned non-ideal effects are analyzed. The virtual ground of the positive terminals of the op-amps guarantees that the charge across the stray capacitors remains constant and eliminates its effect on output voltage. A reference branch is introduced to realize this symmetrical circuit. The systematic offsets of the two op-amps are cancelled. Moreover, it helps to improve the linearity, provide large output swing and reject common-mode noise and even-order distortions. The chopper stabilization technique is also employed to reduce $1/f$ noise and thus improve its resolution.

2. Circuit architecture

Some capacitive microsensors, like pressure sensors, are single-ended. The novel CVC readout circuit presented here is designed for single-ended capacitive sensors with a larger measuring range and high linearity. It can also easily be changed to measure a differential capacitive sensor, as the reference capacitor, C_s, is substituted by the negative part of the differential sensor.

The architecture of the proposed measuring circuit is

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Received 22 November 2011, revised manuscript received 13 February 2012

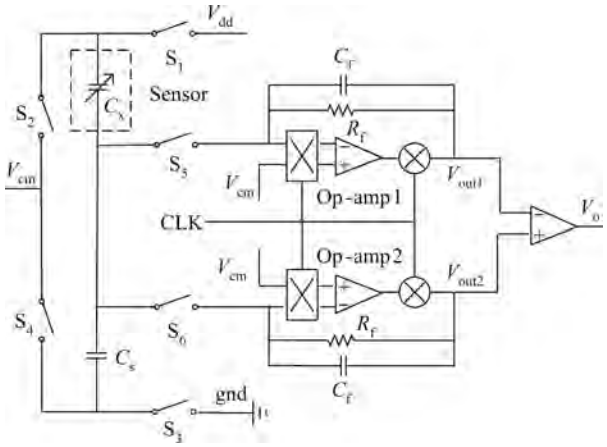

Fig. 1. Proposed symmetrical readout circuit with reference branch.

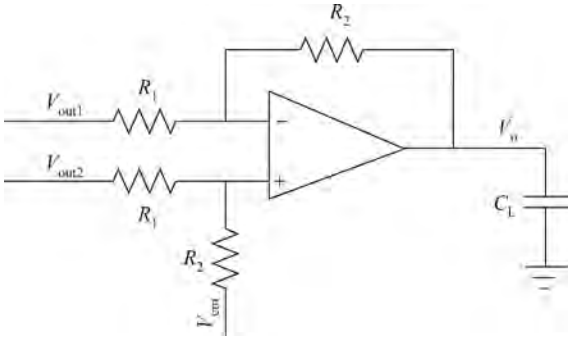

Fig. 2. The realization of the subtracter using resistive feedback.

shown in Fig. 1. The reference capacitance value, C_s, equals the base capacitance value of the under-test capacitors, C_x. S_1 to S_6 are switches controlled by a two-phase non-overlap clock. Two op-amps measure both the charging and discharging currents and convert them to voltage outputs. Since the circuit operates with a single power supply, an internal reference voltage, V_{cm}, is set as $V_{dd}/2$ and generated on-chip.

In the charging period, S_1, S_3 and S_5 are closed, while S_2, S_4 and S_6 are opened. For a typical charging period, the total charge transferred to op-amp 1 is given by:

$$\Delta Q = (C_x - C_s)\frac{V_{dd}}{2} = \Delta C \frac{V_{dd}}{2}. \tag{1}$$

Stray capacitors from the bottom plate of the sensor and input terminals of the op-amps are always parallel with virtual ground. They do not affect the final output. Stray capacitors from the top plate of the sensor are either parallel with the virtual ground or power supply. The charging or discharging current will not flow through the op-amps, therefore the dc output is not affected by all the stray capacitors. The proposed circuit is stray-immune. The op-amp with its feedback resistor R_f and capacitor C_f works as a low pass filter. Compared to the switching frequency, which is around several megahertz, the charge variation in each period can be treated as an equivalent dc current. The dc output voltage, V_{out1}, is given as:

$$V_{out1} = V_{cm} + \frac{V_{dd}}{2} f \Delta C R_f. \tag{2}$$

Similarly, for the discharging period, the final output voltage V_{out2} can also be deduced. The last subtracter is realized by the differential-to-single circuit shown in Fig. 2, with a gain of R_2/R_1. So the ideal final output voltage V_o is:

$$V_o = V_{cm} + \frac{R_2}{R_1} V_{dd} f \Delta C R_f. \tag{3}$$

The ideal sensitivity of this CVC circuit is given by:

$$\frac{\Delta V_o}{\Delta C} = \frac{R_2}{R_1} V_{dd} f R_f. \tag{4}$$

When the chopper technique is not used, considering the offset difference of op-amp 1 and op-amp 2, which is defined as ΔV_{os}, the final output voltage is modified as:

$$V_o = V_{cm} + \frac{R_2}{R_1}\big[\Delta C(V_{dd} + 2\Delta V_{os}) f R_f + \Delta V_{os}(1 + 4C_s f R_f)\big]. \tag{5}$$

Though the two op-amps offset difference affects the resolution and baseline drift, it does not affect the linearity. A random offset still exists while the systematic offsets of the two op-amps are cancelled. Compared with the circuit architecture proposed in Refs. [3–6], this symmetrical architecture doubles the sensitivity, improves the linearity and reduces the baseline drift. Common-mode voltage variation and even order distortions are reduced. Meanwhile, the chopper stabilization technique is adopted to reduce the op-amp flicker noise and offset problems.

3. Circuit design

3.1. Op-amp designed with the chopper stabilization technique

The final dc output is greatly affected by $1/f$ noise and offsets of the op-amps. The chopper stabilization technique is an effective method to relieve these problems[7]. The architecture of single-ended op-amps with chopping is shown in Fig. 3.

The input dc voltage V_x is first modulated to a higher frequency by mixer 1. Then it is amplified and demodulated back to dc voltage by mixer 2. A low pass filter after the op-amp is used to eliminate the chopped offset and noise. The additional two mixers, realized by the MOS switch, do not increase static current or power consumption. The chopped op-amp is a two-stage amplifier with miller compensation. PMOS transistors are used as differential inputs for better matching and noise performance.

The simulation results of the input referred voltage noise, with chopper frequency at 2 MHz and without chopper technique, are shown in Fig. 4. It is clear that $1/f$ noise is greatly suppressed, and is moved to chopping frequency using the chopper stabilization technique. The in-band noise is greatly reduced, and the sensitivity of the CVC readout circuit is not affected by the chopper technique. Thus the resolution and minimum detectable capacitance is improved.

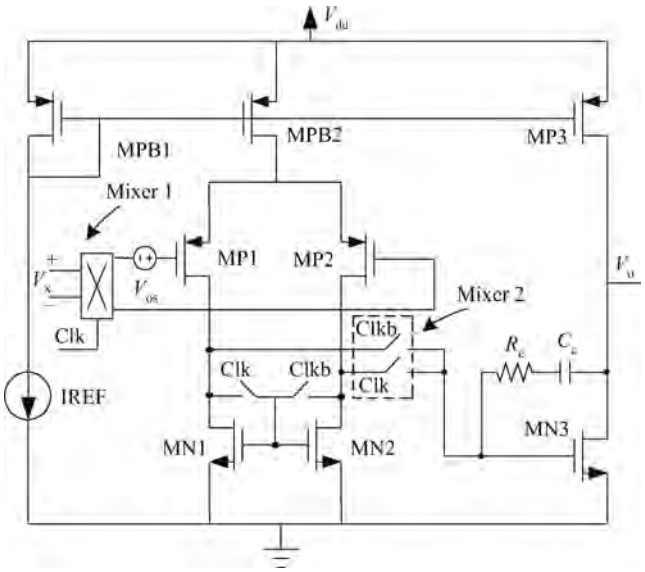

Fig. 3. Op-amp design with chopper technique.

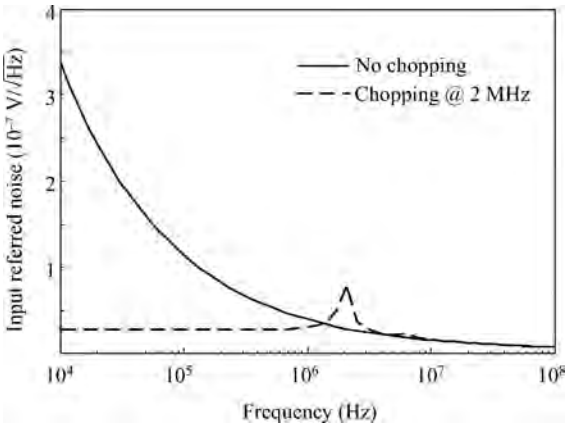

Fig. 4. Input referred voltage noise with and without the chopper stabilization technique.

3.2. Clock and switch

All the switches in Fig. 4 are controlled by clock signals, which are generated by an off-chip crystal oscillator. A two-phase non-overlap clock is adopted to guarantee that all the charge is not inadvertently lost. Moreover, in a charging or discharging period, switches that are directly connected to op-amps should be closed a short time earlier than the other switches to ensure that all the charge is transferred to the op-amps. The four-phase clock generator and time sequence are shown in Fig. 5. Higher switching frequency requires higher power consumption, lower on-resistance of the switch and smaller feedback resistance, while lower switching frequency demands larger feedback resistance, consuming more area.

All the MOS switches encounter the problems of clock feedthrough and charge injection. Dummy switches are used to minimize these problems[8]. Minimum feature length is used to minimize the parasitic capacitance. The on-resistance of the switch is determined by the settling error and switching frequency. Then, switch width is determined according to the on-resistance of the MOS switch.

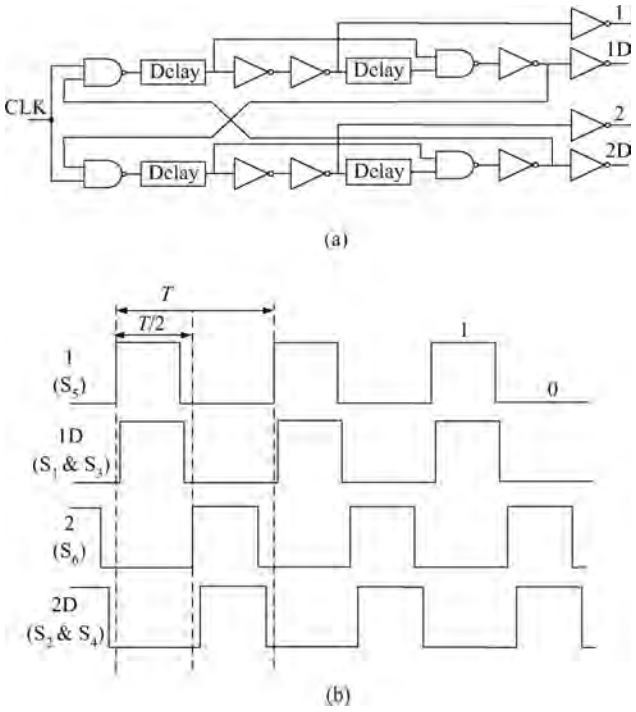

Fig. 5. (a) A four-phase clock generator and (b) a four-phase clock generator.

$$\frac{W}{L} = \frac{1}{\mu_n C_{ox}(V_{dd} - V_{th})R_{on}}. \tag{6}$$

3.3. Capacitance modeling and fabrication

For a real capacitive sensor, its capacitance is time-varying. In order to simulate the transient response of the readout circuit, a simple varactor model is implemented in Verilog-A[9]. The model has four terminals, in which two of them represent a capacitor's terminal and the other two are connected with external controlling voltage. The Verilog-A model is based on the following equations:

$$C_x = C_s + C_V V_{in}, \tag{7}$$

$$I_{C_x} = C_x \frac{dV_{C_x}}{dt}. \tag{8}$$

C_s is the initial value of the capacitive sensor, which is constant, C_V is the capacitance–voltage ratio coefficient, and V_{in} is the controlling voltage. Without loss of generality, the CVC circuit is designed to measure a capacitance that changes from 0 to 5 pF. Thus, C_s is set as 2.5 pF and C_V is chosen as 2.5 pF/V. The amplitude of controlling voltage is 1 V.

Frequency variation of capacitive sensors is generally around several hundred hertz. The response speed of this CVC circuit is verified by transient simulation, as shown in Fig. 6. The under-test capacitance, C_x, changes with a maxim frequency of 1 KHz and the output voltage, V_o, can respond correctly.

The variable capacitor is implemented by an on-chip MIM capacitor array, as shown in Fig. 7. It changes from 0 to 5 pF with a step of 0.25 pF. A 5 bit decoder is designed to reduce

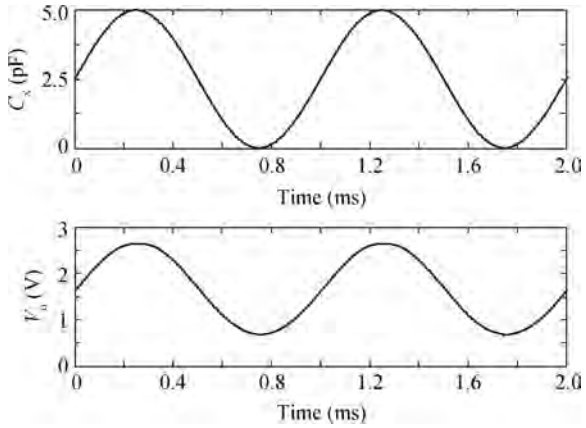

Fig. 6. Transient output voltage in response to a sinusoidal changing sense capacitance.

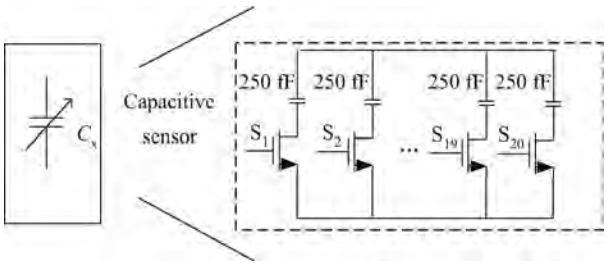

Fig. 7. An on-chip capacitance array.

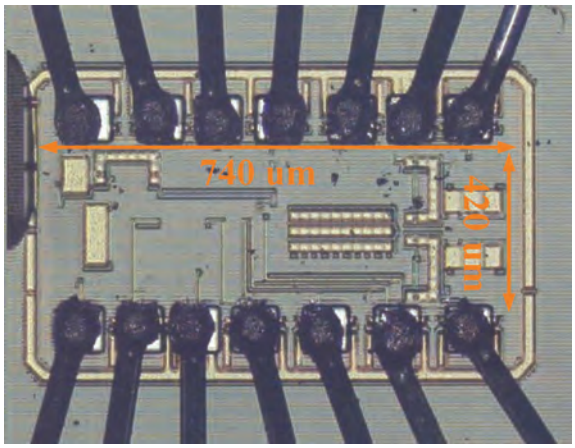

Fig. 8. Micrograph of the proposed chip.

the controlling pads. Static simulation results accord with the theoretical calculations.

4. Measurement results

The circuit is fabricated in a 0.18 μm 2P6M CMOS process. A micrograph of the chip is shown in Fig. 8. The die area is 0.74 × 0.42 mm^2, and the power consumption is 2.5 mW at a 3.3 V power supply.

In this design, the clock frequency is 2 MHz and the feedback resistance is 120 kΩ. The final differential-to-single stage has a gain of 0.5, and static measurement is carried out first to calculate the sensitivity. Figure 9 shows the ideal output voltage and the measured output voltage versus under-test capacitance. Measured sensitivity is 370 mV/pF and linearity error is below 1%. The theoretical sensitivity is 396 mV/pF. The sensitivity deviation is mainly caused by the accuracy of the on-chip resistors. This can be improved by on-chip resistance calibration.

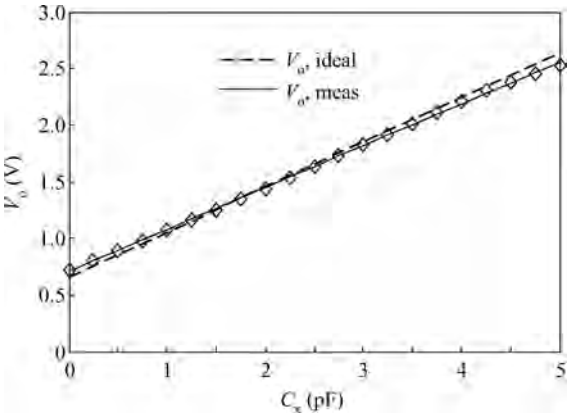

Fig. 9. Comparison of the ideal and measured output voltage.

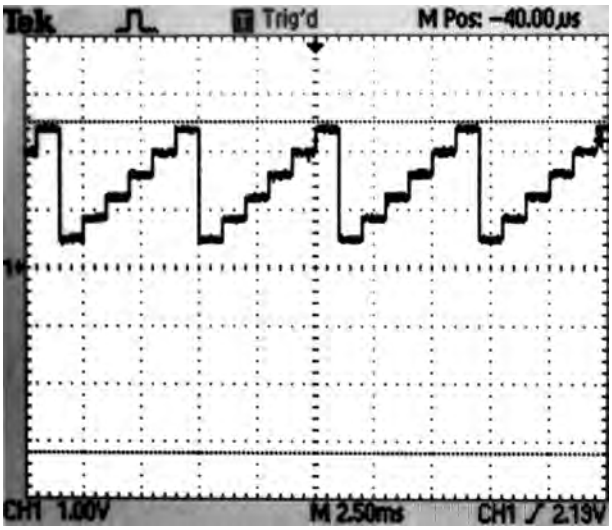

Fig. 10. Output voltage of the capacitive sensor changing from 0 to 5 pF by a 1 pF step with 1 kHz.

Dynamic measurement is also important for sensor application. A Xilinx FPGA is used to generate the controlling signals, changing the sensed capacitor from 0 to 5 pF by a 1 pF step every 1 ms. Figure 10 shows the oscilloscope output. The voltage difference between two close steps is nearly the same, about 370 mV. It is clear that the interface circuit can respond to capacitive sensor variation around several hundred Hz. The results obtained are summarized and compared with other papers in Table 1.

5. Conclusion

This paper presents a low power, high linearity symmetrical readout circuit for capacitive sensors. The readout circuit is based on a transimpedance amplifier with the chopper stabilization technique used to reduce the adverse effects of

Table 1. Performance summary and comparison.

Parameter	This work	Ref. [9]	Ref. [10]	Ref. [11]	Ref. [12]
Sensitivity (mV/pF)	370	7.88	Variable	0.155	N/A
Linearity (%)	1	N/A	1	N/A	N/A
Clock (kHz)	2000	250	Variable	4000	330
Supply (V)	3.3	5	1.8	3.3	5
Power (mW)	2.5	9.38	12	3.78	N/A
Technology (μm)	0.18	0.8	0.18	0.35	0.8

offset and $1/f$ noise. By introducing a reference branch, the symmetrical circuit improves its linearity, provides large output swing, reduces offsets and rejects common-mode noise and even-order distortions. Simulation results are given considering a sinusoidal changing sensor capacitor at a frequency of up to 1 kHz. An on-chip MIM capacitor array is designed for measurement. The proposed circuit consumes 2.5 mW with a power supply voltage of 3.3 V. The measured sensitivity is 370 mV/pF with a linearity error below 1%. Dynamic performance is also verified by FPGA at a switching frequency of 1 kHz.

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