A 12-bit, 40-Ms/s pipelined ADC with an improved operational amplifier*

Wang Yu(王瑜)[1,2], Yang Haigang(杨海钢)[1,†], Yin Tao(尹韬)[1], and Liu Fei(刘飞)[1]

[1]Institute of Electronics, Chinese Academy of Sciences, Beijing 100190, China
[2]Graduate University of the Chinese Academy of Sciences, Beijing 100049, China

Abstract: This paper proposes a 12-bit, 40-Ms/s pipelined analog-to-digital converter (ADC) with an improved high-gain and wide-bandwidth operational amplifier (opamp). Based on the architecture of the proposed ADC, the non-ideal factors of opamps are first analyzed, which have the significant impact on the ADC's resolution. Then, the compensation techniques of the ADC's opamp are presented to restrain the negative effect introduced by the gain-boosting technique and switched-capacitor common-mode-feedback structure. After analysis and optimization, the ADC implemented in a 0.35 μm standard CMOS process shows a maximum signal-to-noise distortion ratio of 60.5 dB and a spurious-free dynamic range of 74.5 dB, respectively, at a 40 MHz sample clock with over 2 Vpp input range.

Key words: pipelined ADC; operational amplifier; compensation technique
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1. Introduction

Modern communication systems are driving the rapid development of analog-to-digital converters (ADCs) to higher performances in a wide bandwidth signal channel. Most of the recently developed general-purpose CMOS ADCs for high speed applications have employed flash, folding, sub-ranging and pipelined architectures. Compared with other structure ADCs, pipelined ADCs are better candidates in wide band communication systems for their better tradeoffs in resolution and converting speed[1].

Intensively increasing the signal-to-noise distortion ratio (SNDR) is the major challenge for a high speed ADC. The negative effect which limits the SNDR is discussed in published work, such as capacitance mismatches[2], the comparator offset[3] and switch nonlinearity[4]. Besides these, this paper systematically presents the operational amplifier (opamp) non-ideal factors which devote the most nonlinearity and noise weight to an ADC's output, emphasizing gain error and finite gain bandwidth error. The error bounds are also given with theoretic analysis for the ADC design.

After modeling and analysis, this ADC exploits a gain-boosting topology opamp to achieve a high gain and wide bandwidth. However, the gain-boosting amplifier limits the frequency bandwidth and phase margin. To solve this problem, a frequency compensation method by adding a compensation capacitor at the output node of the auxiliary amplifier is proposed in this paper. It can suppress the Miller effect referring to the auxiliary amplifier, efficiently improve the unity-gain bandwidth and phase margin of the main amplifier, and make the integrated amplifier work as a single-pole system in the range of unity-gain bandwidth, which improves the stability of the settling behavior. In addition, a PMOS source follower is used to reduce the high frequency interference introduced by the switched-capacitor common-mode-feedback (SC-CMFB) structure. With the compensation techniques, the ADC performs with better resolution compared with the one using conventional opamp.

At the end of this paper, the prototype of 12-bit, 40-Ms/s pipelined ADC is implemented in a commercial 0.35 μm standard CMOS process, the measurement results show that the ADC performs a 60.5 dB SNDR and 74.5 dB spurious-free dynamic range (SFDR) at full sample clock frequency with 81 mA current under a 3.3 V supply.

2. ADC design

2.1. ADC architecture

Figure 1 describes the block diagram of the 12 bit pipelined ADC discussed in this paper. In a high resolution ADC with over 10-bit, the delay error accumulated by stages will exceed the ADC's least significant bit (LSB). So a sample and hold amplifier (SHA) is necessary to hold the high frequency input for the following stages. After that, there is a 2.5 bit stage composed by a 3 bit flash sub-ADC and multi-DAC. This is followed by eight 1.5 bit stages and finally a 2 bit flash ADC. In these stages, the opamp's bandwidth requirement is relaxed. All the circuits are designed in fully differential structure to minimize even-order harmonic distortion.

Figure 2 gives stage circuit diagrams and the timing diagram of the proposed ADC, in which all the circuits are described as a single-end structure for convenience. CLK_1 and CLK_2 are the non-overlap clocks operating in the pipelined ADC, as Figure 2(d) shows. In this work, the SHA front-end circuit is developed based on a simple flip-around structure, in which the input signal is sampled in CLK_1 first, and the opamp realizes the unity-gain feedback closed loop to hold the input in CLK_2 period. The opamp in the SHA circuit significantly impacts the ADC's resolution and converting speed the most in the whole circuit. As Figure 2(b) shows, the first stage con-

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† Corresponding author. Email: yanghg@mail.ie.ac.cn
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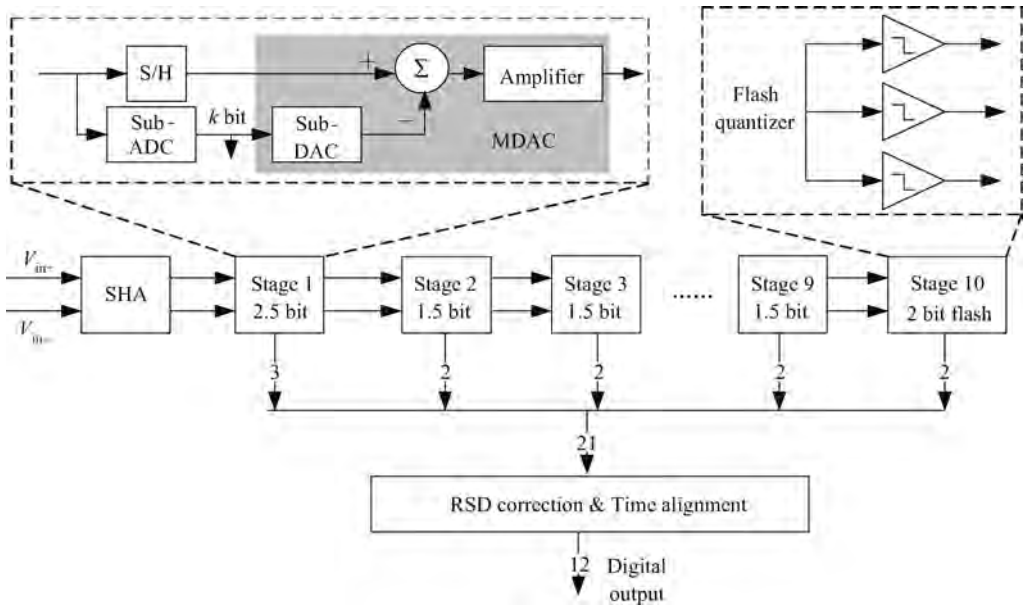

Fig. 1. ADC architecture.

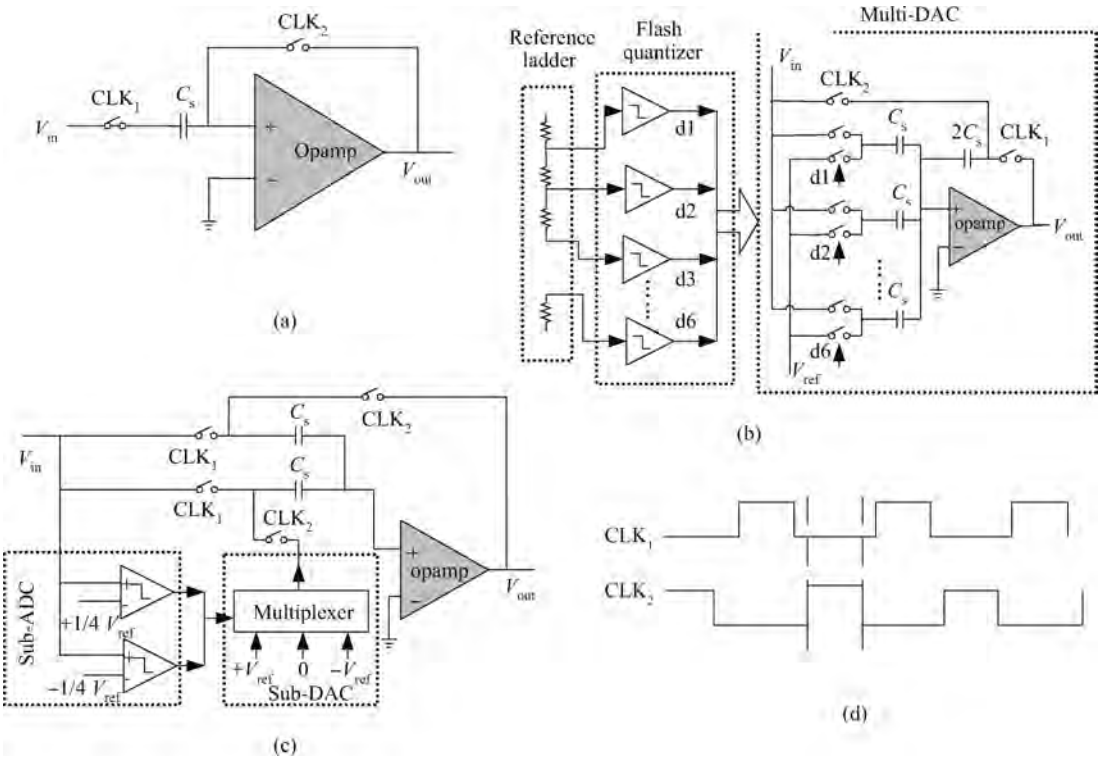

Fig. 2. (a) Sample and hold amplifier. (b) First 2.5 bit stage architecture. (c) 1.5 bit stage architecture. (d) Timing diagram of the non-overlap clock.

verts the input to a 2.5 bit digital output, in which the opamp is composed with the switch-capacitor configuration to amplify residue voltage four times for the next stage. When the SHA circuit holds the input in CLK_2, the first stage samples the input on C_s capacitors. While in the CLK_1 period, the first stage holds and outputs the residue voltage for the next stage in Fig. 2(c). As a conventional 1.5 bit stage, stage 2 to stage 9 also use the opamp to produce a specific multi-DAC output. The capacitors and opamps scale down stage by stage to reduce the power budget. It can be seen that the opamp of every stage plays the most important role in the proposed ADC.

2.2. Non-idealities of opamp in ADC design

In the introduced prototype ADC, in order to maximize the SNDR of the ADC, a high gain and wide bandwidth opamp is required. With the SIMULINK model of non-ideal opamp in the proposed ADC, the relation curves of non-idealities of the

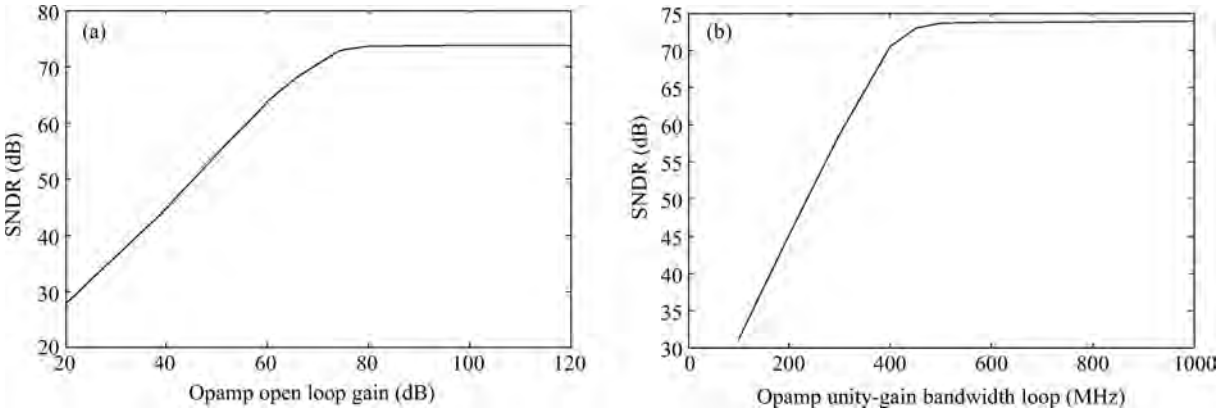

Fig. 3. (a) Opamp open loop gain versus the ADC's SNDR. (b) Opamp unity-gain bandwidth versus ADC's SNDR.

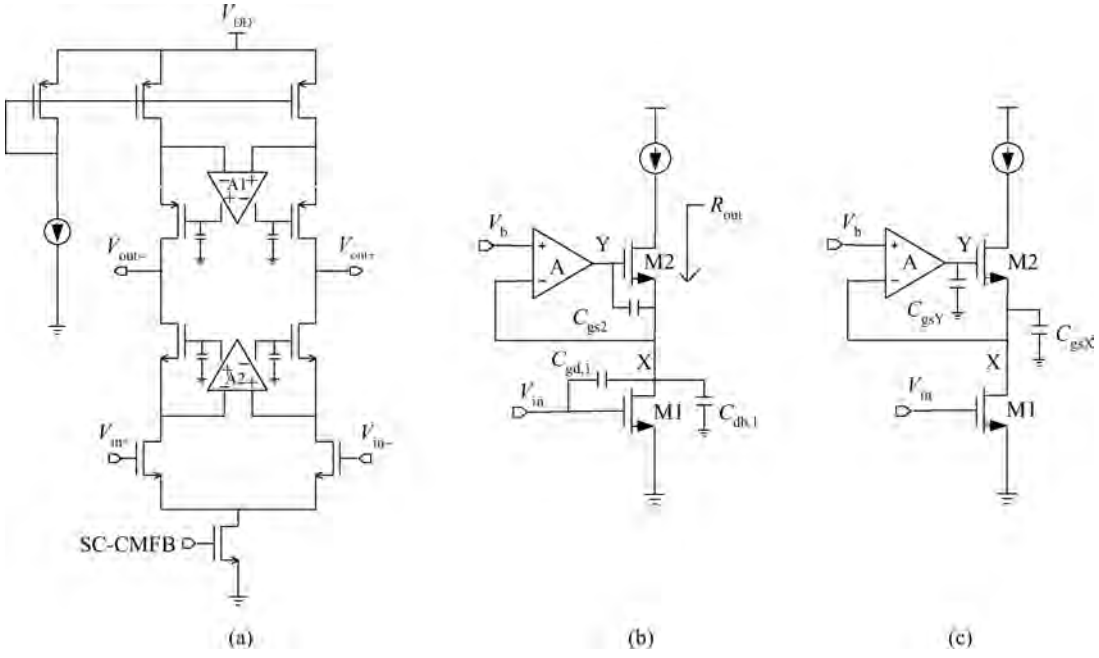

Fig. 4. (a) Gain-boosting amplifier architecture. (b) Gain boosting in cascade structure. (c) Miller effect of $C_{gs,2}$.

amplifier versus the ADC's resolution are depicted in Fig. 3.

The ADC's SNDR declines with the decreased opamp's open loop gain and unity-gain bandwidth under a critical value. In fact, these error bounds can be exactly calculated as follows:

$$A > \frac{1}{\beta} 2^{N+1}, \tag{1}$$

$$f_{\mathrm{u}} > \alpha \frac{f_{\mathrm{clk}} \ln 2^{N+1}}{2\pi\beta}, \tag{2}$$

where A is the open loop gain of the opamp; β is the feedback factor in the closed loop circuit (it is equal to 1 in the structure in Fig. 2(a)); N is the ADC resolution; f_{u} is the unity-gain bandwidth frequency; α is a ratio of the clock period in this closed loop system versus the settling time (usually picks 6); f_{clk} is the sampling clock frequency of the pipelined ADC. It can be seen that the opamp's gain error and finite gain bandwidth totally impedes the ADC to get a maximum SNDR. So the opamp's structure should be carefully designed in such ADCs, which is discussed in Section 3.

3. Compensation techniques of the opamp

3.1. Opamp structure

Based on the analysis in Section 2, it is concluded that the ADC should use a high gain and wide bandwidth opamp for its high resolution of 12 bit at tens of mega Hertz sample clock. To achieve that, an opamp based on the gain-boosted telescope cascode architecture is the best choice. Compared with it, the 2-stage and folded cascade structures both have their disadvantages. The former requires Miller compensation for stability and also consumes more than twice the power dissipation of a single stage[5]. The latter exhibits a lower achievable bandwidth, though it has a larger range of input voltage[6]. The amplifier shown in Fig. 4(a) adopts the gain-boosted technique to achieve the high gain without output swing reduction. However, the gain-boosting technique would restrain the gain-bandwidth of the opamp and further effect the opamp's frequency response. More theoretic analysis of the gain-boosted amplifier is presented in the following.

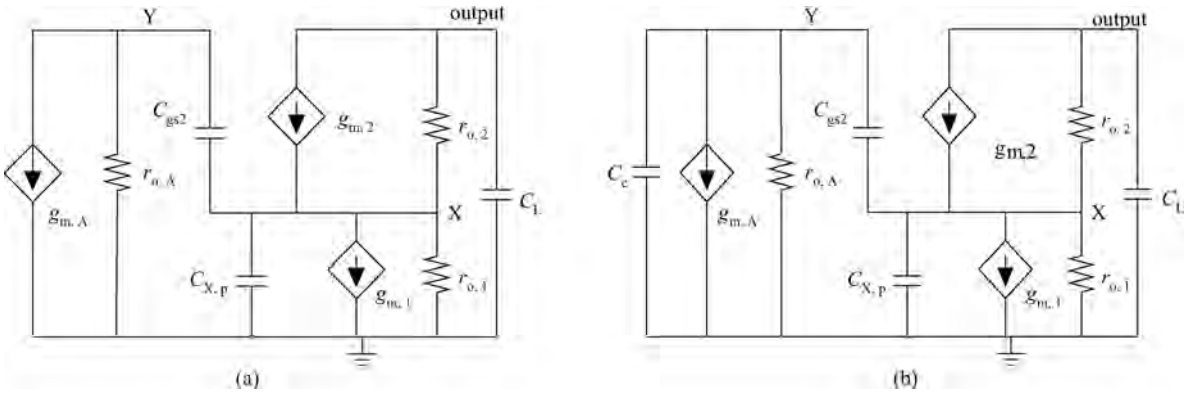

Fig. 5. (a) Small signal model of gain boosting in cascade structure. (b) Compensation capcitor in the small signal model.

3.2. Opamp analysis and compensation

A single-end gain-boosted telescope circuit model is shown in Fig. 4(b) for convenience. As the gain-boosting amplifier gives a negative feed-back at the gate voltage of M2, the output resistance is calculated as Eq. (3)[7]:

$$R_{\text{out}} \approx A_0 g_{\text{m},2} r_{\text{o},1} r_{\text{o},2}, \tag{3}$$

where A_0 is the open loop gain of the gain boosting amplifier; $g_{\text{m},2}$ is the transconductance of M2; $r_{\text{o},1}, r_{\text{o},2}$ is the output equivalent resistances of M1 and M2. Then, the output voltage gain is

$$A_{\text{v}} = g_{\text{m},1} R_{\text{out}} \approx A_0 g_{\text{m},1} r_{\text{o},1} r_{\text{o},2} g_{\text{m},2}. \tag{4}$$

The main pole of the circuit is at the output node, which dominates the –3 dB bandwidth of such gain-boosted opamp. The frequency of –3 dB bandwidth is

$$\omega_{3\text{db}} = \frac{1}{C_{\text{Load}} R_{\text{out}}} = \frac{1}{C_{\text{load}} A_0 g_{\text{m},2} r_{\text{o},1} r_{\text{o},2}}. \tag{5}$$

A small signal model of the gain-boosted structure is presented in Fig. 5(a). Here, the gain-boosting amplifier is simplified as a model of transconductance $g_{\text{m,A}}$ and output resistance $r_{\text{o,A}}$. $C_{\text{X,p}}$ presents the parasitic capacitance at node X, including $C_{\text{db},1}$ and the miller capacitance of $C_{\text{gd},1}$ ($C_{\text{gd},1}$ is multiplied by approximately 2 in such simple common-source transistor M1[8]). C_{L} is the output load capacitance. The current through C_{L} is

$$I_{C_{\text{L}}} = V_{\text{out}} C_{\text{L}} s = -\left[g_{\text{m},2} (V_{\text{Y}} - V_{\text{X}}) + (V_{\text{out}} - V_{\text{X}}) \frac{1}{r_{\text{o},2}} \right]. \tag{6}$$

and

$$-I_{C_{\text{L}}} + (V_{\text{Y}} - V_{\text{X}}) C_{\text{gs},2} s = g_{\text{m},1} V_{\text{in}} + \frac{V_{\text{X}}}{r_{\text{o},1}} + V_{\text{X}} C_{\text{X,p}} s, \tag{7}$$

where V_{in} is the input signal in Fig. 4(b), and the current through $C_{\text{gs},2}$ is

$$-(V_{\text{Y}} - V_{\text{X}}) C_{\text{gs},2} s = V_{\text{X}} g_{\text{m,A}} + \frac{V_{\text{Y}}}{r_{\text{o,A}}}. \tag{8}$$

Then,

$$\frac{V_{\text{out}}}{V_{\text{in}}} \approx -\frac{g_{\text{m,A}} r_{\text{o,A}} g_{\text{m},2} g_{\text{m},1} + s C_{\text{gs},2} \dfrac{r_{\text{o,A}}}{r_{\text{o},2}}}{g_{\text{m,A}} r_{\text{o,A}} C_{\text{gs},2} C_{\text{L}} s \left(s + \dfrac{g_{\text{m,A}} r_{\text{o,A}} g_{\text{m},2}}{g_{\text{m,A}} r_{\text{o,A}} C_{\text{gs},2} + C_{\text{X,p}}} \right) + \dfrac{1}{r_{\text{o},1} r_{\text{o},2}}}. \tag{9}$$

It is deduced that the gain-boosting technique with $C_{\text{gs},2}$ introduces a zero and reduces the second pole of the amplifier drastically. This could be explained as the Miller effect of $C_{\text{gs},2}$ at node X, which is the second pole in such telescope stage. As Figure 4(c) shows, $C_{\text{gs},2}$'s Miller capacitance $C_{\text{gs,X}}$ is:

$$\begin{aligned} C_{\text{gsX}} &= \frac{1}{Z_{\text{gs,X}} s} = \left[\frac{Z_{\text{gs},2}}{1 - A_{\text{YX}}} s \right]^{-1} = C_{\text{gs},2} \left(1 - \frac{V_{\text{Y}}}{V_{\text{X}}} \right) \\ &= C_{\text{gs},2} \left(1 + \frac{g_{\text{m,A}}}{g_{\text{o,A}}} \right), \end{aligned} \tag{10}$$

where $Z_{\text{gs},2}$ is the impedance from the gate to the source of M2; A_{YX} is the gain of node Y to node X; $g_{\text{o,A}}$ is the output conductance of the auxiliary amplifier.

3.3. Experiment of opamp

Obviously, the parasitic capacitance at node X increases a great deal because of the gain-boosting amplifier, which pushes the frequency of the pole at node X much closer to origin; so, the unity-gain bandwidth is limited by the auxiliary amplifier. To restrain the Miller effect of $C_{\text{gs,X}}$ this paper presents a method of adding the compensate capacitance at the output of the auxiliary amplifier (node Y) shown in Fig. 5(b). The current through $C_{\text{gs},2}$ is distributed separately to C_{c}. The new transfer function could be educed as

$$\begin{aligned} \frac{V_{\text{out}}}{V_{\text{in}}} \approx & -g_{\text{m,A}} r_{\text{o,A}} g_{\text{m},1} g_{\text{m},2} \left(1 + \frac{C_{\text{c}}}{g_{\text{m,A}}} s \right) \\ & \times \left[C_{\text{c}} C_{\text{gs},2} C_{\text{L}} r_{0,\text{A}} s^3 + C_{\text{L}} r_{0,\text{A}} (g_{\text{m},2} C_{\text{c}} + g_{\text{m,A}} C_{\text{gs}}) s^2 \right. \\ & \left. + g_{\text{m,A}} r_{\text{o,A}} g_{\text{m},2} C_{\text{L}} s + \frac{1}{r_{\text{o},2} r_{\text{o},1}} \right]^{-1} \end{aligned}$$

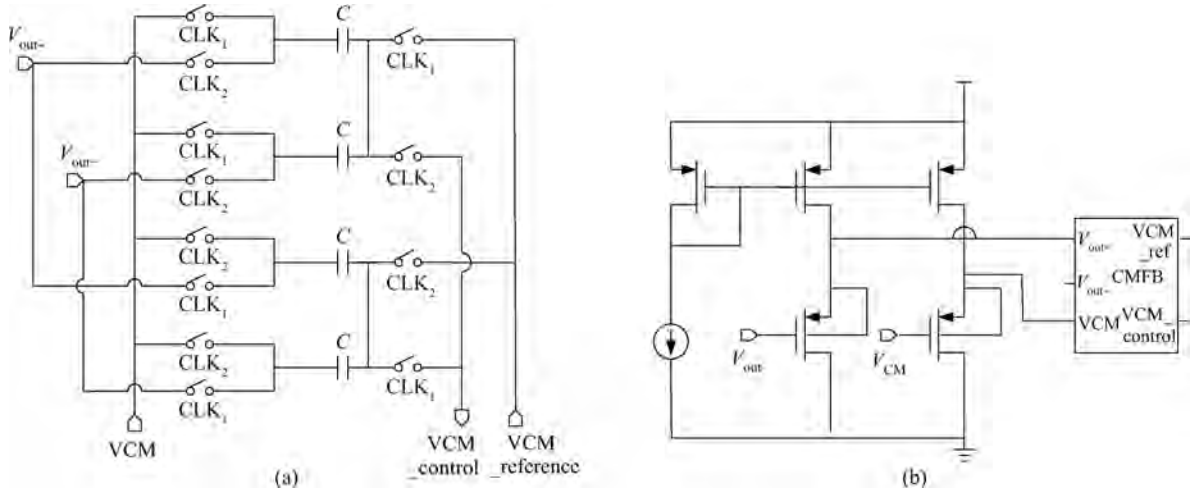

Fig. 6. (a) Circuit diagram of CMFB unit. (b) Buffer for the CMFB unit.

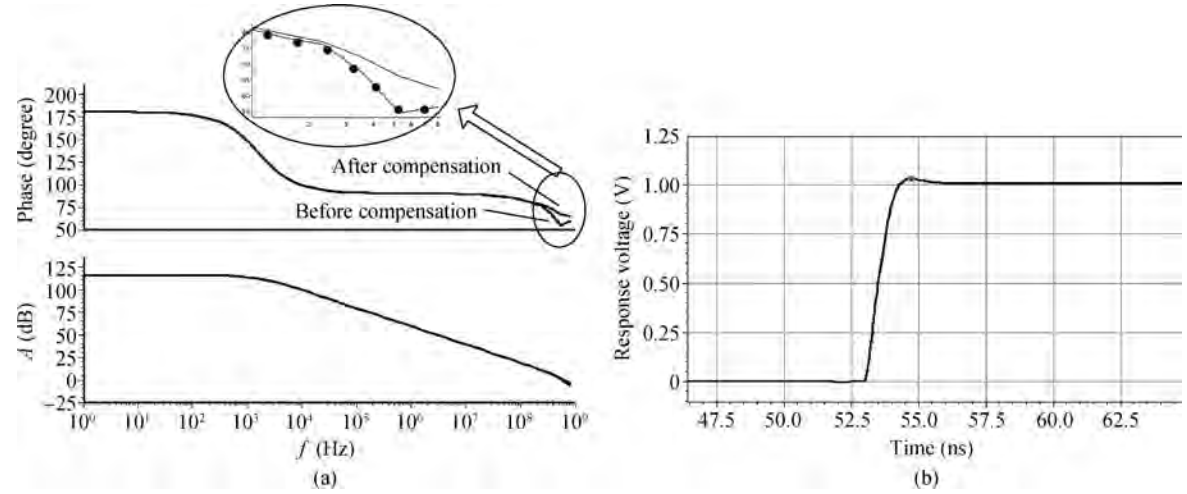

Fig. 7. (a) Comparison of the frequency response between the improved opamp and a conventional one. (b) Tested response wave of the opamp in a unity-closed loop.

$$= -\frac{g_{m,1}\left(1+\frac{C_c}{g_{m,A}}s\right)}{C_L s\left(\frac{C_c}{g_{m,A}}s+1\right)\left(\frac{C_{gs}}{g_{m,2}}s+1\right)+\frac{1}{g_{m,A}r_{o,A}g_{m,2}r_{o,2}r_{o,1}}}. \quad (11)$$

Focusing on the pole referenced to $C_{gs,2}$, it has pushed away from origin in Eq. (11). This is because at high frequencies (as we approach the pole at node X), the compensate capacitor C_c parallel connects with C_{gsY}, dropping the gain of the auxiliary amplifier and suppressing the Miller effect of $C_{gs,2}$. Then, in the unity-gain bandwidth range, only one pole is dominated, which makes the amplifier stable, like a single-pole system. After discussing the compensation with the purpose of broadening the wide bandwidth, we now turn our attention to the CMFB and its negative effect on the opamp output.

As Figure 6(a) shows, SC-CMFB can rapidly hold the opamp's common-mode voltage under the high frequency condition compared with continuous time CMFB. Here, CLK_1 and CLK_2 are a pair of complementary clocks for the SC-CMFB unit to refresh the charge on the capacitor, which is used to detect the output voltage. In fact, the switch-capacitance structure can be seen as an equal resistor in the whole operating time. The equal resistance is[8]

$$R_{equal} = \frac{1}{f_{clk}c}, \quad (12)$$

where f_{clk} is the frequency of CLK_1 and CLK_2, and C is the capacitance of the refreshing capacitors. In this work, in order to get the stable voltage in a quick period, f_{clk} is up to 20 MHz. With this high frequency clock, the SC-CMFB switch introduces high frequency interference to the output, which generates glitches of the opamp's transient output. To restrain such effect in a high speed opamp, the proposed amplifier uses a technique of inserting an insolating buffer between the output node and the SC-CMFB unit, as shown in Fig. 6(b). In fact, a PMOS source follower is used as a unity-gain buffer in this schematic, where the symbol CMFB represents the structure in Fig. 6(a). In order not to compress the output range of the main amplifier, the PMOS transistors work in a different voltage to avoid the body effects described in Fig. 6(b). So, a gain-boosted

Table 1. Opamp comparison.

Item	After compensation	Before compensation	Ref. [9]	Ref. [10]	Ref. [11]
A_v (dB)	114	114	63.95	85	56
GBW (MHz)	721	635	283	481	450
PM (°)	63	54	61.9	68	77
Load capacitance (pF)	6	6	1.5	3	1
Slew rate (V/μs)	850	741	—	—	—
Settling time (ns)	3.2	5.05	3.96	6	6
Power (mW)	27	27	19.94	5.8	1.6
Voltage supply (V)	3.3	3.3	3.3	1.8	1
FoM_1*	18.27	16.09	1.36	21.1	15.75
FoM_2*	50.06	27.94	5.386	41.47	46.88

$$* \text{FoM}_1 = \frac{A_v(\text{dB}) \cdot \text{GBW(MHz)} \cdot C_{\text{Load}}(\text{pF})}{\text{Power}(\mu\text{W})}; \quad \text{FoM}_2 = \frac{\text{GBW(MHz)} \cdot C_{\text{Load}}(\text{pF})}{\text{Settlingtime(ns)} \cdot \text{Power(mW)}}$$

Table 2. ADC performance comparisons.

Parameter	This work	Ref. [12]	Ref. [13]	Ref. [14]
Process (μm)	0.35	0.18	0.13	—
Resolution (bit)	12	11	12	12
Conversion rate (Ms/s)	40	45	40	50
Voltage supply (V)	3.3	1.8	1.2	3.3
Input range (Vpp)	2	1.3	1	2
SNR (dB)	60.5	60.1	60.5	65.5
SFDR (dB)	74.5	70	78.2	74
DNL (LSB)	–1.37/+1.35	–0.4/+0.45	±0.45	±0.75
INL (LSB)	–6.8/+7.2	–1/+1.1	–6/+4	±0.75
Current (mA)	81	45 (only analog core)	13	103

opamp using these two compensation techniques is designed to meet the requirement of the wide bandwidth and high gain in the ADC circuit.

Figure 7(a) compares the frequency response of the improved amplifier (the bold line) with the conventional one (the dotted line). It clearly represents that the unity-gain bandwidth and phase margin are improved due to the proposed compensation techniques. The amplifier has almost the same characters of a single-pole system. Figure 7(b) validates the measurement results of the improved opamp's unity-gain closed loop performance. When a 1 V step signal is implied on the opamp's different input, a 1 V voltage response is settled after 3.2 ns.

Table 1 gives a brief comparison between the improved opamp, the structure which is not compensated and another work. It shows that the proposed amplifier could achieve a broader bandwidth and phase margin than the conventional one. In addition, the improved opamp is proved to reach the quickest settling behavior and a better property in ADCs compared with other research. ADCs using the improved opamp and conventional opamp have been simulated to verify the improvement of compensation techniques, as Figure 8 shows. The conventional ADC's SNDR degrades over 10 dB especially in the high frequency sampling clock, which further proves the advantages of the proposed ADC with the improved opamp.

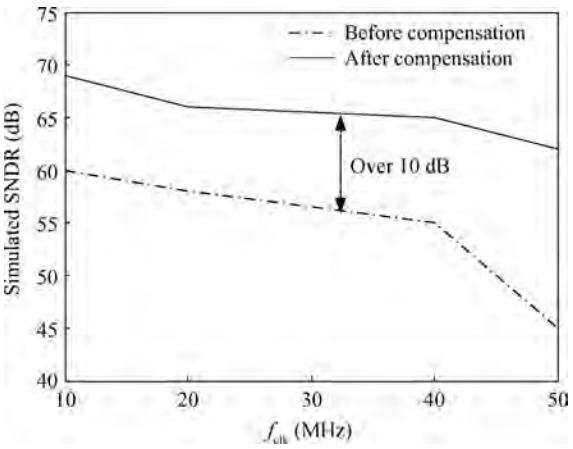

Fig. 8. Simulated SNDR Comparison between the improved ADC and the conventional ADC.

4. Other component circuitry

Figure 9 shows the dynamic comparator used in the ADC stages. When the stage operates in the sample phase, the latch signal falls low to cut off the bias current, and in the amplify phase the latch signal rises high to turn on the tail current sources M5 and M6. While the differential pairs M1–M4 judge the input signal and the reference voltage to produce the decision signal Q. The circuit achieves a high frequency response of the proposed ADC with little power dissipation.

Switch nonlinearity is also a problem in the pipelined ADC. In every stage, the input switch is bootstrapped by the circuit, as Figure 10 shows. Here C_B is the bootstrapped capacitor, which lifts the gate voltage of the switch transistor M9 with V_{in} change. So, the linearity of switch on-resistance has been improved with a stable switch overdrive voltage.

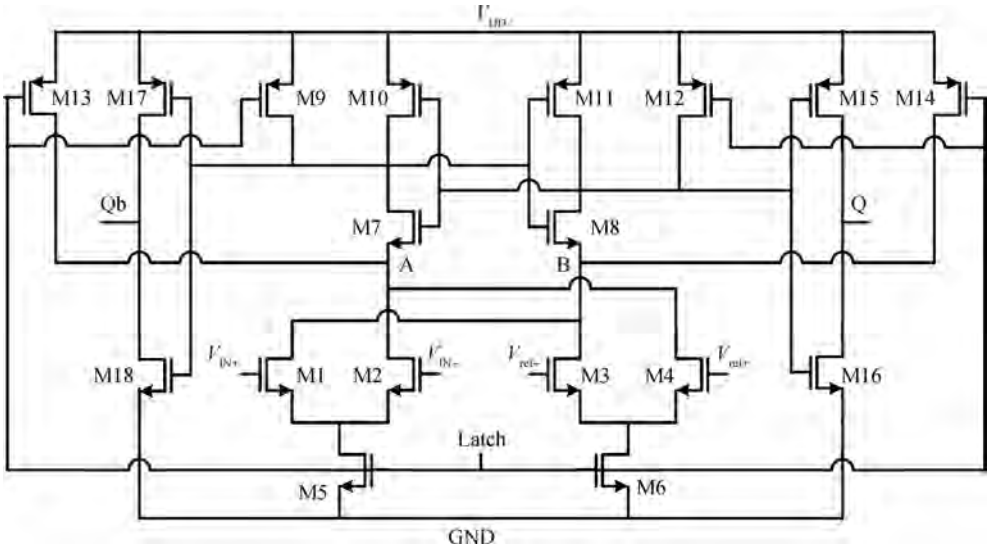

Fig. 9. Dynamic comparator structure.

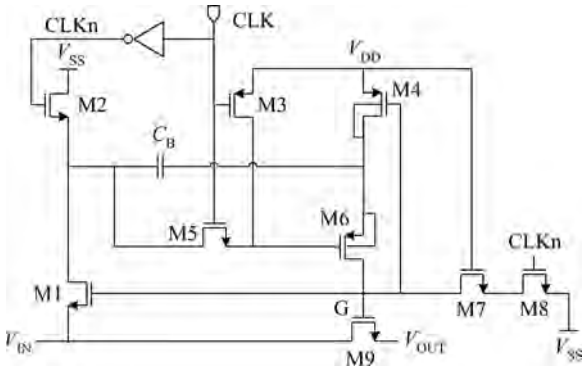

Fig. 10. Bootstrapped switch circuit.

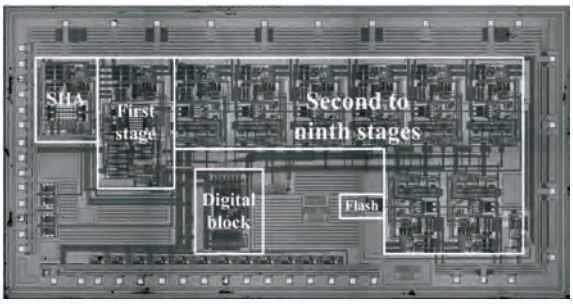

Fig. 11. Die micrograph of the fabricated circuit.

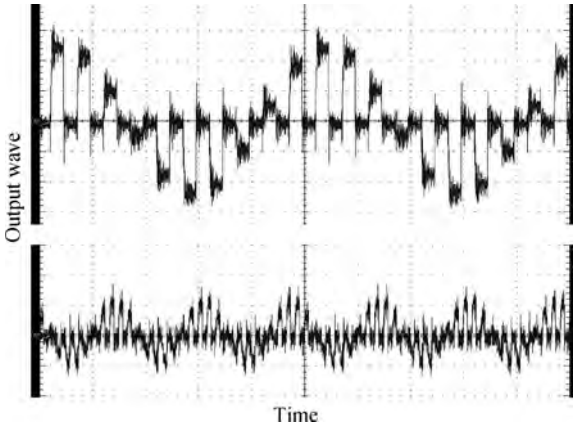

Fig. 12. Sample output wave of SHA under 10 MHz and 40 MHz sampling clock.

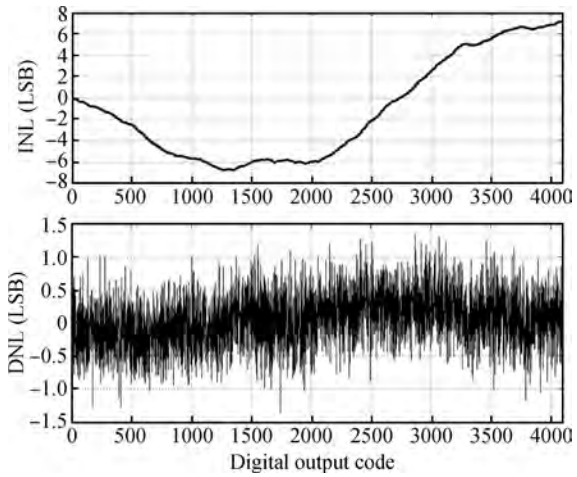

Fig. 13. INL & DNL of the ADC @ 40 Ms/s.

5. Prototype measurement

Based on efficient estimation of the non-idealities, a 12-bit 40-Ms/s pipelined ADC with the improved opamp is implemented in a standard 0.35 μm CMOS process, which has been optimized at schematic and layout levels. Figure 11 shows the die micrograph of the fabricated circuit. All critical individual blocks appear in the chip. The core of the ADC occupies an area of less than 5.2 mm^2.

Figure 12 validates the measurement wave of the sample and hold circuit outputs in 10 MHz and 40 MHz sample clock frequencies. The output shows great integrity, which means that the input wave is specifically sampled under a different operating frequency in the pipelined ADC with the im-

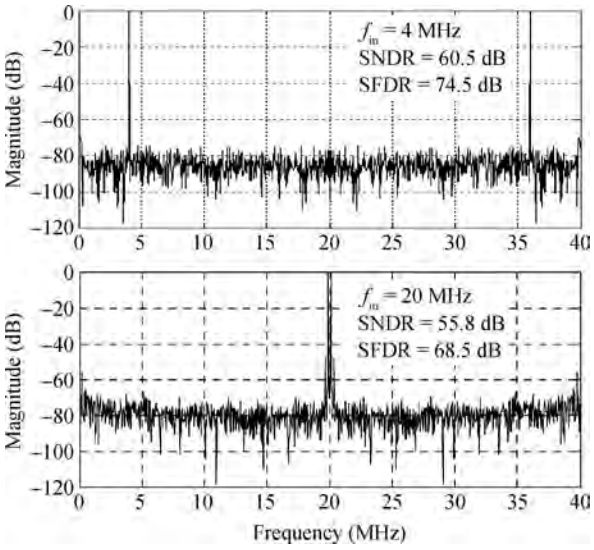

Fig. 14. Frequency spectrum of the circuit output with 4 MHz & 20 MHz input @ 40 Msps.

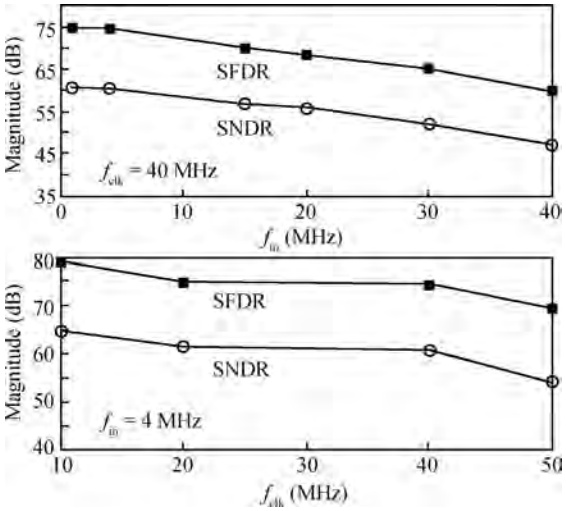

Fig. 15. SNDR & SFDR versus input frequency & sample frequency.

proved opamp. The ADC's tested INL and DNL are depicted in Fig. 13, which are within –1.37 to +1.35 and –6.8 to +7.2, respectively. The nonlinearity is a little larger, which owes to capacitors mismatch of ADC stages. Figure 14 gives the tested frequency spectrum of the 12 bit ADC at 40 MHz sampling rate with a 4 MHz and 20 MHz input frequency. It is tested that the SNDR is 60.5 dB and SFDR is 74.5 dB with 4 MHz input frequency at 40 Ms/s. The performance parameters of the chip are summarized in Table 2. The SNDR and SFDR versus the input frequency at 40 MHz sample clock is shown in Fig. 15, which also gives the SNDR and SFDR versus the sampling clock frequency with a 4 MHz input. It is shown that the ADC could maintain a good performance under a different sample clock and with a different input frequency.

Table 2 also gives results from other works and a commercial chip compared with this work. It is shown that the proposed ADC has good performances with a larger input range. More work should be taken to reduce the power consumption and to implement some digital calibration in the future.

6. Conclusion

A 12-bit, 40-Ms/s pipelined ADC with an improved high gain and wide bandwidth operational amplifier is proposed. The non-ideal factors of the ADC have been analyzed in terms of the opamp's gain error and finite gain bandwidth. An optimized system has been implemented as well. To achieve a high performance ADC, a high gain and wide bandwidth amplifier has been exploited, which used a method of adding compensate capacitors at the output of the gain-boosting amplifiers to restrain the degradation of bandwidth and the phase margin derived from the gain-boosted technique. In addition, the problem that the SC-CMFB technique impacts the opamp's output properties has also been solved by isolating the output node and CMFB unit with a buffer as the PMOS source follower. Finally, the ADC was implemented in a standard 0.35 μm CMOS process and tested with a 60.5 dB SNDR and 74.5 dB SFDR operating at a 40 MHz sample clock with over 2 Vpp input range.

References

[1] Le B, Rondeau T W, Reed J H, et al. Analog-to-digital converters—a review of the past, present and future. IEEE Signal Processing Magazine, November 2005: 69

[2] Ray S, Song B S. A 13-b linear, 40-MS/s pipelined ADC with self-configured capacitor matching. IEEE J Solid-State Circuits, 2007, 42(3): 463

[3] Quinn P J, van Roermund A H M. Accuracy limitations of pipelined ADCs. IEEE International Symposium on Circuits and Systems, 2005, 3: 1956

[4] Aksin D, Al-Shyoukh M, Maloberti F. Switch bootstrapping for precise sampling beyond supply voltage. IEEE J Solid-State Circuits, 2006, 41(8): 1938

[5] Pugliese A, Amoroso F A, Cappuccino G, et al. Settling time optimization for three-stage CMOS amplifier topologies. IEEE Trans Circuits Syst 2009, 56(12): 2569

[6] Li Y L, Han K F, Tan X, et al. Transconductance enhancement method for operational transconductance amplifiers. Electron Lett, 2010, 46(19): 1321

[7] Bult K, Green G J G M. A fast-settling CMOS op amp for SC circuits with 90-dB DC gain. IEEE J Solid-State Circuits, 1990, 25(6): 1379

[8] Razavi B. Design of analog CMOS integrated circuits. McGraw-Hill Higher Education, 2001

[9] Ning Ning, Yu Qi, Wang Xiangzhan. A novel clock feed-through frequency compensation for fast-setting of folded-cascode OTA. Chinese Journal of Semiconductors, 2006, 27(10): 1737

[10] Fan Mingjun, Ren Junyan, Guo Yao, et al. A novel low-voltage operational amplifier for low-power pipelined ADCs. Journal of Semiconductors, 2009, 30(1): 015009

[11] Taherzadeh-Sani M, Hamou A A. A 1-V process-insensitive current-scalable two-stage opamp with enhanced DC gain and settling behavior in 65-nm digital CMOS. IEEE J Solid-State Circuits, 2011, 46(3): 660

[12] Ahmed I, Johns D A. An 11-bit 45 MS/s pipelined ADC with rapid calibration of DAC errors in a multibit pipeline stage. IEEE J Solid-State Circuits, 2008, 43(7): 1626

[13] Fan M J, Ren J Y, Shu G H. A 12-bit 40-MS/s SHA-less pipelined ADC using a front-end RC matching technique. Journal of Semiconductors, 2011, 32(1): 015002

[14] www.analog.com/static/imported_files/data_sheets/AD9863.pdf