Study of radiation-induced leakage current between adjacent devices in a CMOS integrated circuit

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Abstract: Radiation-induced inter-device leakage is studied using an analytical model and TCAD simulation. There were some different opinions in understanding the process of defect build-up in trench oxide and parasitic leakage path turning on from earlier studies. To reanalyze this problem and make it beyond argument, every possible variable is considered using theoretical analysis, not just the change of electric field or oxide thickness independently. Among all possible inter-device leakage paths, parasitic structures with N-well as both drain and source are comparatively more sensitive to the total dose effect when a voltage discrepancy exists between the drain and source region. Since N-well regions are commonly connected to the same power supply, these kinds of structures will not be a problem in a real CMOS integrated circuit. Generally speaking, conduction paths of inter-device leakage existing in a real integrated circuit and under real electrical circumstances are not very sensitive to the total ionizing dose effect.

Key words: Total ionizing dose effect; inter-device leakage current; CMOS IC
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1. Introduction

Since semiconductors have scaled to the deep sub-micron level and thin gate oxides have brought inherent radiation tolerance, the threat of significant threshold voltage shifts resulting from total dose irradiation have been reduced. Meanwhile, radiation-induced leakage current, which is caused by a positive charge trapped in the isolation layers, becomes one of the most significant problems of hardness assurance for modern CMOS technologies[1−4]. Generally speaking, radiation-induced leakage simulation demands a multi-scale approach based on the level of physical and circuit modeling. The circuit modeling approach is required for more cost-effective simulations[5, 6].

However, a total ionizing dose (TID) effect will work on the whole circuit or chip. There is one assumption that basic devices would still work independently after irradiation, which we need to verify before intending to execute circuit simulation. This assumption suggests that the accumulated dose would only change the parameters of single devices, like MOSFETs, and will not turn on any parasitic structure. Unfortunately, researchers from Arizona State University have predicted that radiation-induced inter-device leakage may increase notably when entering the deep sub-micron level[3]. To study this problem quantitatively, two research groups both designed field oxide field effect transistors (FOXFETs) which use shallow trench isolation (STI) as a gate dielectric. Their test results after irradiation show that inter-device leakage may even exceed 1 nA and would not be neglected[7−9].

However, the structure of the FOXFETs in one study are different from parasitic structures in common CMOS integrated circuits, but more similar to those used in high-energy physics, like that from silicon strip detector[7, 8]. The other study does design FOXFETs similar to real parasitic structures, but they come to the conclusion that fairly uniform trends in defect build-up occur near all the STI interface[9]. Contrary to this opinion, some researchers believe that forming an inversion layer at the STI bottom is harder than forming an inversion layer at the STI sidewall due to the low electric field[10]. And other researchers think that the parasitic conduction is expected to take place first at the bottom of the STI then extend towards the upper portion of the STI sidewalls resulting from the effect of oxide thickness[11, 12].

To reanalyze this problem and make it beyond argument, radiation-induced leakage current between adjacent devices in a CMOS IC is studied in this paper. First, the process of a parasitic conduction path turning on is analyzed. Then it could be concluded which part of the STI interface would turn on first along with increasing the accumulated dose. Second, using the theoretical analysis above, a qualitative prediction can be made about the comparison between intra-device leakage (leakage current from drain to source in a single MOSFET) and inter-device leakage due to different parasitic structures. In the end, simulation results will be presented to validate the prediction above, and then a conclusion will be made about the seriousness of radiation-induced inter-device leakage to a real integrated circuit. What's more, the experimental results of an intra-device leakage of single MOSFETs are presented to validate the calculation model in this paper.

2. Theoretical analysis and ISE TCAD validation

2.1. Device structure and simulation setup

The device models studied in this work belong to 250 nm CMOS technology. Table 1 presents the values of several basic

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Table 1. Values of basic structure parameters for the 250 nm CMOS technology.

Parameter	Value
Inclination angle of STI sidewall	85°
Gate oxide thickness	5.5 nm
STI oxide thickness	400 nm
V_{dd}	2.5 V
Thickness of oxide between Metal I and diffusion	1 μm

Table 2. Values of physical parameters for simulation of TID irradiation.

Parameter	Value
Type of traps	hNeutral
Trap concentration	1×10^{18} cm^{-3}
Hole capture cross section	1×10^{-12} cm^2
Electron capture cross section	4×10^{-13} cm^2

structure parameters. For core transistors, the gate oxide thickness is only 5.5 nm, but the thickness of the STI isolation oxide is much bigger.

To introduce the effect of irradiation, values of the physical parameters for the simulation are presented in Table 2. Process simulation and an inverse modeling approach are used to calibrate the doping profiles within the 3-D device model. Then the experimental results of single MOSFETs after irradiation are presented to validate the parameter values in Table 2.

2.2. Theoretical analysis

Modern trench structures (STI) use very steep sidewalls (85°). To simplify analysis, a planer structure with a sharp trench edge is used, although real STI structures may differ from this idealized geometry in the top region, like recessed or overfilled ones. Due to a tunneling effect in thin oxides, charge trapping is highly reduced for oxides thinner than 8 nm[13]. Then the error from this simplified model can be neglected. In nearly all cases the gate oxide extends over the top surface of the trench and produces a high electric field that extends into the isolation region. The electric field plays a key part in both the initial separation of electron–hole pairs and charge migration. In fact, total dose effects working on CMOS trench isolation can be divided into four processes. First, electron–hole pairs are generated in the oxide, but only a portion of them do not immediately recombine, the probability of escaping initial recombination is the yield function $Y(E)$. And $Y(E)$ can be expressed as follows[14]:

$$Y(E) = \left(\frac{|E| + E_0}{|E| + E_1}\right)^m, \quad m = 0.9, \\ E_0 = 0.1 \text{ V/cm}, \quad E_1 = 1.35 \text{ MV/cm}. \quad (1)$$

Figure 1 presents the distribution of the electric field value along the STI sidewall when the gate voltage equals 2.5 V. Then the yield function value can be calculated and it decreases exponentially with the depth below the gate oxide. Second, carriers escaping initial recombination will be transported to the Si/SiO_2 interface mainly by drift. The simulation result of potential distribution is shown in Fig. 2. And the potential gradient is approximately a series of semicircles[4, 5]. The distance between the equipotential lines decreases with radius, and the electric field increases correspondingly.

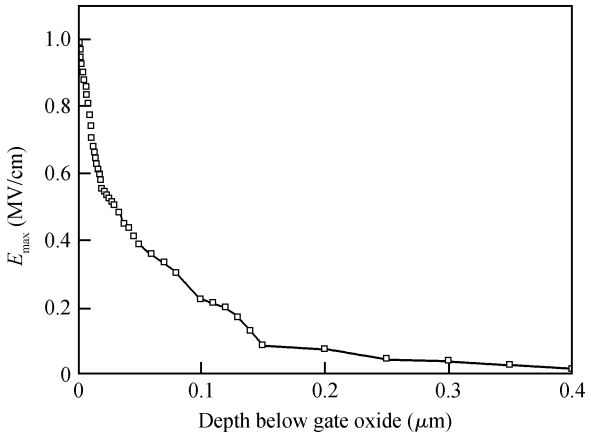

Fig. 1. Electric field distribution along the STI sidewall when the gate voltage equals 2.5 V by TCAD simulation.

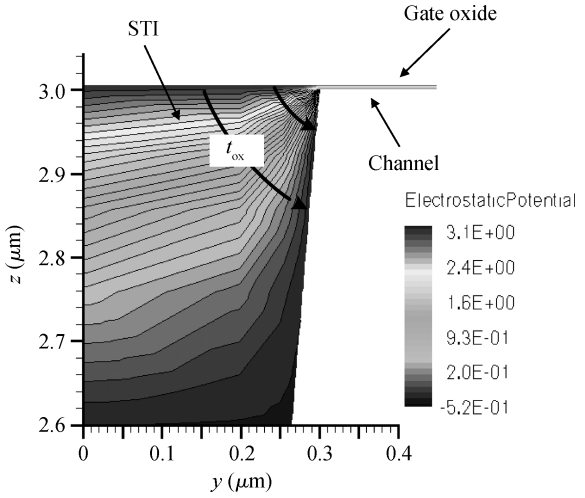

Fig. 2. Distribution of electric potential along the STI sidewall when the gate voltage equals 2.5 V by TCAD simulation.

From Fig. 2, the length of the field lines in the STI region is increasing with depth below gate oxide. That means the path length value t_{ox} between the gate contact to the substrate is becoming bigger. Although the gate voltage equals 2.5 V and the substrate equals 0 V, the voltage discrepancy in the top and bottom region of the trench oxide doesn't equal 2.5 V, but the summation of 2.5 V and $\phi_{s's}$, the work function discrepancy between the N^+ poly gate and the P-substrate. And Figure 2 presents a voltage discrepancy about 3.6 V, which means that expressions from some papers aren't completely accurate[4, 15].

To study the region effect of total dose effects working on an STI structure, the trench region is split into numerous elementary parasitic transistors. If we set the depth below gate oxide as variable x, then $t_{ox}(x)$ can be interpreted as depth of the gate oxide of elementary parasitic transistors.

The yield function $Y(E)$ is a minimum when $t_{ox}(x)$ reaches its maximum which is according to the STI base, because of the minimum electric field values. $Y(E)$ and $t_{ox}(x)$ exhibit opposite trends. That is why the product of $Y(E)$ and

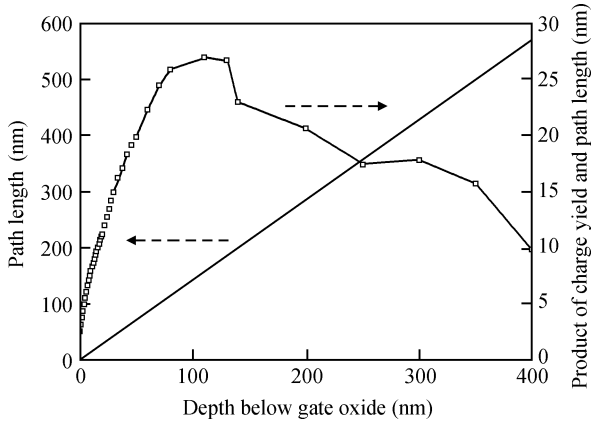

Fig. 3. Distribution of t_{ox} and the product of charge yield and tox along the STI sidewall.

$t_{ox}(x)$ reaches its maximum in about 100 nm below the gate oxide. Third, carriers will be trapped at the interface between the trench oxide and the adjacent silicon and then trapped charges emerge. It has been found that the hole traps are located within a few nanometers of the interface. And electron trapping can be neglected considering that the electron and hole mobility in the oxide are equal to 20 and 10^{-5} cm^2/(V· s), respectively. The continuity equation for the hole traps is:

$$\frac{\partial p_T}{\partial t} = \sigma_p j_p (N_T - p_T), \tag{2}$$

where p_T is the concentration of trapped holes, j_p is the hole flux, σ_p is the cross section of hole captured by neutral hole traps, and N_T is the concentration of neutral hole traps in the trench oxide. We set the variable u to represent the distance from the top of the gate oxide following the electric field lines ($0 \leqslant u \leqslant t_{ox}$). Then the expression of holes flux is:

$$j_p = g\dot{D}Yu, \tag{3}$$

where g is the initial generation rate of electron–hole pairs in the oxide (7.6×10^{12} rad(Si)$^{-1}\cdot$cm^{-3})[14], and $\dot{D}$ is the dose rate during irradiation. From Eqs. (2) and (3), the expression of p_T can be solved:

$$p_T(u) = N_t[1 - \exp(-\sigma_p g D Y \cdot u)], \tag{4}$$

where $D = \dot{D}t$ is the total dose. Figure 4 presents the calculation results of $p_T(t_{ox}(x))$ from analytical equation (4) and TCAD simulation, which is consistent to some extent.

Finally, the trapped charge would reduce the threshold voltage values of elementary parasitic transistors. $Q_{ox}(x)$ is the equivalent surface density of charge, which can be calculated using $p_T(x,u)$. Then the threshold voltage values after irradiation can be expressed as:

$$\begin{aligned} V_T(x) &= V_{To}(x) - \frac{Q_{ox}(x)}{\epsilon_{SiO_2}/t_{ox}(x)} \\ &= \left[\phi_{S'S} - \frac{-\sqrt{2q\epsilon_{Si}N_A(x)\cdot 2\psi_F(x)}}{\epsilon_{SiO_2}/t_{ox}(x)} \right. \\ &\quad \left. + 2\psi_F(x)\right] - \frac{Q_{ox}(x)}{\epsilon_{SiO_2}/t_{ox}(x)}, \end{aligned} \tag{5}$$

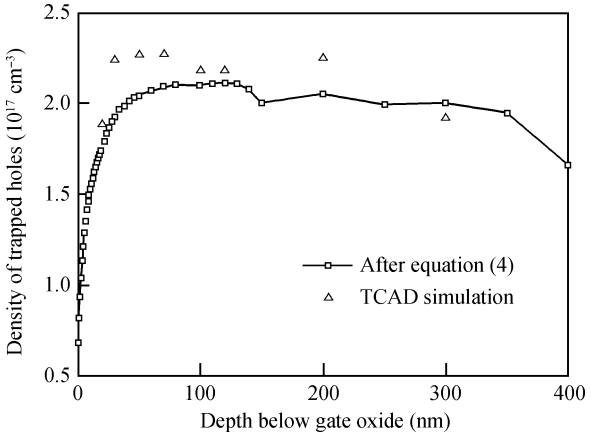

Fig. 4. Calculation results of $p_T(t_{ox}(x))$ analytical equation (4) and TCAD simulation presented as an example, where $N_T = 3 \times 10^{17}$ cm^{-3}, $\sigma_p = 1 \times 10^{-12}$ cm^2, $D = 8 \times 10^4$ rad(Si).

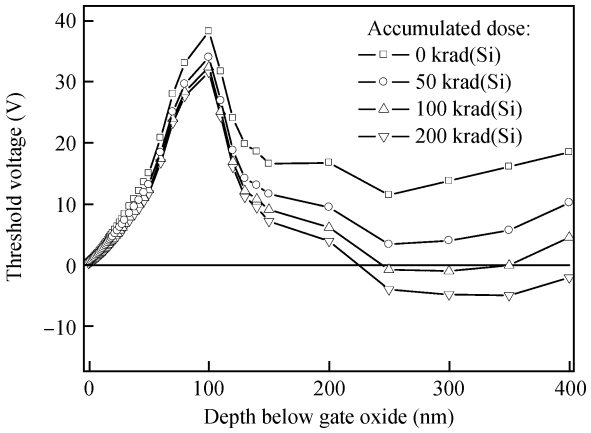

Fig. 5. Calculation results of threshold voltage values before and after irradiation according to Eqs. (4), (5) and (6).

where $N_A(x)$ is the doping density of substrate next to the STI sidewall, and $\psi_F(x)$ is the corresponding Fermi potential. Since the hole traps are located within a few nanometers of the interface[2], we get an estimate that $Q_{ox}(x)$ can be connected to using the equation below:

$$Q_{ox}(x) = p_t(x)qd = N_t q[1 - \exp(-\sigma_p g D Y u)]d, \tag{6}$$

where d is the equivalent distance from the boundary of trapped charge to the interface.

According to Eqs. (4), (5) and (6), threshold voltage values before and after irradiation can be calculated (Fig. 5). For the non-irradiated device, $V_t(x)$ reaches its maximum when the depth below gate oxide equals about 100 nm because of the opposite trends of $Y(x)$ and $t_{ox}(x)$. During irradiation, the density of trapped charge gradually increases, and then the $V_t(x)$ value is reduced to a negative region first at the lower part of STI sidewall due to retrograde well doping. Considering the high doping density and comparatively short collection path length in the nearby oxide, silicon near the upper part of the STI sidewall is the hardest to turn on. Figure 6 presents the distribution of current density in the channel with different accumulated doses from TCAD simulation, from which we can see the inversion emerging along with the increase of accumulated

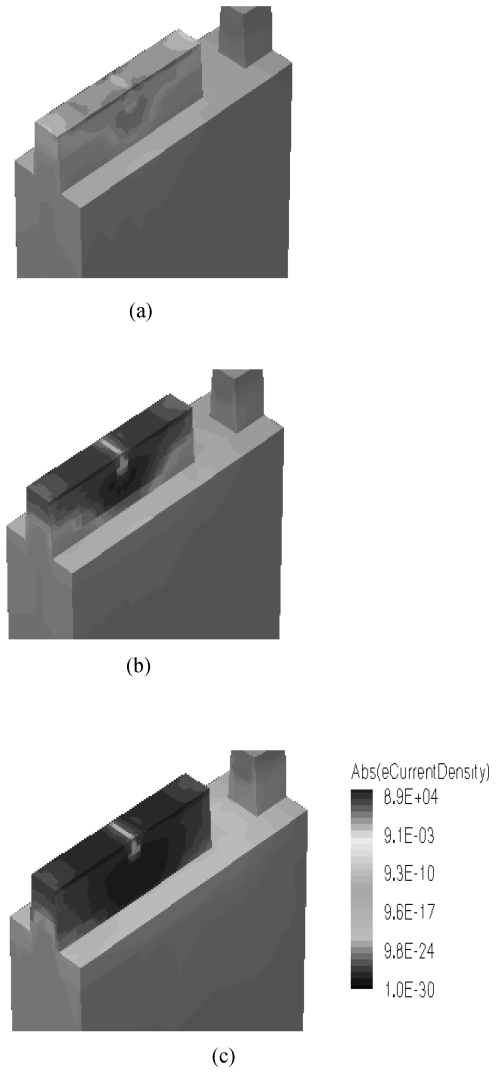

Fig. 6. Distribution of current density in the channel with different accumulated doses, where the turning on of parasitic conduction path can be seen. (a) 50 krad(Si). (b) 100 krad(Si). (c) 200 krad(Si).

dose. And it suggests that the lower part of the STI sidewall contributes more to the turning on of the parasitic conduction path.

3. Comparison between different leakage paths

Radiation-induced intra-device leakage is the leakage current flowing from the drain of a single MOS device to the source, like the circumstance shown in Fig. 6. The conduction path of intra-device leakage is actually a parallel combination of elementary parasitic transistors. So once any of these elementary transistors turns on, the whole intra-device leakage will increase to a high value. Radiation-induced inter-device leakage is the leakage current flowing between different devices. Its conduction path can be described as an arrangement of elementary parasitic transistors in series. That means inter-device leakage will increase obviously only when every elementary parasitic transistor is turned on. So generally speaking, inter-device leakage due to any kinds of parasitic structures should be less than the intra-device leakage. Figure 7 presents TCAD simulation and the experimental results of the

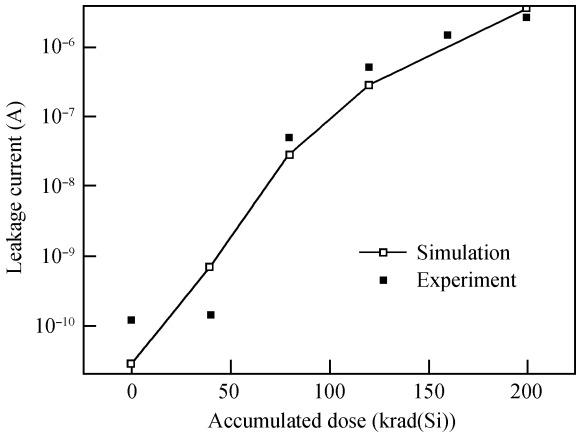

Fig. 7. Off-state intra-leakage current ($V_{gs} = 0$ V, $V_{ds} = 0.1$ V) varying with accumulated dose from TCAD simulation and experiment results.

off-state intra-leakage current ($V_{gs} = 0$ V, $V_{ds} = 0.1$ V) varying with accumulated dose. The experiment is executed using a Cobalt-60 γ source. The sample is one nMOSFET with W/L equal 0.3/0.24 μm and irradiated under the worst bias condition($V_{gs} = 2.5$ V) with a dose rate of 50 krad(Si)/s.

The different parasitic structures related to inter-device leakage are listed in Table 3, and they are named as leakage paths No. 1 – No. 5. Leakage path No. 1 is similar to a structure from a silicon strip detector in high-energy physics but often used as a study object for inter-device leakage due to its simplicity. Leakage paths No. 2 – No. 5 belong to parasitic structures from real CMOS integrated circuits. When a leakage path uses Polysilicon as the gate material, the corresponding gate dielectric will be an STI oxide. Then if a leakage path uses the lowest layer of metal (Metal 1) as the gate material, combination of STI and deposited oxide between Metal 1 and the diffusion region will behave as the gate dielectric.

From Fig. 8, leakage path No. 1 is composed of thin, medium, and thick oxide elementary parasitic transistors. This leakage path will be deteriorated only when all elementary transistors related to STI sidewall and STI base are turned on. And leakage path No. 2 only contains elementary transistors with a uniform oxide. In section II, the whole process of charge build-up in the STI sidewall and then turning on the elementary parasitic transistors is studied in detail. The conclusion is that the lower part of the STI sidewall is inclined to reduce the threshold voltage to become negative for 0.25 μm technology. So a qualitative estimation can be made that leakage path No. 2 would be easier to deteriorate than path No. 1. Figure 8 also presents a schematic picture of No. 3 leakage path existing in a real IC circuit.

From Fig. 9, radiation-induced inter-device leakage of parasitic structure No. 2 may exceed 1 nA when the accumulated dose equals 200 krad(Si). Contrary to that, inter-device leakage of structure No. 1 is about 2 pA with $W = 0.69$ μm and $L = 0.6$ μm in the same circumstance.

Leakage paths No. 3 – No. 5 use the lowest layer of metal (Metal 1) as the gate material, and 1.4 μm SiO_2 as the corresponding gate dielectric. Compared to those using the STI as a gate dielectric, the charge yield value $Y(x)$ in the STI region

Table 3. Classification of radiation-induced inter-device leakage paths existing in real ICs or commonly studied in former studies.

No.	Drain/Source	Gate/dielectric	Description	Existing in real IC?
1	n+/n+	Polysilicon/STI	Parasitic structure commonly studied in former work	No
2	n-well/n-well	Polysilicon/STI	Leakage path between the n-well regions with a poly gate strip placed above	Yes
3	n+/n+	Metal 1/STI+SiO_2(1 μm)	Leakage path between the n+ drain/source regions of different p-channel devices	Yes
4	n+/n-well	Metal 1/STI+SiO_2(1 μm)	Leakage path between nwell and the n+ drain/source region of a nearby p-channel device	Yes
5	n-well/n-well	Metal 1/STI+SiO_2(1 μm)	Leakage path between the n-well regions with a metal strip placed above	Yes

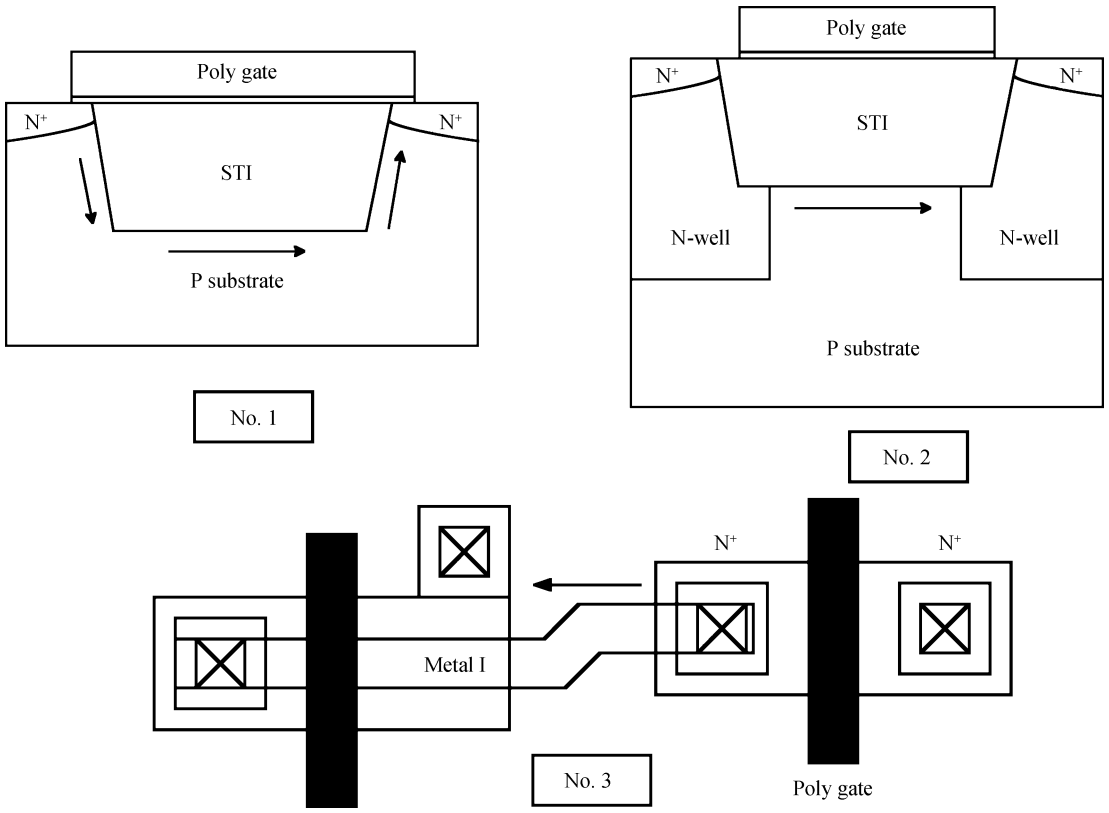

Fig. 8. Schematic pictures of leakage paths No. 1 to No. 3, possible flowing paths of leakage are presented by arrows.

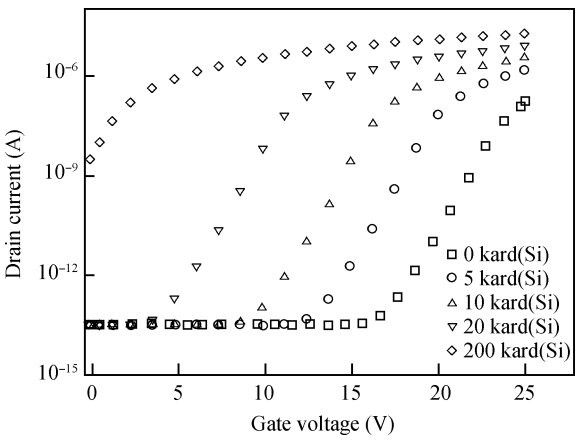

Fig. 9. I_d–V_{gs} characteristics of leakage path No. 2 with $W = 0.69$ μm, $L = 0.8$ μm, $V_d = 2.5$ V and $V_b = V_s = 0$ V before and after irradiation from TCAD simulation.

will be much smaller considering the whole oxide depth. And the collection length value $t_{ox}(x)$ will be bigger. Among the three kinds of structures, leakage path No. 5 is similar to No. 2 with N-well regions as both drain and source, so leakage path No. 5 would be the most sensitive to the total dose effect.

From Fig. 10, radiation-induced inter-device leakage of parasitic structure No. 5 is about 0.3 nA when the accumulated dose equals 200 krad(Si). Contrary to that, inter-device leakage of structure No. 1 is about 0.01 pA with $W = 0.69$ μm and $L = 0.6$ μm in the same circumstance.

The inter-device leakage current between adjacent devices is actually a function of parasitic structure, oxide thickness (t_{ox}), doping concentration in nearby silicon (N_A), gate bias during irradiation and test bias after irradiation. For example, although parasitic structures with N-well as both drain and source are comparatively more sensitive to the TID effect, N-well regions are commonly connected to the same power supply. That means although there is a possible conduction path

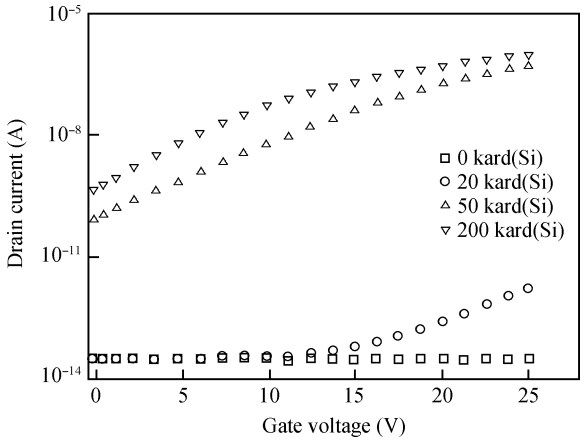

Fig. 10. I_d–V_{gs} characteristics of leakage path No. 5 with $W = 0.69$ μm, $L = 0.8$ μm, $V_d = 2.5$ V and $V_b = V_s = 0$ V before and after irradiation from TCAD simulation.

between two N-wells, there exists no voltage discrepancy. So leakage paths No. 2 and No. 5 from Table 3 will not be a problem in a real CMOS integrated circuit.

In Table 3, only parasitic structures No. 3 and No. 4 fulfill the requirements that both exist in real ICs and with a voltage discrepancy between the drain and source during test conditions. But they are harder to turn on due to the insensitivity of elementary transistors near the upper part of the STI sidewall.

4. Conclusion

Radiation-induced inter-device leakage is studied in this paper using an analytical model and TCAD simulation. There were some different opinions in explaining the process of defect build-up in the trench oxide and the parasitic leakage path turning on from former studies. Using theoretical analysis, every possible variable is considered, not just the change of electric field or oxide thickness independently. Inter-device leakage is smaller than intra-device leakage for any possible structure. Inter-device leakage paths can be classified into five categories. Among these classifications, parasitic structures with N-well as both drain and source are comparatively more sensitive to the TID effect when a voltage discrepancy exists between the drain and source region. Inter-device leakage of this parasitic structure may exceed 1 nA when the accumulated dose equals 200 krad(Si). Since N-well regions are commonly connected to the same power supply, this kind of structure will not be a problem in a real CMOS integrated circuit. Contrary to that, parasitic structures with the lowest layer of metal (Metal 1) as the gate material, 1.4 μm SiO_2 as the corresponding gate dielectric, and n^+ doping as the drain or source region (leakage paths No. 3 and No. 4 from Table 3) are far less sensitive because silicon near the upper part of the STI sidewall is harder to turn into an inversion state. Inter-device leakage of these parasitic structures is less than 1 pA when the accumulated dose equals 200 krad(Si). In a word, possible conduction paths of inter-device leakage existing in real ICs and under real electrical circumstances are not very sensitive to the TID effect. This conclusion is made using analysis under 0.25 μm technology. Furthermore, along with the reduced feature size, the value of channel doping will gradually increase and make the elementary parasitic transistors corresponding to the upper part of STI oxide even harder to turn on. Thus although the intra-device leakage may still be obvious, the radiation-induced inter-device leakage current will grow smaller and smaller.

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