A 6th order wideband active-RC LPF for LTE application*

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Abstract: A low power, highly linear active-RC filter is presented. This filter is synthesized from a low pass 6 order Chebyshev RLC ladder, and exhibits a reconfigurable bandwidth (10 MHz, 50 MHz). In order to meet the high cutoff frequency (50 MHz) and strict adjacent channel rejection requirements, a novel operational amplifier based on a new compensation technique is used, which optimizes high frequency filter performance and minimizes current consumption. This filter is fabricated in a 0.18 μm CMOS process, the measurement results indicate that the filter provides 10 MHz and 50 MHz selectable bandwidth, and excellent adjacent channel rejection: –15.3 dB at 12.5 MHz with 10 MHz cutoff frequency, –8.3 dB at 60 MHz with 50 MHz cutoff frequency, three times out-band rejection more than 60 dB while the in-band ripple is less than 1 dB.

Key words: active-RC; compensation amplifier; pole-zero; reconfigurable

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1. Introduction

3G is one of the promising solutions used for wireless communication and, recently, the next generation of long term evolution (LTE) has been proposed and standardized. In LTE, carrier aggregation allows the deployment of bandwidths of up to 100 MHz, enabling peak target data rates in excess of 1 Gb/s in downlink and 500 Mb/s in uplink[1]. When direct conversion architecture is employed for those systems, a low pass filter (LPF) with a selectable bandwidth of 10/50 MHz is required.

In this filter design, the strict adjacent-band rejection and out-band rejection constrain the selection of the LCR prototype. Owing to the stringent adjacent channel rejection, Chebyshev filters are more suitable and require less orders than Butterworth filters. Owing to the requirement of enough out-band rejection and minimize in-band ripple, Chebyshev-I filters are more suitable than Chebyshev-II, ellipse filters do. Based on the requirements of adjacent-band rejection and out-band rejection, a low pass six order Chebyshev-I RLC prototype is chosen, shown in Fig. 1.

Two structures can be selected to realize the filter: G_m–C and active-RC. G_m–C filters are generally used since G_m amplifiers have high bandwidth[2]. On the other hand, active-RC filters have not been considered appropriate for wideband applications since they require a high unit gain bandwidth (GBW) operational amplifier (OPAMP), hence the large power dissipation. However, active-RC filters have wide dynamic ranges and are suitable for LTE since orthogonal frequency division multiplexing (OFDM) with 64 quadrature amplitude modulation (QAM) requires high linearity. In this paper, a novel operational amplifier is introduced, which demonstrates a very good compromise between high frequency performance and the current consumption in an active-RC filter. An 8.5 times boost is applied to the dominant pole of the amplifier relative to traditional compensation without causing any stability problems.

2. Filter architecture

Figure 2 shows the proposed filter architecture: six order, Chebyshev-II, 10 MHz/50 MHz bandwidth reconfigurable active RC type. The top-level architecture mainly consists of a cascade of three biquad stages, which is preferred over other configurations, such as the leapfrog[3,4], because of its straightforward utilization and easily modifiable transfer function. To compensate the variation of cutoff frequency due to process, voltage and temperature (PVT), an auto frequency calibration (AFC) is also given in this design.

3. Filter design

3.1. Novel operational amplifier design

In order to expand the amplifier's bandwidth without sacrificing gain and consuming more current, a new compensation technique is adopted. Compared with the conventional compensation amplifier[5], the novel idea places two cross-coupled capacitor C_f and series resistor R_f between the first and second

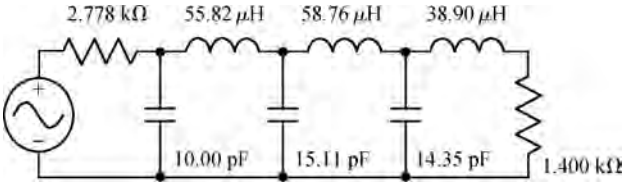

Fig. 1. LCR prototype.

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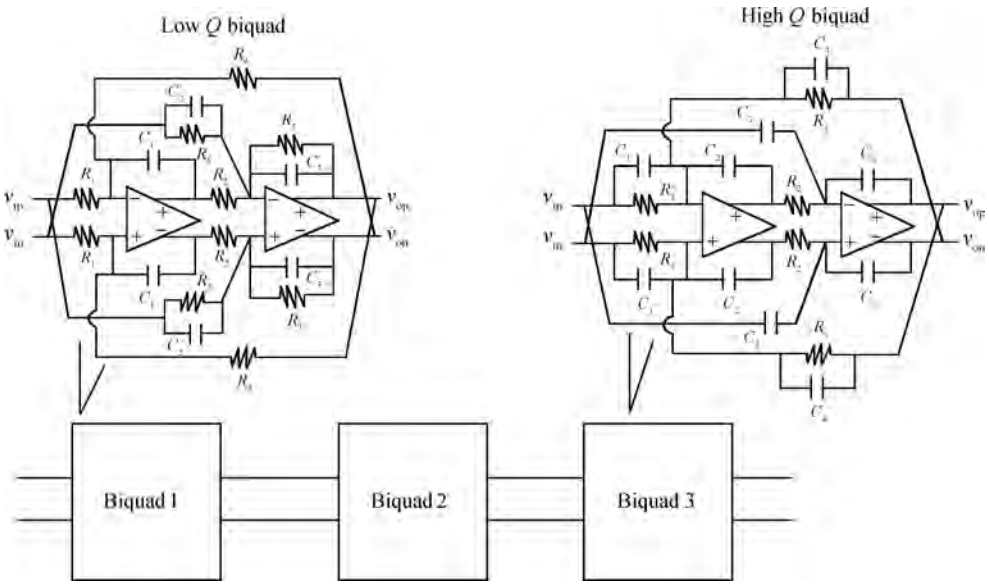


Fig. 2. Active RC filter architecture.

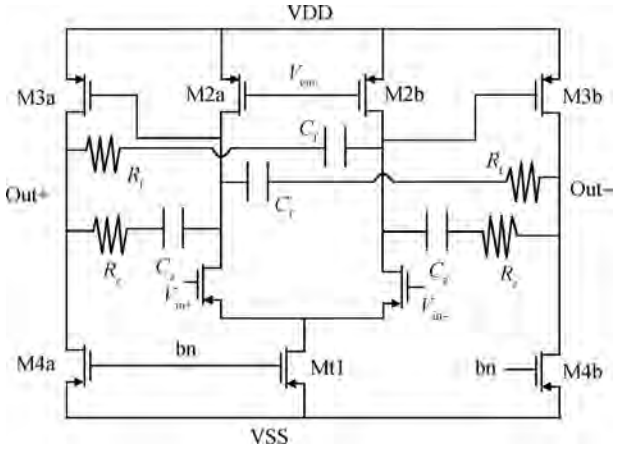


Fig. 3. Novel compensation amplifier.

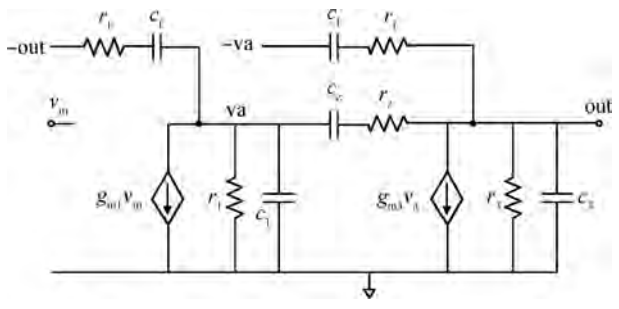


Fig. 4. Small signal model of the amplifier.

stages, as shown in Fig. 3. For detailed discussion, the simplified AC equivalent model of the amplifier is presented in Fig. 4.

In Fig. 4, c_1 represents the parasitic capacitor of stage one, and c_3 represents the sum of the load capacitor and parasitic capacitor of stage two. r_1 is the resistance seen from node va, which is equal to the native resistance of M2a in parallel with the native resistance of M1a, namely $r_{o1}//r_{o2}$. The resistance r_3 stands for the output resistance of the amplifier, equals to $r_{o3}//r_{o4}$. Using Kirchhoff's current law at node "v_a" and node "out", the current conservation equations (1) and (2) can be achieved, as shown below:

$$\frac{v_a}{r_1||\dfrac{1}{c_1 s}}+\frac{v_a-\text{out}}{r_z+\dfrac{1}{c_z s}}+g_{m1}v_{in}+\frac{v_a+\text{out}}{r_f+\dfrac{1}{c_f s}}=0, \quad (1)$$

$$g_{m3}v_a+\frac{\text{out}}{r_3||\dfrac{1}{c_3 s}}+\frac{\text{out}-v_a}{r_z+\dfrac{1}{c_z s}}+\frac{\text{out}+v_a}{r_f+\dfrac{1}{c_f s}}=0. \quad (2)$$

From Eqs. (1) and (2), the differential transfer function of the novel compensation amplifier can be calculated. The numerator and denominator of the transfer function is shown in Eq. (3):

$$\begin{aligned}\text{num}=&\, g_{m1}v_{in}[c_z s(r_f c_f s+1)-g_{m3}(r_z c_z s+1)(r_f c_f s+1)\\&-c_f s(r_z c_z s+1)](r_z c_z s+1)(r_f c_f s+1),\end{aligned}$$

$$\begin{aligned}\text{den}=&\,[c_z s(r_f c_f s+1)-c_f s(r_z c_z s+1)][c_z s(r_f c_f s+1)\\&-g_{m3}(r_z c_z s+1)(r_f c_f s+1)-c_f s(r_z c_z s+1)]\\&-[(r_z c_z s+1)(r_f c_f s+1)(c_1 s+1/r_1)\\&+c_z s(r_f c_f s+1)+c_f s(r_z c_z s+1)]\\&\times[(c_3 s+1/r_3)(r_z c_z s+1)(r_f c_f s+1)\\&+c_z s(r_f c_f s+1)+c_f s(r_z c_z s+1)].\end{aligned} \quad (3)$$

Equation (3) shows that the transfer function has six poles and four zeros, which is difficult to analyze manually. In order to have an in depth observation of the novel amplifier's behavior, firstly, we can assume that the denominator of the transfer function looks like the following:

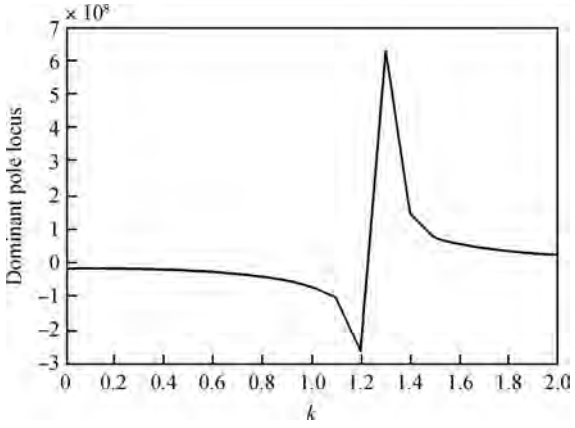


Fig. 5. Pole locus of the novel amplifier.

$$D(s) = \prod_{i=1}^{6} (s - p_i). \quad (4)$$

The expansion of this polynomial is a 6th order polynomial:

$$D(s) = s^6 + c_1 s^5 + c_2 s^4 + c_3 s^3 + c_4 s^2 + c_5 s^1 + c_6, \quad (5)$$

where

$$c_5 = -p_1 p_2 p_3 p_4 p_5 - p_6(p_1 p_2 p_3 p_4 + p_2 p_3 p_4 p_5 + p_1 p_3 p_4 p_5 + p_1 p_2 p_4 p_5 + p_1 p_2 p_3 p_5), \quad (6)$$

$$c_6 = p_1 p_2 p_3 p_4 p_5 p_6, \quad (7)$$

$$-\frac{c_6}{c_5} = \frac{p_6}{1 + p_6\left(\frac{1}{p_5} + \frac{1}{p_4} + \frac{1}{p_3} + \frac{1}{p_2} + \frac{1}{p_1}\right)}, \quad (8)$$

Assuming the dominant pole is p_6, whose absolute value is much less than that of the other poles, an appropriate estimation of Eq. (8) can be obtained, as shown in Eq. (9):

$$-\frac{c_6}{c_5} = \frac{p_6}{1 + p_6\left(\frac{1}{p_5} + \frac{1}{p_4} + \frac{1}{p_3} + \frac{1}{p_2} + \frac{1}{p_1}\right)} \approx p_6. \quad (9)$$

According to Eq. (9), the dominant pole of Eq. (3) can be represented by Eq. (10). When $c_f = 0$, the novel compensation amplifier turns to a traditional two stage amplifier, then the dominant pole expression changes to Eq. (11):

$$p_{\text{domi, novel}} = -1/r_1 r_3 \left[g_{m3}(c_z - c_f) + \frac{2(r_z c_z + r_f c_f)}{r_1 r_3} + \frac{c_1 + c_z + c_f}{r_3} + \frac{c_3 + c_z + c_f}{r_1} \right], \quad (10)$$

$$p_{\text{domi, conventional}} = -1/r_1 r_3 \left[g_{m3} c_z + \frac{2 r_z c_z}{r_1 r_3} + \frac{c_1 + c_z}{r_3} + \frac{c_3 + c_z}{r_1} \right]. \quad (11)$$

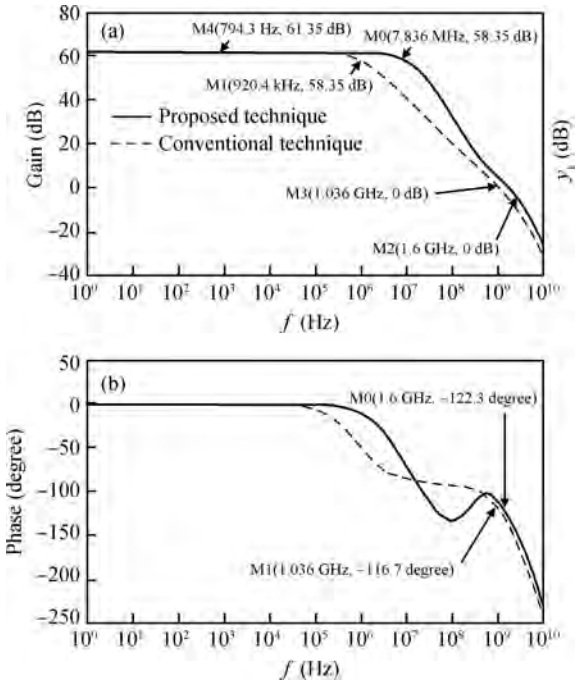


Fig. 6. (a) Amplifier gain and (b) phase of the proposed technique and the conventional RC compensation network.

For a stable circuit, the poles are located in the left half of the x–y plane. In order to estimate the dominant pole characteristic of the novel compensated amplifier more conveniently, supposing that the values of $c_1, r_1, c_3, r_3, c_z, r_z, r_f$ in Eq. (10) are fixed, taking $c_f = kc_z$, the locus of the dominant pole in the novel compensated amplifier (Eq. (10)) can be plotted using Matlab, which is shown in Fig. 5.

In Fig. 5, the x axis is k, and y axis is the dominant pole locus. When $k<1.2$, the pole is negative, $k\geqslant 1.2$, the pole goes to right-half of the x–y plane, and the system becomes unstable. When $k<1.2$, the dominant pole location goes to a higher frequency along with the increase of k. For example, when $k = 0$, the dominant pole of the amplifier is 0.92 MHz, when k nears 1.2, the dominant pole of the amplifier is 41.4 MHz, forty times larger than the case $k = 0$ (the traditional compensation case). So it is clear that the novel compensation technique of the two-stage amplifier can dramatically expand the dominant pole without consuming more current.

For stability consideration, let $c_f = c_z$ (k=1). This new compensation technique also provides a double zero character to the amplifier. It adds positively to the phase response, thus moving the –180 intersect at a much higher frequency. Figure 6 illustrates a comparison of the gain and phase achieved when the above described technique and the classic pole-splitting method are applied to the amplifier. From Fig. 6 and Table 1 we can see that the proposed technique offers an 8.5 times increase in the frequency of the amplifier's dominant pole. The unity gain bandwidth also increased 1.6 times than the traditional one with only a 5.6° phase margin less.

3.2. Resistor ladder design

In this work, a variable resistor ladder is used to compensate the variation of cutoff frequency due to PVT, but the non-

Table 1. Simulation result of the compared compensation technique.

Parameter	This work	Conventional technique
Dominant pole (MHz)	7.836	0.92
GBW (GHz)	1.6	1.036
Phase margin (°)	57.5	63.3

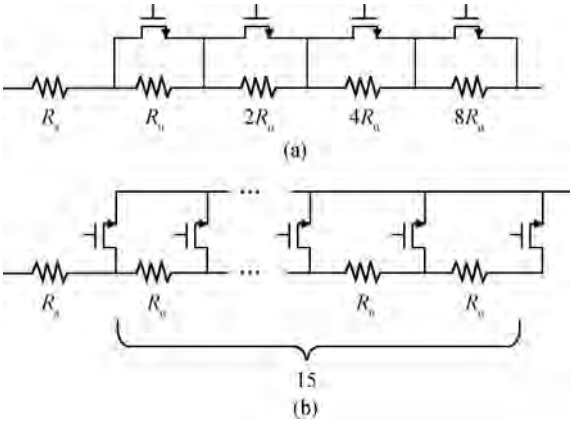


Fig. 7. (a) Binary-weighted resistor bank. (b) One-hot variable resistor.

ideality of the resistor ladder also causes the Q changing in the filter. The variable resistor consists of NMOS switches and unit-resistors. The gate widths of the NMOS switches should be large enough to ensure that on-resistances remain negligible with respect to the unit resistance under PVT variations. However, in scaled CMOS technologies, an on-resistance per unit gate width is very high due to low power supply voltages. The gate width of the switches becomes large, and so does the parasitic capacitance of the switches. This large capacitance introduces poles comparable to or even lower than the GBW of an amplifier. Therefore, the variable resistor is very important for a filter.

Figures 7(a) and 7(b) show a 4-b binary-weighted resistor bank and a one-hot serially connected variable resistor, respectively. The frequency response of the one-hot resistor is much better than that of the binary-weighted resistor, since half of the parasitic capacitance is connected to the virtual ground of an active-RC filter and it does not contribute to the frequency response. So in this design, we choose the resistor structure in Fig. 7(b).

3.3. On-chip automatic turning technique

In order to turn the filter to the desired cutoff frequency, an on-chip automatic turning circuit is required. As shown in Fig. 8, the turning loop consists of an oscillator, a reference filter, two binary counters (counters A and B), a digital comparator and a latch. The oscillator has the same structure as the high-Q biquad shown in Fig. 2, except that C_5 between two amplifiers is omitted. By turning the oscillating frequency f_o of the oscillator, the –3 dB frequency of each biquad in the filter will be turned, as does the filter's cutoff frequency.

f_o is measured by the A counters at first, which is controlled by a reference clock signal f_{clk}. The value is latched at the end of each clock period, compared with the digital input

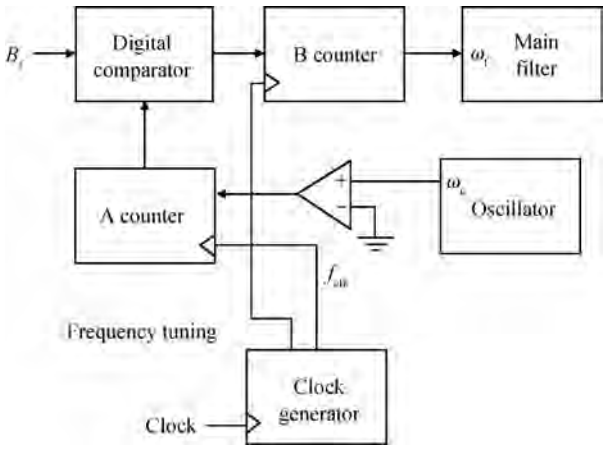


Fig. 8. Automatic turning system of filter.

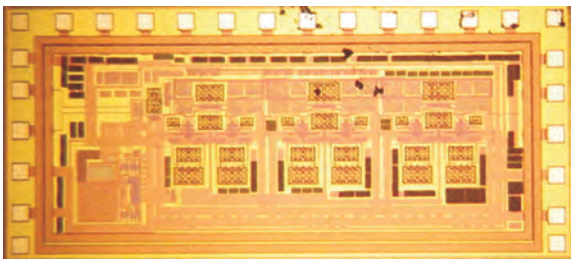


Fig. 9. Chip photo.

word B_f using the digital comparator. When the value of the A counter is less (greater) than the value B_f, the B counter which control the filter's resistor ladder will be decreased (increased) by one, to turn the filters cutoff frequency. When the value of A counter is equal to B_f, f_o reaches the desired value, and the B counter is unchanged. The desired oscillating frequency can be written as:

$$\omega_d = 2\pi f_d = 2\pi B_f f_{clk}. \quad (12)$$

Ideally, $f_d = f_o$. However, due to the error from measuring f_o and the finite filter's resolution, f_o may deviate from the ideal value. In order to improve the turning resolution, the clock signal should have a long period together with a long count of A.

4. Measurement results

The proposed filter was fabricated in a TSMC 0.18 μm process with a 1.8 V supply. The chip micrograph is shown in Fig. 9, where a filter core circuit occupies an area of 1.0 × 0.7 mm^2. The integrated capacitors and resistors were implemented with MIM capacitors and high resistivity poly-silicon resistors.

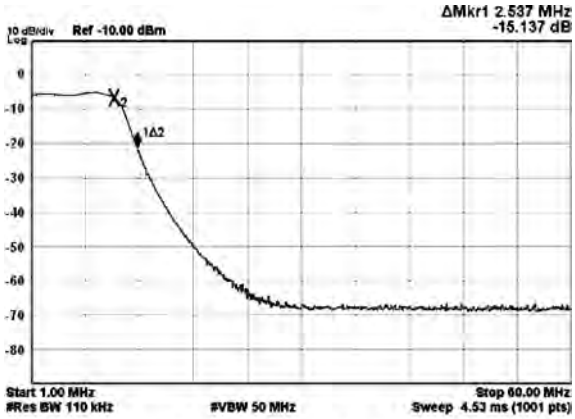
Figure 10 illustrates the measured magnitude response of cutoff frequency of 10 MHz and 50 MHz after frequency turning. As shown in the magnitude response, the filter indicated excellent adjacent channel rejection: –15.3 dB at 12.5 MHz with 10 MHz cutoff frequency, –8.3 dB at 60 MHz with 50 MHz cutoff frequency, which meets the steep stop-band attenuation requirement in LTE.

Table 2. Performance summary.

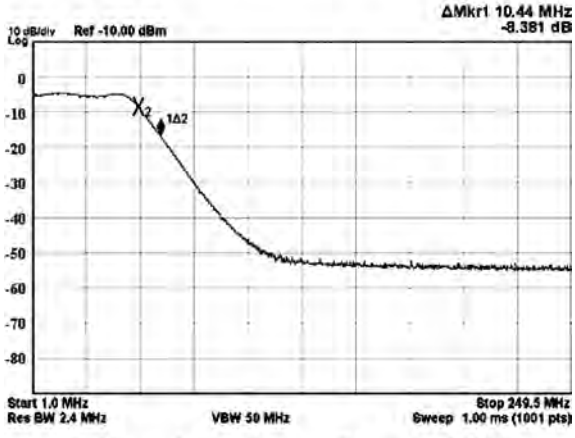
Parameter	Value
Technology	TSMC 0.18 μm RF process/1.8 V
Filter order/ type	Six order/Chebyshev-II
Cutoff frequency	10 MHz/50 MHz
Input referred noise	72 nV/$\sqrt{\text{Hz}}$
In-band IM3	–57.2 dB @ 10 MHz/–58.6 dB @ 50 MHz
In-band IIP3	18.6 dBm @ 10 MHz/19.3 dBm @ 50 MHz
Power consumption	18 mW
Die area	1.0×0.7 mm^2

Table 3. Comparison with recently published works.

Reference	Process (μm)	Topology	Order	Power/Pole (mW/pole)	Cutoff range (MHz)	IIP3 (dBm)
Ref. [6]	0.25	Acitve_RC	5	11	20	31
Ref. [7]	0.18	Acitve_RC	4	5	10	32
Ref. [8]	0.13	Active_RC	4	0.7 mA/2.7 mA	2.11/11	21
This work	0.18	Active_RC	6	3	10/50	18.6



(a) Magnitude response of cutoff frequency 10 MHz



(b) Magnitude response of cutoff frequency 50 MHz

Fig. 10. The measured magnitude response of filter cutoff frequency.

An in-band 3rd intermodulation (IM3) of –57.2 dB is obtained at 10 MHz cutoff frequency when the input powers of two tones are –10 dBm (at 3 MHz and 4 MHz), as shown in Fig. 11. According to the equation: IIP3 $= \frac{\Delta P(\text{dB})}{2} + P_{\text{in}}$, the 3rd input intercept point (IIP3) of the filter is 18.6 dBm. Table 2 shows the measured result of the proposed filter, and

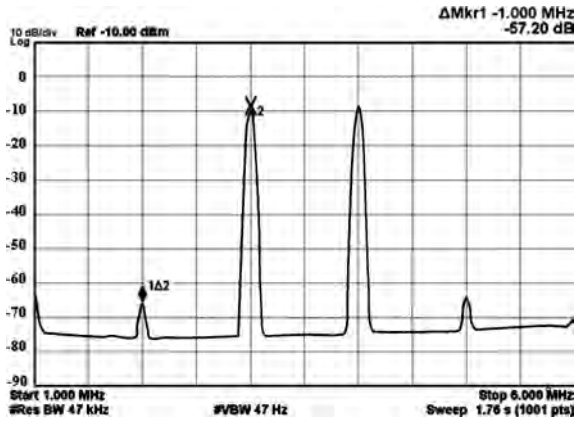


Fig. 11. The measured in-band IM3.

Table 3 gives a comparison between this work and other recently reported works. The power dissipation of the filter is 18 mA, which can be cut down slightly when shrinking the width of the opamp in the low Q biquad of this circuit.

5. Conclusion

A six-order active-RC filter with modifiable bandwidth was presented. The amplifier of the filter utilizes a new compensation technique, which allows for optimized high frequency filter performance and minimized current consumption. A filter prototype has been fabricated in a 0.18 μm CMOS process, the measurement result indicates that the filter provides 10 MHz and 50 MHz selectable bandwidth, excellent adjacent channel rejection: –15.2 dB at 12.5 MHz with 10 MHz cutoff frequency, –8.2 dB at 60 MHz with 50 MHz cutoff frequency, power consumption is 18 mA.

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