Worst-case total dose radiation effect in deep-submicron SRAM circuits*

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Abstract: The worst-case radiation effect in deep-submicron SRAM (static random access memory) circuits is studied through theoretical analysis and experimental validation. Detailed analysis about the radiation effect in different parts of circuitry is presented. For SRAM cells and a sense amplifier which includes flip-flop structures, their failure level against ionizing radiation will have a connection with the storage state during irradiation. They are inclined to store or read the same state as the one stored during irradiation. Worst-case test scheme for an SRAM circuit is presented, which contains a write operation that changes the storage states into the opposite ones after irradiation and then a read operation with opposite storage states. An irradiation experiment is designed for one 0.25 μm SRAM circuit which has a capacity of 1 k $\times$ 8 bits. The failure level against ionizing radiation concluded from this test scheme (150 krad(Si)) is much lower than the one from the simplest test scheme (1 Mrad(Si)). It is obvious that the failure level will be overestimated if the simplest test scheme is chosen as the test standard for SRAM circuits against ionizing radiation.

Key words: worst-case test scheme; total dose effect; deep-submicron SRAM circuits
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1. Introduction

Metal–oxide–semiconductor (MOS) devices exposed to radiation will experience shifts in their performance parameters including threshold voltage and leakage current due to increased oxide trapped charge[1−3]. It is known that the shifts of parameters will have a strong connection with irradiation bias[4,5]. For nMOS transistors, the degradation will be more severe when biased with positive gate voltage ('ON' state) than a zero or negative value ('OFF' state)[6].

The total dose testing standard, MIL-STD-883, method 1019, emphasizes the use of worst-case test vectors (WCTVs) whenever possible[7]. Despite this emphasis, WCTVs are not always used in the total dose testing of VLSI circuits, resulting from the difficulty of identification. From a previous study, researchers usually choose the simplest test scheme to verify the failure level[8,9]. When the total dose effect of SRAM circuits is studied, common test methods may include static mode (power supply is on, but without reading or writing during irradiation), dynamic mode (continually implementing reading or writing during irradiation) and floating mode (power supply is off). If the static mode is used for example, a specific storage pattern should be chosen between all '1', all '0', checkerboard pattern, etc, and then the address inputs and data inputs should be set during irradiation. In short, lots of combinations are available when dealing with irradiation and test procedures and it is impossible to try them all.

As technologies change, a continuing trend is for devices to have smaller feature size and bigger capacity. This makes it even more difficult to define a reasonable set of irradiation and test vectors that ensure the worst case response for an SRAM circuit only by experience. Thus the analysis to identify the worst-case operating condition under which a circuit may be most vulnerable to radiation becomes increasingly important. Researchers from Vanderbilt University have made a great deal of effort to develop an identification method of the worst-case test vectors for combinational logic circuit and cell-based ASIC circuits[10−13]. However, their work can be reasonably used only in a combinational circuit to study logic failure.

In this paper, the worst-case total dose effect in deep-submicron SRAM circuits is studied using theoretical analysis and experimental validation. First, detailed analysis about radiation effect in different parts of circuitry are presented. Then the worst-case test scheme for an SRAM circuit is identified based on the analytical results. Finally, experimental results are presented to validate the conclusion above.

2. Radiation effect in deep-submicron SRAM circuits

From former studies, MOSFETs with feature size more than 1 μm are very sensitive to the total ionizing dose effect. The shifts of threshold voltage can be so obvious that the threshold voltage value might become below zero with an accumulated dose of even less than 100 krad(Si)[1]. Since semiconductors have scaled into the deep sub-micron and thin-gate oxides have brought inherent radiation tolerance, the threat of significant threshold voltage shifts resulting from total dose irradiation has been reduced. In fact, when the depth of gate oxide is less than 8 nm, this corresponding effect can be neglected to some extent[14]. Meanwhile, the radiation-induced

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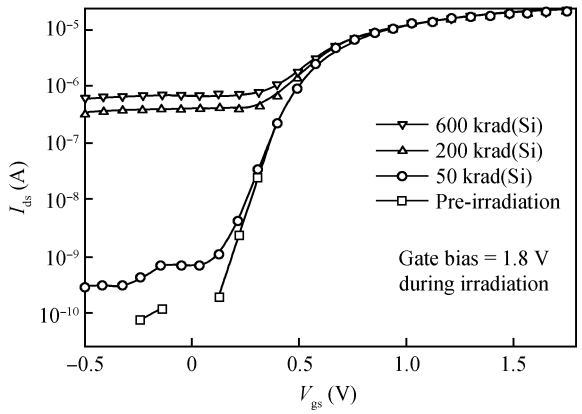

Fig. 1. I–V electrical curves of an nMOS transistor (W/L = 0.22/0.18 μm) after radiation exposure with a high gate voltage.

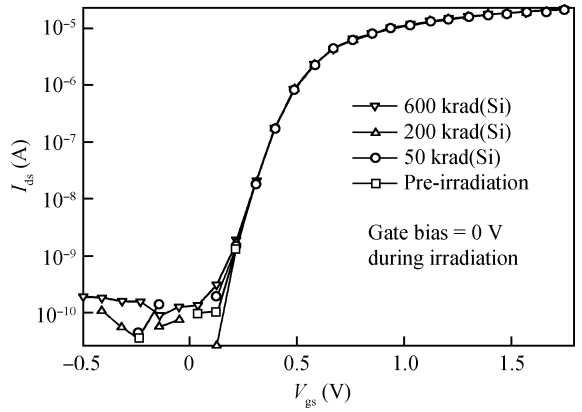

Fig. 2. I–V electrical curves of an nMOS transistor (W/L = 0.22/0.18 μm) after radiation exposure with a low gate voltage.

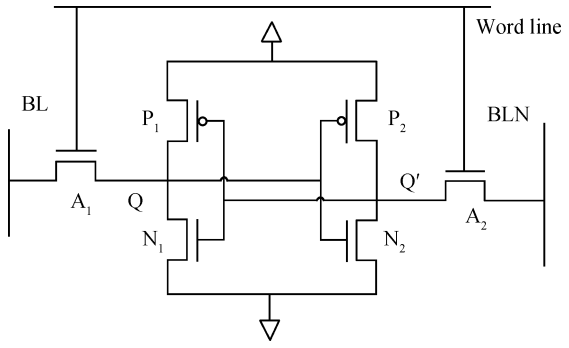

Fig. 3. Six-transistor SRAM cell.

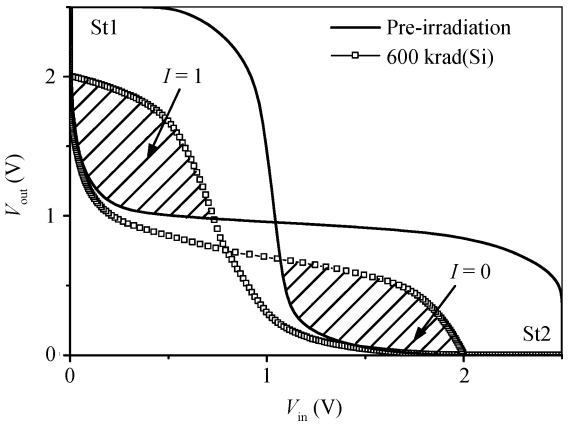

Fig. 4. Transfer characteristics of the inverters from a 6-T SRAM cell with feature size 0.25 μm. I represents the storage state of the cell during irradiation.

leakage current, which is caused by the positive charge trapping in the isolation layers, becomes one of the most significant problems of hardness assurance for modern CMOS technologies[15, 16]. I–V electrical curves of an nMOS transistor with feature size 0.18 μm (Fig. 1) exhibit this phenomenon clearly. From Fig. 1 and Fig. 2, we can see that the performance degradation of nMOS transistors does have a close connection with bias during irradiation.

The six-transistor SRAM cell shown in Fig. 3 consists of two cross-coupled driver transistors N_1 and N_2, two load transistors P_1 and P_2, and a pair of access elements A_1 and A_2. For the six-transistor SRAM cell with feature size 0.25 μm in this work, the stability of the two cross-coupled inverters can be graphically visualized in Fig. 4. Before irradiation, the transfer curves intersect at two stable points St1 and St2. Using the experimental results of MOSFETs after irradiation and circuit simulation tools, the total dose effect of CMOS circuits can be simulated. When accumulated dose equals 600 krad(Si), the high logic level degrades to less than V_{dd} because of the high leakage current, meanwhile the hold SNM (static noise margin) decreases regardless of whether the storage state during irradiation is '0' or '1', as shown in the shadow areas of Fig. 4, luckily there are still two stable points existing. That means the SRAM cell can keep holding the correct logical state. However, when the cell stores the '1' state during irradiation (I = 1), the margin for the cell to hold the '0' state decreases, but it becomes easier for the cell to hold the '1' state. In a word, the mismatch between the two storage states is enlarged.

The write operation of an SRAM cell is performed by forcing high and low voltages to a pair of bit lines (Fig. 3, BL and BLn). The corresponding write margin is to measure the voltage of the bit line required to flip the state. An adequate write margin is ensured by sizing the access transistor A_1/A_2 to be stronger than the pull up device P_1/P_2. Since the radiation effect of pMOS transistors with feature size entering the deep-submicron level is negligible, and the leakage current increase of an nMOS in an 'OFF' state is very small, the write margin of a deep-submicron SRAM cell can be said to be insensitive to the total ionizing dose effect.

Correct operations of write and data retention are very important for an SRAM circuit, but only these are not enough. The data stored in a cell has to be read nondestructively. To read a SRAM cell, the bit lines BL and BLn are pre-charged high to V_{dd} and the word line is then asserted. Since the leakage current increase of an nMOS in the 'ON' state is quite big, this extra current will flow through the corresponding bit line, which is against the normal condition. The transfer curves to calculate read margin values before and after irradiation are shown in Fig. 5.

From Fig. 5, mismatch of the cell can be seen clearly even before irradiation due to the cell design. The read margin for the '0' state (upper part) is bigger than the '1' state. After irradia-

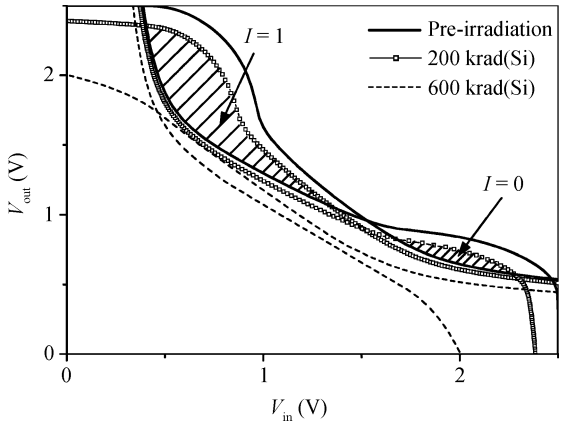

Fig. 5. Transfer characteristics of each side of the SRAM cell with feature size 0.25 μm before and after irradiation, from which the read margin values can be calculated.

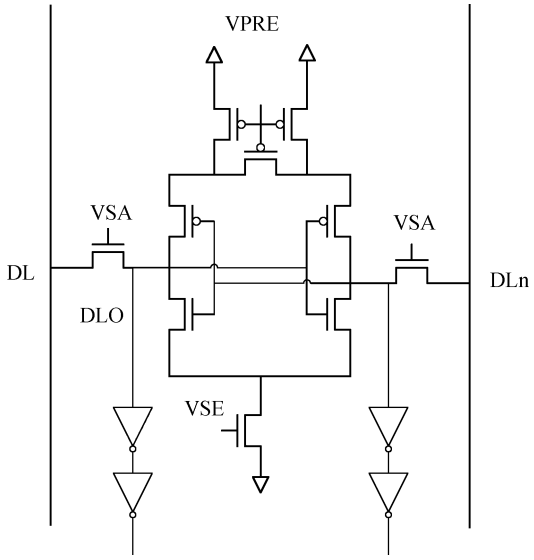

Fig. 6. Commonly used differential CMOS sense amplifier for SRAM circuits.

tion, the asymmetry in the transfer curves becomes more obvious. If the cell stores the '1' state during irradiation ($I = 1$), the margin for the cell to read a '0' state will decrease, meanwhile the margin value to read a '1' state will increase. A similar thing would happen for the '0' state ($I = 0$) that the cell would be inclined to read the same state as the one stored during irradiation. When the accumulated dose equals 200 krad(Si), the read operation will remain accurate no matter what the storage states are during and after irradiation. However, when the accumulated dose increases to 600 krad(Si), the cell can only read the same state as the storage one during irradiation, and the data stored in the cell would not be read nondestructively at all times.

Besides the cells, a whole SRAM circuit also includes other control circuitries, such as a sense amplifier, pre-charge circuit, decoders, address transition detector, I/O circuit, etc. Most SRAM designs use a differential sense amplifier to amplify the small signal differential voltage between the bit lines and then swing into a large signal output, as shown in Fig. 6.

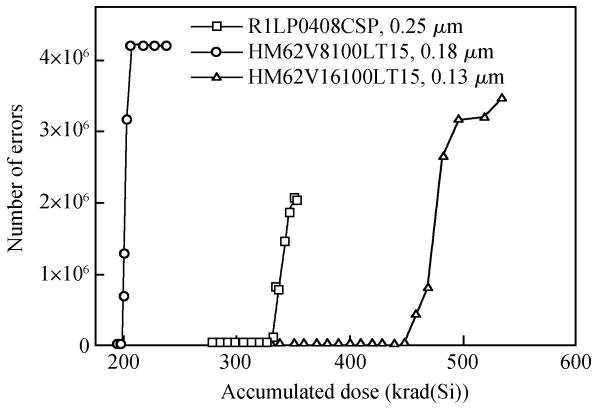

Fig. 7. The relationship between number of error bits and accumulated dose when implementing the ionizing dose test of several deep-submicron SRAM circuits using the simplest test scheme.

Since the sense amplifier includes a flip-flop structure, its degradation to radiation exposure would behave in the same way as an SRAM cell. Or rather, the failure level of the sense amplifier against ionizing radiation would have a connection with the storage state during irradiation. For example, if the last operation of the sense amplifier before irradiation is to read a '1' state from some SRAM cell and static mode is chosen during irradiation, it will store the '1' state till the next read operation after irradiation occurs. Then the read margin of the amplifier to the '0' state will decrease, while the margin to the '1' state will increase.

Unlike SRAM cells or sense amplifiers, other circuitries in an SRAM circuit only include static CMOS gates or other linear structures. So their failure levels to ionizing radiation only have relations to the input vectors during and after irradiation.

3. Identification of the worst-case test scheme

One simplest test scheme for irradiation test of an SRAM circuit is to first implement the write operation and make the cells store a specific pattern, then read them continually to check for possible failures[8, 9]. From the above section, the margin of SRAM cells and amplifiers to one state would even increase if they keep storing the same state as the one stored during irradiation. That means these two kinds of circuits would not fail using this simple test scheme where storage values are not changed during the whole test procedure. Thus only failures of other control circuitries would be seen in this kind of test against ionizing radiation. This conclusion has been validated by experimental results. Our group has implemented total ionizing dose tests of deep-submicron SRAM circuits including feature sizes of 0.25, 0.18, and 0.13 μm many times. When following this test scheme, the corresponding number of error bits would increase suddenly from zero to a big value, which may even be the total number of bits, when the accumulated dose arrives at a threshold value. This typical phenomenon of error bits increasing suddenly is shown in Fig. 7. If this kind of error was due to the failure of SRAM cells, Figure 7 would be smoother like upset bits changing with LET (linear energy transfer) value from a single event upset test, because of the variability between different cells. Thus the whole phe-

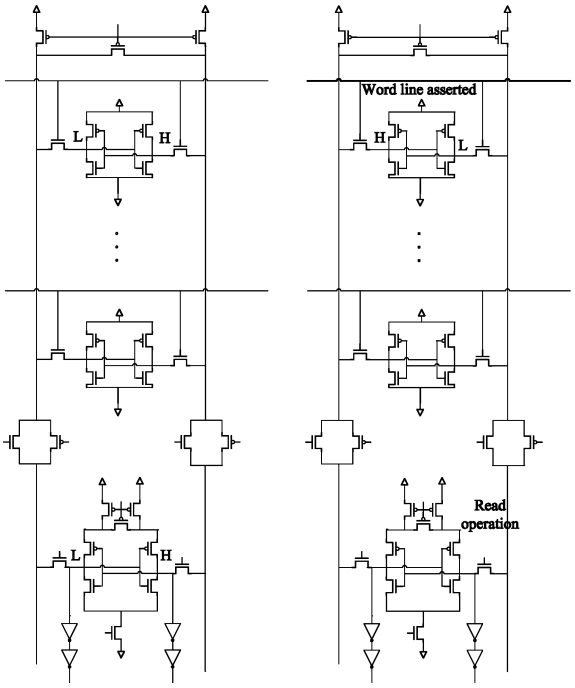

Fig. 8. Illustration of the worst-case test scheme for SRAM cells and a sense amplifier containing operation states during irradiation (left) and after irradiation (right).

nomena suggests failure of control circuitries to some extent, maybe decoder circuits, etc.

Considering the analysis above, it is certain that this test scheme is not consistent with the total dose testing standard, MIL-STD-883, method 1019, which emphasizes the use of worst-case test vectors (WCTVs) whenever possible. To fix the problem, the worst-case test scheme of an SRAM circuit should be identified where the failure of different circuitries would be visible to the utmost extent.

Since the emergence of performance degradation for SRAM cells and sense amplifiers demands operation with different storage states during and after irradiation, the worst-case test scheme is to maintain the same storage states during irradiation and then change the storage states into the opposite ones before the read test. From Fig. 4 and Fig. 5, a conclusion can be drawn that the read operation is more sensitive to radiation than data retention for this kind of SRAM cell with a feature size of 0.25 μm. In addition, the correctness of the sense amplifier can only be verified during the read operation. Thus the read operation with opposite storage states after irradiation should be included in the test scheme. To sum up, the worst-case test scheme of SRAM cells and sense amplifiers can be expressed in Fig. 8.

4. Experimental validation

To verify the analysis above, an irradiation experiment is designed for a 0.25 μm SRAM circuit which has a capacity of 1 k $\times$ 8 bits. Since the main purpose is to validate if the test scheme presented in this paper fulfills the requirement of the worst-case testing standard, two different test schemes are designed.

The simplest SRAM circuit test scheme is implemented

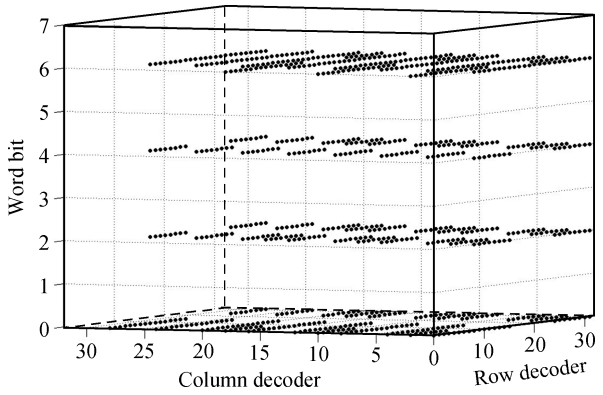

Fig. 9. Bitmaps of error bits when implementing the ionizing dose test of one 0.25 μm SRAM circuit using the worst-case test scheme, with accumulated doses equal to 150 krad(Si).

first. That means we execute the write operation and make the cells store a specific pattern (55H) at the beginning, then read them continually to check for possible failures. Till the total dose accumulated arrives at 1 Mrad(Si), no error bit is observed under this condition. Then an additional operation of rewrite is executed to verify the performance of the SRAM circuit. However, except for the pattern stored during irradiation (55H), no other patterns can be read completely correctly.

Then the test results from the scheme introduced in this paper are presented. When arranging the experiment following this scheme, we first execute the write operation and make the cells store a specific pattern (55H), and read them continually to check for possible failures. The difference from the first scheme is that an opposite storage pattern (AAH) is written into the SRAM circuit every 50 krad(Si) during irradiation and then a read operation is implemented to check for possible failures. Under this condition, error bits emerge during the read operation with storage pattern AAH when the accumulated dose reaches 150 krad(Si). Bitmaps of error bits are shown in Fig. 9 and Fig. 10. Considering the mismatch of read margin for different storage state, errors first occur for the read operation of cells with a '0' state while storing a '1' state during irradiation. Until about 240 krad(Si), errors corresponding to the read operation of cells with the '1' state while storing a '0' state during irradiation emerge too.

Failure level against ionizing radiation concluded from this test scheme (150 krad(Si)) is much lower than the one from the simplest test scheme (1 Mrad(Si)). It is obvious that the failure level would be overestimated if the simplest test scheme is chosen as the test standard for SRAM circuits against ionizing radiation. The test scheme introduced in this paper could inspect not only the performance degradation of control circuitries in an SRAM circuit, but also the degradation of SRAM cells and sense amplifiers. Thus it can be considered as the worst-case test scheme for deep-submicron SRAM circuits.

5. Conclusion

The worst-case radiation effect in deep-submicron SRAM circuits is studied through theoretical analysis and experimental validation. For SRAM cells and sense amplifiers, which includes flip-flop structures, their failure levels against ionizing

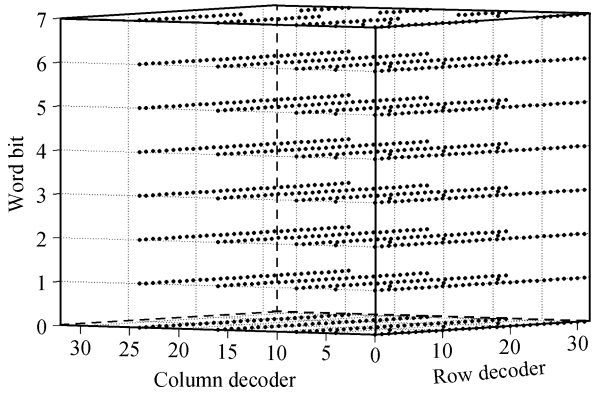

Fig. 10. Bitmaps of error bits when implementing the ionizing dose test of one 0.25 μm SRAM circuit using the worst-case test scheme, with accumulated doses equal to 240 krad(Si).

radiation would have a connection with the storage state during irradiation. They are inclined to store or read the same state as the one stored during irradiation. Other circuitries in a SRAM circuit only include static CMOS gates or other linear structures. Thus their failure levels against ionizing radiation only have relation to input vectors during and after irradiation.

Based on the theoretical analysis, a worst-case test scheme for SRAM circuit is presented which contains a write operation that changes the storage states into the opposite ones after irradiation and then the read operation with opposite storage states. An irradiation experiment is designed with one 0.25 μm SRAM circuit which has a capacity of 1 k $\times$ 8 bits. The failure level against ionizing radiation concluded from this test scheme (150 krad(Si)) is much lower than the one from the simplest test scheme (1 Mrad(Si)). The test scheme introduced in this paper could inspect not only the performance degradation of control circuitries in a SRAM circuit, but also the degradation of SRAM cells and sense amplifiers. Thus it can be considered as a worst-case test scheme for deep-submicron SRAM circuits.

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