Investigation of the polysilicon p–i–n diode and diode string as a process compatible and portable ESD protection device

Jiang Yibo(姜一波)†, Du Huan(杜寰), and Han Zhengsheng(韩郑生)

Institute of Microelectronics, Chinese Academy of Sciences, Beijing 100029, China

Abstract: The polysilicon p–i–n diode displays noticeable process compatibility and portability in advanced technologies as an electrostatic-discharge (ESD) protection device. This paper presents the reverse breakdown, current leakage and capacitance characteristics of fabricated polysilicon p–i–n diodes. To evaluate the ESD robustness, the forward and reverse TLP I–V characteristics were measured. The polysilicon p–i–n diode string was also investigated to further reduce capacitance and fulfill the requirements of tunable cut-in or reverse breakdown voltage. Finally, to explain the effects of the device parameters, we analyze and discuss the inherent properties of polysilicon p–i–n diodes.

Key words: polysilicon p–i–n diode; ESD; polysilicon p–i–n diode string
DOI: 10.1088/1674-4926/33/7/074009 **EEACC:** 2570

1. Introduction

With the development of microelectronic technology, ESD (electrostatic-discharge) protection becomes a major issue for the reliability of the continual scaling circuit. In some advanced technologies such as SOI (silicon on insulator) and the III–V compound, the integration of ESD protection is a tough challenge when considering process compatibility and the portability of the ESD protection design. The diode built in polysilicon is fully process compatible with a majority of processes and is partly portable. Besides being attributed to the non-existence of a vertical junction, its capacitance and coupling noise is lower than diodes built in bulk-Si[1−3].

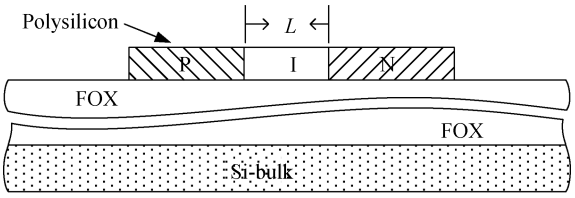
This paper investigates the polysilicon p–i–n diodes and diode strings which were formed by stacking polysilicon p–i–n diodes. The reverse breakdown, leakage current and capacitance characteristics are displayed, and the TLP test system is used to measure their ESD robustness. Additional polysilicon diodes were staked in a cascaded configuration to control capacitance, reverse breakdown voltage or cut-in voltage. In the last section, a comprehensive analysis and discussion present the effects of the device parameters and the inherent properties of the device.

2. The polysilicon p–i–n diode

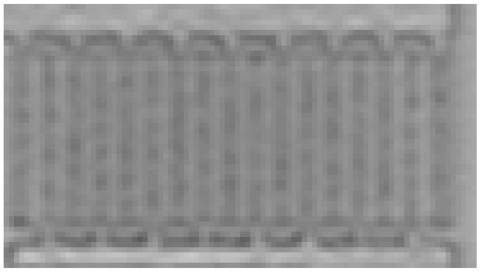
A sketch of the structure and a device photo of a polysilicon p–i–n diode are displayed in Figs. 1(a) and 1(b). The device was fabricated using 0.5 μm HV diffusion processing. Contributing to low capacitance and noise insensitivity, a whole polysilicon layer was disposed over an FOX (field-oxide) layer and fully isolated to Si-bulk. The diode was formed by implanting n-type or p-type impurities into the polysilicon layer. An additional undoped center region, of which length defined as L, was located between the p-type and the n-type regions. L is the most crucial parameter for p–i–n polysilicon diodes, as shown in Fig. 2.

Figure 2 shows the measured results of the fabricated polysilicon p–i–n diode with different L values, which ranged from 0.3 to 1.5 μm. These devices were designed with a large dimension of 1200 μm (1.05×10^{-2} mm^2 for the $L = 0.8$ μm device). When L increased to 1.5 μm, a significant increase in $V_{\rm br}$ (reverse breakdown voltage, which is defined at –10 μA current) from 3.7 V ($L = 0.8$ μm) to 9.5 V ($L = 1.5$ μm) is shown in Fig. 2(a). The forward cut-in voltage varied slightly. Meanwhile, both leakage current (reverse bias voltage was –1 V) and capacitance declined effectively when L increased to 1.5 μm, as shown in Figs. 2(b) and 2(c). The physical mechanisms are further discussed in Section 4.

As an ESD protection device, further investigations about ESD protection performance are displayed in Fig. 3. Figure 3(a) shows the forward TLP I–V characteristics of polysil-



(a)



(b)

Fig. 1. (a) A sketch of the structure and (b) a device photo of a polysilicon p–i–n diode.

† Corresponding author. Email: jybjybjyb@gmail.com
Received 12 December 2011, revised manuscript received 1 February 2012

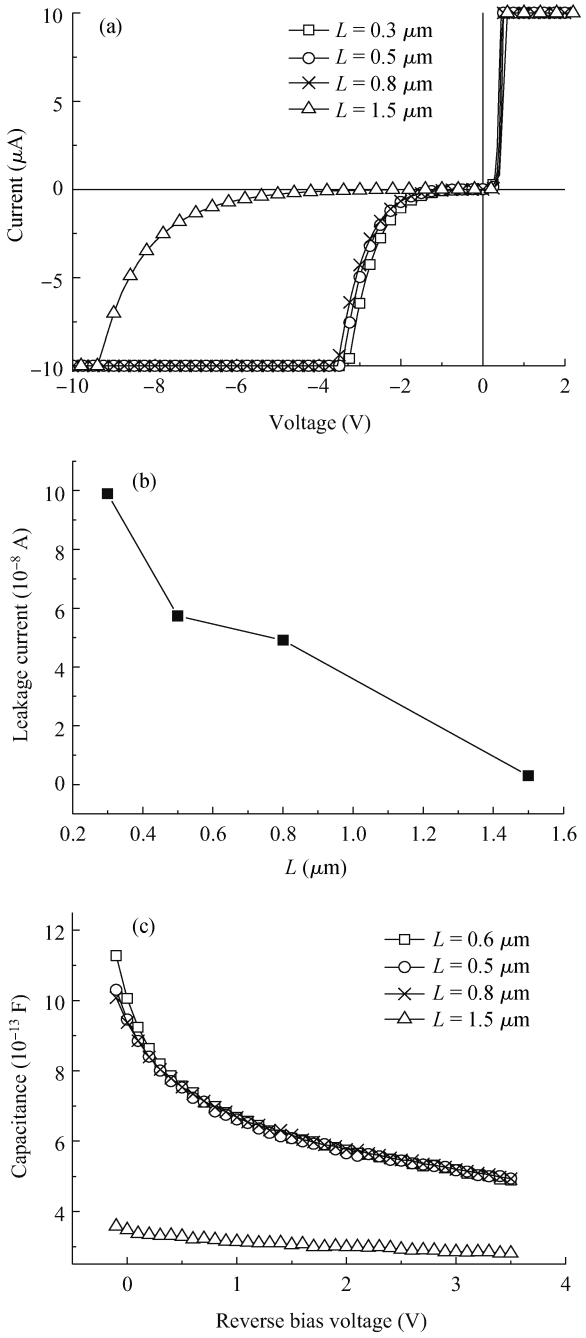


Fig. 2. (a) Reverse breakdown, (b) leakage current and (c) capacitance characteristics of 1200 μm wide polysilicon diodes with different L values.

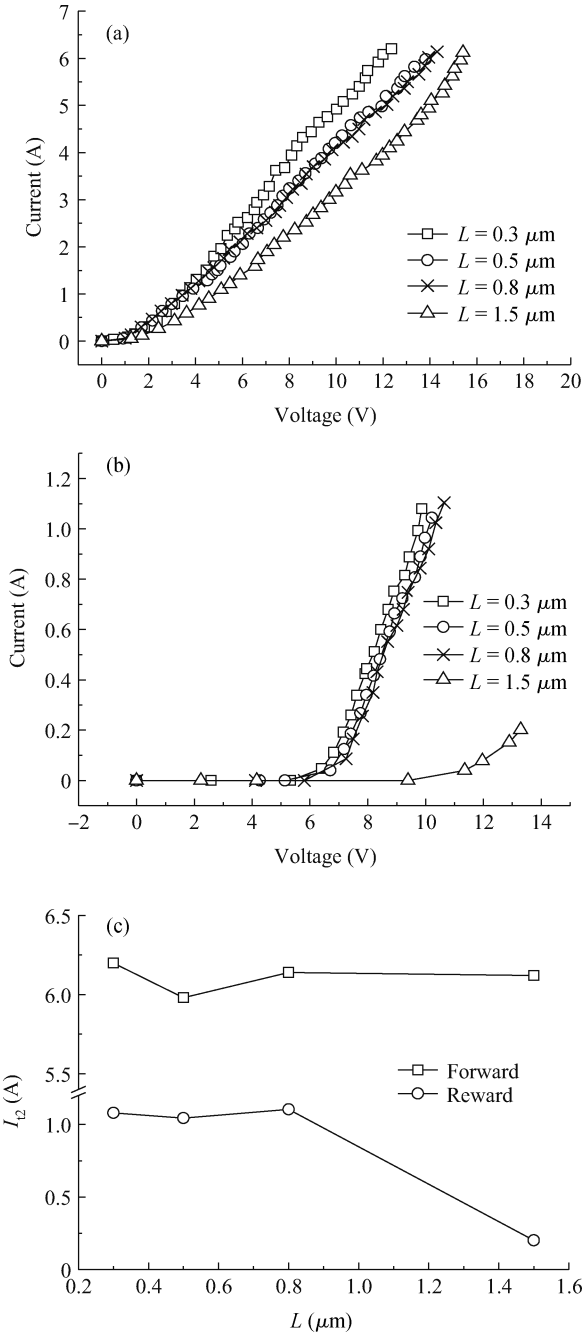


Fig. 3. (a) Forward and (b) reverse TLP I–V characteristics and (c) measured I_{t2} of 1200 μm wide polysilicon diodes with different L values.

icon diodes with different L values (0.3/0.5/0.8/1.5 μm). The second breakdown (or thermal breakdown) current, I_{t2}, determined the ESD robustness. When L increased, the forward I_{t2} stayed around 6.1 A but the forward turn-on resistor increased. In Fig. 3(b) the reverse TLP I–V characteristic revealed that the reverse I_{t2} declined sharply to 0.2 A when L increased to 1.5 μm. Figure 3(c) describes the relationship between L and forward or reverse I_{t2}. It indicates that L, reverse breakdown and capacitance were limited in a narrow range to maintain the ESD protection level.

3. The polysilicon p–i–n diode string

To further reduce capacitance and increase cut-in voltage or V_{br}, polysilicon p–i–n diodes were stacked in a cascaded configuration to form the polysilicon p–i–n diode string. Compared with the bulk-Si device, the polysilicon diode string did not provide vertical junction capacitance and avoided the Darlington effect when excessive diodes were stacked together[4]. Thus the p–i–n diode string built in polysilicon was an appropriate choice when aiming to reduce capacitance, increase cut-in voltage or reverse breakdown voltage. These fabricated devices were designed with a dimension of 150 μm (6.75 $\times$

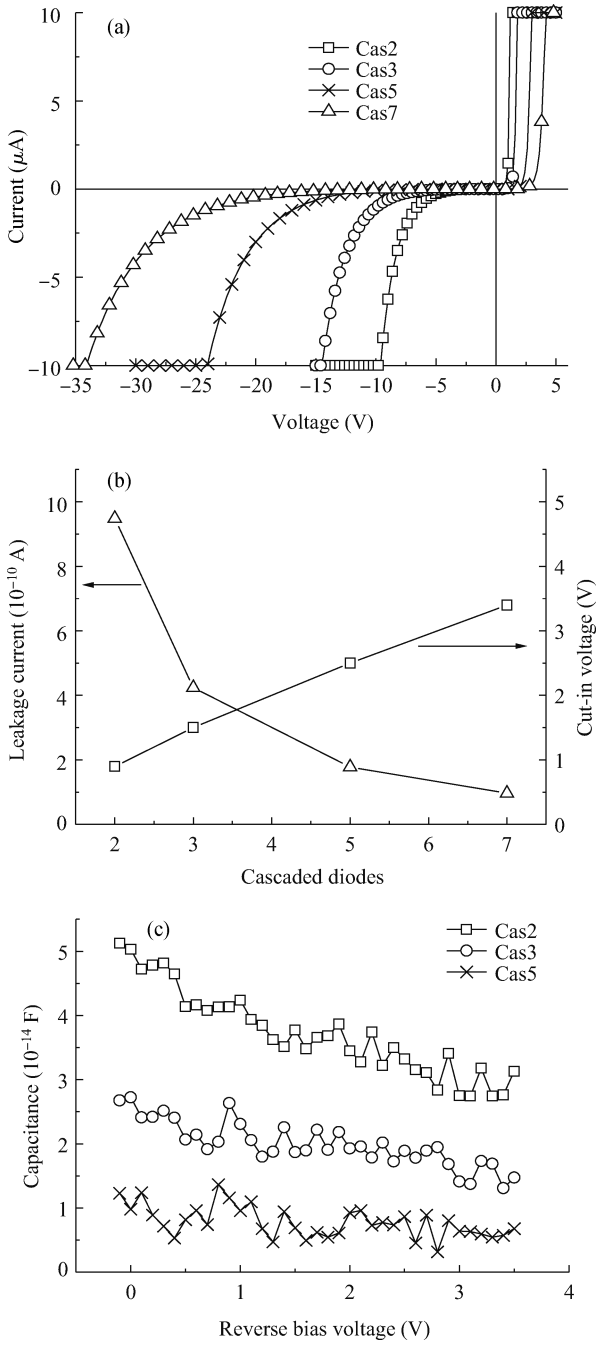


Fig. 4. (a) Reverse breakdown, (b) leakage current and (c) capacitance characteristics of 150 μm wide polysilicon diode strings with different numbers of diodes.

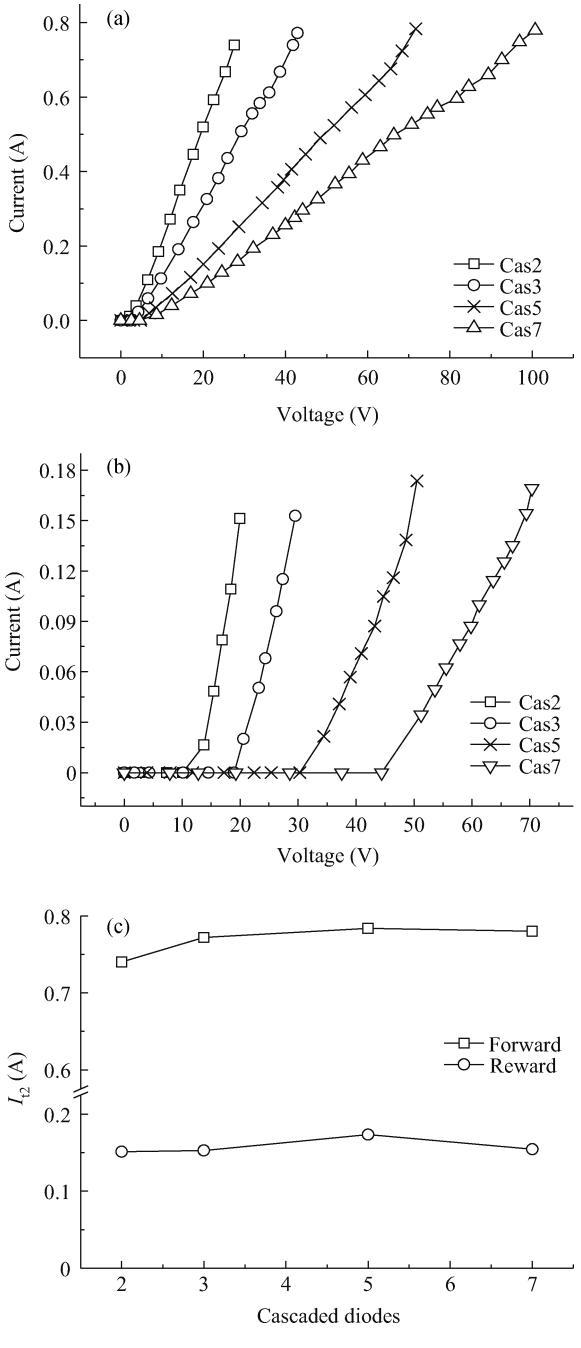


Fig. 5. (a) Forward and (b) reverse TLP I–V characteristics and (c) measured I_{t2} of 150 μm wide polysilicon diode strings with different numbers of diodes.

10^{-3} mm^2 for the diode string cascading three $L = 0.8$ μm diodes). Figure 4 shows the measured results of the polysilicon p–i–n diode ($L = 0.8$ μm) strings formed by 2/3/5/7 diodes (Cas2/Cas3/Cas5/Cas7). Cascading more diodes induced the V_{br} (also defined at –10 μA current) and cut-in voltage increase, as shown in Fig. 4(a). In Fig. 4(b), it is revealed that cut-in voltage increased regularly and leakage current (reverse bias voltage was –1 V) reduced effectually. The dependence of the capacitance on the stacked number of diodes can be seen in Fig. 4(c), which shows that the polysilicon diode string was one solution when designing an ultra-low parasitic capacitance ESD protection device to minimize negative impacts.

Simultaneously, the ESD performance of the polysilicon p–i–n diode string is displayed in Fig. 5, through measuring the TLP I–V characteristic. When more diodes were stacked together, I_{t2} did not decline but the turn-on resistor increased as shown in Fig. 5(a). As Figure 5(b) shows, cascading more diodes induced a significant increase in reverse knee voltage from 12 to 41 V, but a slight variance of I_{t2} in the reverse condition. Figure 5(c) describes the relationship between the counts of stacked diodes and the forward or reverse I_{t2}. The ESD protection device was able to be designed with ultra-low parasitic capacitance and desired cut-in or V_{br}, while maintaining a high ESD protection level throughout the stacking polysili-

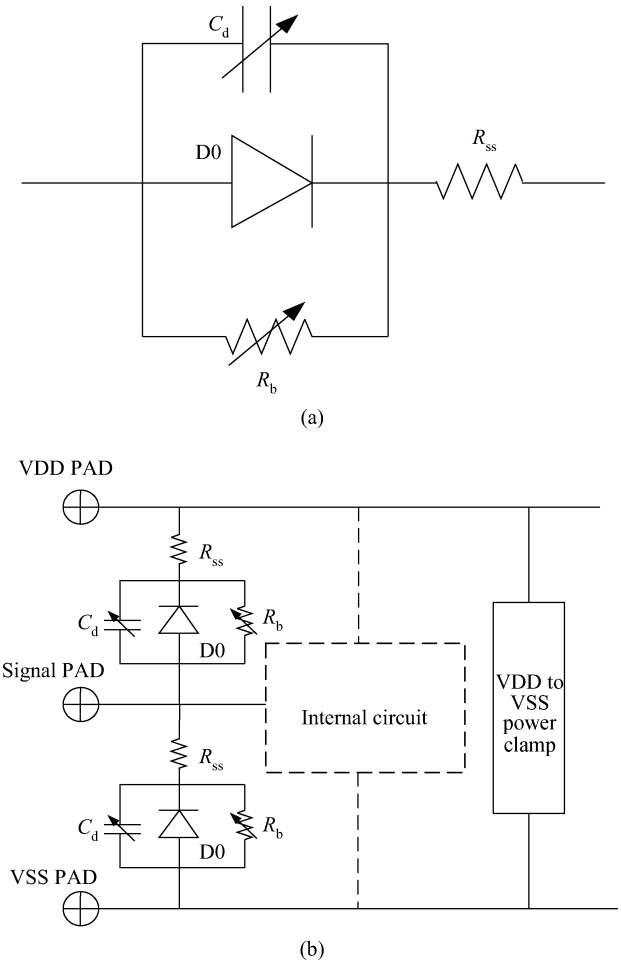


Fig. 6. Schematics of (a) the equivalent circuit of a polysilicon p–i–n diode and (b) the ESD protection design with polysilicon p–i–n diodes.

con diodes in a cascaded configuration.

4. Analysis and discussion

In this section we comprehensively analyze and discuss the polysilicon p–i–n diodes. In order to reveal the effects of L and the inherent properties of the device, an equivalent circuit was proposed, as shown in Fig. 6(a). D0 was assumed as a diode without an I region, but its V_{br} was regulated by L. The polysilicon boundary-induced resistor was defined as R_b, which induced non-ignorable leakage current[5]. C_d was polysilicon p–i–n diode capacitance, which depended strongly upon L, and series R_{ss} was parasitical resistance. A schematic of the general full-chip ESD protection design[6] with polysilicon p–i–n diodes is displayed in Fig. 6(b). It indicates that these reverse diodes were the primary source for ESD protection-induced signal noise and loading capacitance for the internal circuit.

The charge and electric field distribution of a polysilicon p–i–n diode is displayed in Fig. 7. N_a and N_d are the acceptor and donor concentrations, respectively. According to Poisson's equation and boundary conditions, it gets

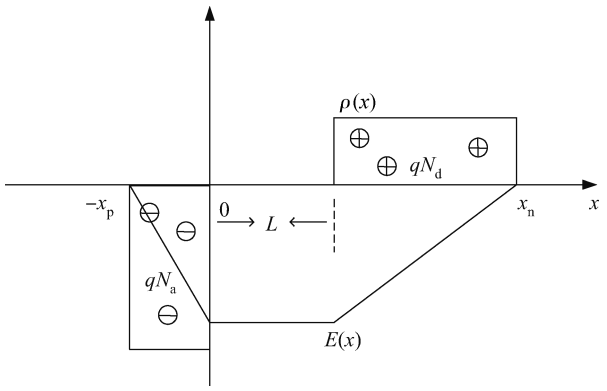


Fig. 7. The charge and electric field distribution of a polysilicon p–i–n diode.

$$E_m = \frac{qN_a x_p}{\varepsilon_{si}} = \frac{qN_d(x_n - L)}{\varepsilon_{si}}, \tag{1}$$

$$\Psi_t = \frac{E_m(W_d + L)}{2}, \tag{2}$$

where E_m and Ψ_t are the maximum electric field and total potential drop, respectively, ε_{si} is the silicon dielectric constant, $W_d = x_p + x_n$ is the total depletion layer width, and

$$W_d = \sqrt{\frac{2\varepsilon_{si}(N_a + N_d)\Psi_t}{qN_aN_d} + L^2}, \tag{3}$$

$$\Psi_t = \Psi_{bi} - V_{bias}, \tag{4}$$

where Ψ_{bi} and V_{bias} are the build-in and external bias voltage, respectively. Assuming that the diodes with and without the I region had the same total potential drop, we get

$$E_{m0} = \frac{2\Psi_{t0}}{W_{d0}}, \tag{5}$$

$$E_m = \frac{2\Psi_t}{W_d + L}, \tag{6}$$

where Ψ_{t0}, W_{d0} and E_{m0} are the total potential drop, depletion layer width and maximum electric field of the diode without I region, respectively. According to the avalanche breakdown mechanism, breakdown occurred once the maximum electric field exceeded the critical electric field, which approximated to constant in silicon[7]. Assuming $E_m = E_{m0}$, we got

$$\frac{2\Psi_{t0}}{W_{d0}} = \frac{2\Psi_t}{W_d + L}, \tag{7}$$

$$\frac{\Psi_{bi} - V_{br0}}{\sqrt{\dfrac{2\varepsilon_{si}(N_a + N_d)(\Psi_{bi} - V_{br0})}{qN_aN_d}}} = \frac{\Psi_{bi} - V_{br}}{\sqrt{\dfrac{2\varepsilon_{si}(N_a + N_d)(\Psi_{bi} - V_{br})}{qN_aN_d} + L^2} + L}, \tag{8}$$

$$V_{br} = V_{br0} - 2L\sqrt{\frac{(\Psi_{bi} - V_{br0})qN_aN_d}{2\varepsilon_{si}(N_a + N_d)}}, \tag{9}$$

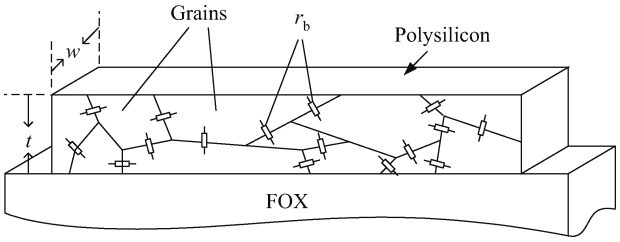


Fig. 8. Schematic of polysilicon grain boundary-induced resistance in poly-Si.

where V_{br0} ($V_{br0} < 0$) is the reverse breakdown voltage of the diode without I region. This indicates that increasing L effectively raises the reverse breakdown voltage ($V_{br} < 0$). As a parallel plate capacitor, the capacitance of the p–i–n diode (C_d) is

$$C_d = \frac{A\varepsilon_{si}}{W_d}, \tag{10}$$

$$C_d = C_0 \frac{W_{d0}}{W_d}, \tag{11}$$

$$C_d = C_0 / \sqrt{1 + \frac{L^2 q N_a N_d (\Psi_{bi} - V_{bias})}{2\varepsilon_{si}(N_a + N_d)}}, \tag{12}$$

where A is the junction area. Increasing the reverse bias voltage or L induces a C_d decline because of the wider W_d. This is accordant with the measured results above.

Moreover, some specific properties of this device which were manufactured in the polysilicon layer were considerable. Figure 8 displays a schematic of a polysilicon grain, which induces the grain boundary resistance R_b. It is assumed that the highest leakage current in the polysilicon diode originated from the paralleled polysilicon resistance R_b, which is expressed as

$$R_b = \frac{W_d r_b}{wtsn}, \tag{13}$$

$$R_b = \frac{r_b}{wtsn} \sqrt{\frac{2\varepsilon_{si}(N_a + N_d)(\Psi_{bi} - V_{bias})}{qN_a N_d} + L^2}, \tag{14}$$

where w and t are the width and thickness of the depletion layer, respectively. r_b is the resistance of a single grain boundary per grain interface area, s is the mean grain size, and n is the number of carriers. When a –1 V reverse bias voltage is applied on the device, R_b induces a high leakage current through the polysilicon diode, as shown in the aforementioned experiments.

5. Conclusions

In this paper, a polysilicon p–i–n diode and diode string were investigated to fulfill the process compatibility requirements of ESD protection devices in advanced technologies. The relationship between the I region width, L, and the device characteristics were revealed, and the physical mechanisms of the device were discussed comprehensively. In order to fulfill the desired cut-in or reverse breakdown voltage and the requirement of ultra-low capacitance, investigations into polysilicon p–i–n diode string were also performed.

References

[1] Richier C, Salome P, Mabboux G, et al. Investigation on different ESD protection strategies devoted to 3.3 V RF applications (2 GHz) in a 0.18 μm CMOS process. Electrical Overstress/Electrostatic Discharge Symposium Proceedings, 2000

[2] Ker M D, Chen S L. On-chip high-voltage charge pump circuit in standard CMOS processes with polysilicon diodes. Asian Solid-State Circuits Conference, 2005

[3] Ker M D, Chang C Y, Jiang H C. Design of negative charge pump circuit with polysilicon diodes in a 0.25 μm CMOS process. Proceedings IEEE Asia-Pacific Conference on ASIC, 2002

[4] Wang A Z H. On-chip ESD protection for integrated circuits: an IC design perspective. New York: Kluwer Academic Publishers, 2002

[5] Thewes R, Brederlow R, Dahl C. Explanation and quantitative model for the matching behavior of poly-silicon resistors. International Electron Devices Meeting Technical Digest, 1998

[6] Ker M D, Wang C T. Design of high-voltage-tolerant ESD protection circuit in low-voltage CMOS processes. IEEE Trans Device Mater Reliab, 2009, 9(1): 49

[7] Sze S M. Physicals of semiconductor devices. New York: John Wiley & Sons, Inc, 1981