A fourth-order bandwidth-reconfigurable delta–sigma modulator for audio applications*

Wang Junqian(王俊乾)[1], Yang Haifeng(杨海峰)[1], Wei Rui(魏蕊)[1], Xu Jun(许俊)[1,†], and Ren Junyan(任俊彦)[1,2]

[1]State Key Laboratory of ASIC & System, Fudan University, Shanghai 201203, China
[2]Microelectronics Science and Technology Innovation Platform, Fudan University, Shanghai 201203, China

Abstract: A single loop fourth-order delta–sigma modulator is presented for audio applications. A reconfigurable mechanism is adopted for two bandwidth-based modes (8 kHz/16 kHz). Manufactured in the SMIC 0.13 μm CMOS mixed signal process, the chip consumes low power (153.6 μW) and occupies a core area of 0.98×0.46 mm^2. The presented modulator achieves an 89.3 dB SNR and 90.2 dB dynamic range in 16 kHz mode, as well as a 90.2 dB SNR and 86 dB dynamic range in 8 kHz mode. The designed modulator shows a very competitive figure of merit among state-of-the-art low voltage modulators.

Key words: delta–sigma modulator; feedforward architecture; reconfiguration; switched capacitor; bootstrapped switch

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1. Introduction

In recent years, the ever demanding electronic portable systems market, e.g. personal digital media, cellular phones and medical electronic devices, have been proposing more stringent requirements for kernel circuitry components. With a scaling down of feature size, the CMOS technology process requires a corresponding reduction in power supply, which poses a great challenge for system configuration and circuitry design techniques.

Analog-to-digital converters (ADCs) usually play a significant role as the interface in audio-visual and communication systems. With the systems ceaselessly enhancing their capability, the speed and accuracy of ADCs must follow in their footstep to improve overall performance.

Trading off speed and resolution, the delta–sigma converter has been a favorable candidate among various ADCs in recent years to meet the increasingly stringent specifications in VLSI systems. Different from the Nyquist converter, the delta–sigma ADC is characterized by two key techniques known as over-sampling and noise shaping. These are adopted in measuring instruments and audio application fields such as the VOIP system to provide signal transmission with higher sound quality.

Since the voice band ranges from 0.2 to 8 kHz, general hearing aids require a signal bandwidth up to 8 kHz. But to satisfy the specification of high-end hearing aids, a signal bandwidth up to 16 kHz needs to be processed to ensure sound quality with high fidelity.

In this paper, a reconfigurable mechanism for 8 kHz and 16 kHz modes is proposed, aiming at different applications. We present a single loop fourth-order SDM with feedforward architecture. Due to reduced voltage swing at inner nodes of the loop filter, the linearity requirement of OTAs is relieved. Moreover, two stage OTAs with class AB topology are used to optimize power consumption. The single bit quantizer and the single bit feedback DAC are designed to be oriented towards a low power contribution to the overall modulator.

2. Architectural design

In this section, the architectural design and other relevant considerations will be discussed for low power optimization. Firstly, the choice of modulator topology is explained through comparing structures and quantization implementations. Later, the stability issue is analyzed, and finally signal scaling is considered for relaxing the requirements of OTAs.

2.1. Modulator topology

There are several factors for consideration when designing a delta–sigma modulator, including the order, the oversampling ratio, the loop structure and the quantization bit.

A single loop is employed compared with the cascaded structure because the noise leakage of the MASH loop due to mismatch between analogue and digital components causes serious degradation of modulator performance.

Feedforward architecture has become a good candidate in recent years because the signal component appearing at the inner nodes of the loop filter is much smaller than that in feedback architecture, which greatly relaxes the linearity requirement of OTAs[1]. To strengthen noise suppression in the baseband, a local feedback loop around the two integrators is added to form a resonator[2]. However, the resonator adds extra load to the OTA and makes the design more complicated.

The multibit quantizer has become popular in recent years

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† Corresponding author. Email: jxu@fudan.edu.cn
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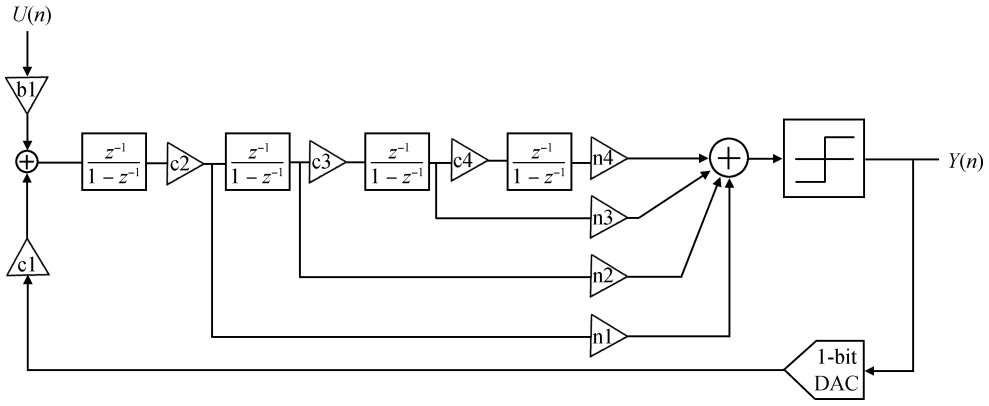

Fig. 1. Single loop fourth-order topology.

because of greater suppression of quantization noise and hence better SNR. But the comparator group is not power efficient and requires an additional calibration technique, e.g. dynamic element match (DEM) to improve feedback DAC linearity. Therefore, a single-bit quantizer is adopted because of its simplicity and high linearity.

In order to achieve an aggressive noise shaping dynamic for the specified high resolution, we choose a fourth-order modulator with a 128× oversampling ratio after extensive behavioral simulations. Figure 1 depicts the designed single loop fourth-order modulator topology.

2.2. Stability issue

As the delta–sigma modulator is a feedback system, stability is of great concern to ensure convergency operation. The loop order and out-of-band peak gain of NTF (H_inf) have a large influence on the stability of the overall system. For single bit quantization, H_inf = 1.5 is chosen to ensure stability[3]. As analyzed in Ref. [1], the parasitic capacitor at the input node of the comparator, combined with the switch, stores the feedforward charge and forms the parasitic fifth integrator. Thanks to the additional integrator, the attenuation of the quantization noise in the signal band is slightly increased, and the noise shaping dynamic is reinforced.

However, due to the parasitic integrator, the extra zero of the NTF moves to the right on the real axis as the parasitic capacitance increases, causing H_inf to be more than 1.5 and resulting in instability. An oversized capacitor should thus be avoided in the design process. In our design, total capacitance is only a few tens of fF, which poses no threat to stability.

2.3. Output swings of integrators

As noted previously, the feedforward structure has the advantage of low voltage swing at inner nodes. A behavioral simulation is performed to show the integrator output swings, as in Fig. 2. Through coefficient scaling, the output swing of each integrator is limited within 30% to the reference voltage, which relieves the linearity requirement of OTAs.

3. Circuit implementation

The key analog blocks in the modulator are introduced in this section, including OTAs, a comparator, and a DAC. The design issues are analyzed and discussed subsequently.

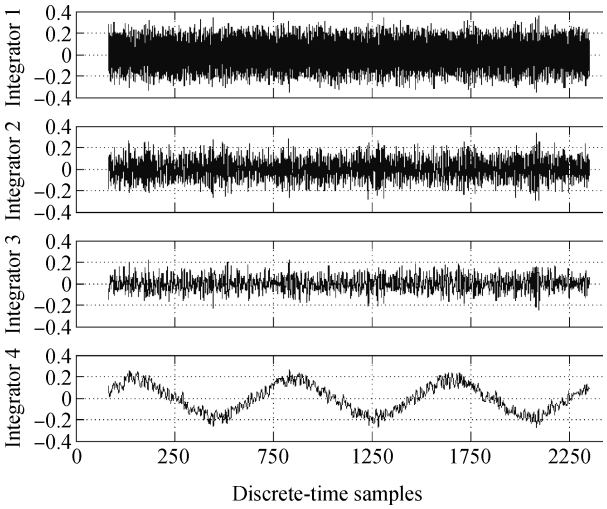

Fig. 2. The output swings of the respective integrators.

3.1. Low power and high performance OTA

In a delta–sigma modulator for high resolution and low power, the operational transconductance amplifier (OTA) is the most critical building block since it has a dominant impact on the performance of the entire modulator.

Gain leakage, nonlinear gain effect and limited slew rate are the three major sources that determine OTA performance.

Finite gain will cause integrator leakage and influence settling accuracy. As analyzed in Ref. [4], the DC gain of the OTA varies with its output nonlinearly, which will result in distortion and deteriorate the performance. To relieve this effect, the output swing is scaled to a small range, as explained in Section 2.2. Slew rate is the source to influence settling speed. A sweep simulation shows that slew rate more than 5 V/μs constitutes no threat to the modulator.

A folded cascode OTA is adopted in Ref. [5] to achieve a high dc gain. However, it is not suitable for low voltage designs. A class A amplifier is used in Ref. [4], but it features a low slew rate (SR) given a certain amount of static current.

An OTA topology based on that in Ref. [6] is adopted in this work, as illustrated in Fig. 3, using a large PMOS input pair

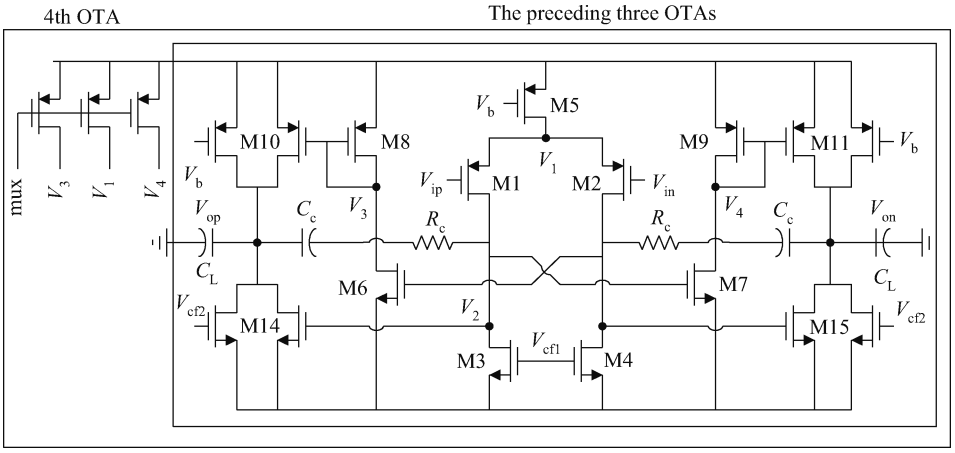

Fig. 3. The structure of OTAs.

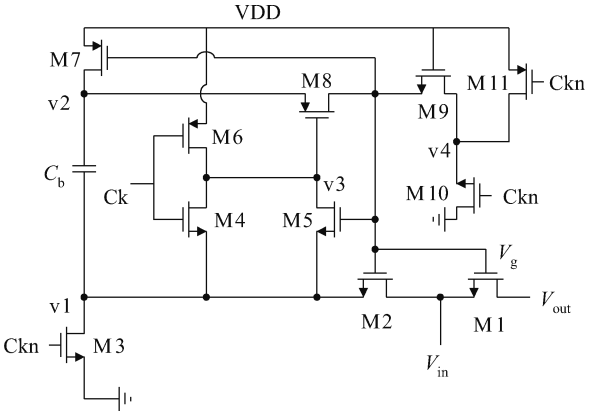

Fig. 4. A bootstrapped switch

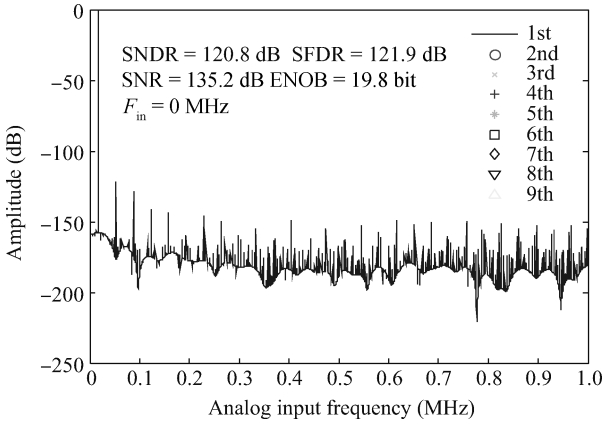

Fig. 5. The FFT simulation result of bootstrapped switch.

to suppress flicker noise for the first stage and a class AB second stage, as can be seen in Ref. [7]. A compensation capacitor (C_c) is bridged between the two stages to split two poles, while a series resistor (R_c) is inserted to avoid a right half-plane zero.

3.2. High linearity sampling switch

Due to the stringent requirement of the first integrator, a high linearity of the sampling switch is required. Since the on-resistor of NMOS switch changes with input signal, the bootstrap technique is adopted to ensure a constant on-resistor[8],which is depicted in Fig. 4.

FFT simulation indicates in Fig. 5 that when applied an input signal of 17 kHz sampled at 4 MHz, the output spectrum reaches 135.2 dB SNR, 120.8 dB SNDR and 19.8 bit ENOB.

Due to the fixed voltage of the feedback signal V_{ref+} and V_{ref-}, a generic switch using CMOS transistors suffices for linearity.

3.3. The adder

In front of the quantizer, a summation circuit is needed to add integrator outputs. A switched capacitor topology based on current mirror is chosen in Ref. [5], while an active adder made of an opamp and resistors is proposed in Ref. [9]. Both of them consume quiescent current. For low power consideration, an adder composed of all switched capacitors is adopted by Ref. [1]. It features simplicity and power efficiency.

Figure 6 shows the topology of the adder where it samples the output voltage of each integrator during CK1 and performs a summing operation during the CK2 phase.

3.4. The quantizer

As mentioned in Section 2, single bit quantization is adopted for high linearity, and the dynamic requirement of the comparator is alleviated since its nonidealities such as offset, metastability and hysteresis are noise shaped. The comparator adopted in Ref. [10] is comprised of a preamplifier, a regenerative latch and an SR latch. The analog preamplifier is separated from the dynamic latch to reduce kickback noise. However, the analog preamplifier flows quiescent current, which is not expected in our low power design.

Based on the structure in Ref. [11], a schematic of the comparator employed is shown in Fig. 7, in which transistors M2, M3, M8 and M9 constitute two positive feedback loops, providing fast comparison speeds. When CK gets low, the comparator is in reset mode. The output is shorted to the supply voltage and the regeneration loop is broken off. When CK gets high, the voltage difference between the two inputs is reinforced by the regenerative latch, driving two outputs to com-

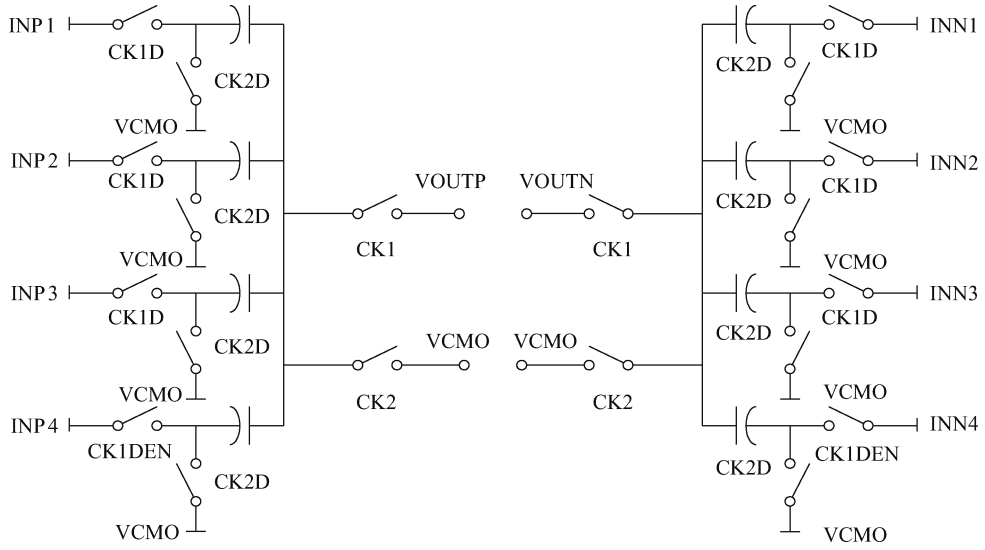

Fig. 6. The topology of the adder with switched capacitors.

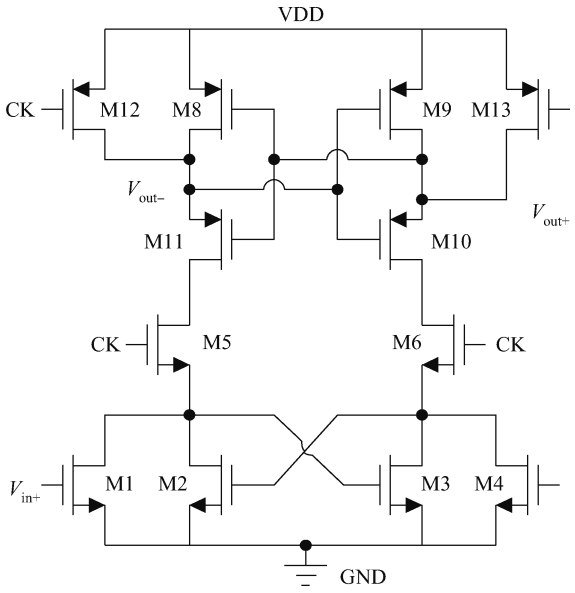

Fig. 7. A schematic of the comparator.

plementary supply voltages.

3.5. Overall modulator implementation

3.5.1. Mode reconfiguration

As Figure 8 shows, the overall modulator is composed of a fourth-order loop filter, an adder, a quantizer and a feedback DAC. In order to implement between two modes, a control signal (mux) is used to reconfigure the modulator. In the summation circuit, the output of the fourth integrator is controlled by the signal ck1den (= mux & ck1d). When the mux gets high, the fourth OTA operates and the adder performs a summation with the fourth integrator output, which leads to a fourth-order noise-shaping in the application of the 16 kHz mode. When the mux gets low, the modulator degenerates into a third-order dynamic with the fourth OTA shut off, which results in a power saving for the 8 kHz mode. Figure 3 also illustrates the fourth OTA with additional control signals. When mux gets low, the M5, M8, M9, M10, M11 transistors are shut off and the V1, V2, V3 nodes are at a high level, resulting in no static current in both stages.

3.5.2. Noise budget

The modulator is implemented by switched capacitors for discrete time operation. The first stage contributes most of the thermal noise to the modulator. The SNR determined by the first integrator thermal noise is expressed in Eq. (1):

$$\mathrm{SNR}_{KT/C} = \frac{V_{\mathrm{sw}}^2 C_{\mathrm{S}} \cdot \mathrm{OSR}}{2 \times 4KT}, \tag{1}$$

where V_{sw} denotes the voltage swing and OSR refers to the oversampling ratio. To achieve an SNR of more than 98 dB for 16 bit resolution, we choose a sampling capacitor of 3.4 pF for reliability. As the sampling noise from other integrators is at least second-order noise shaped, it has a rather small influence on the modulator. Therefore the sampling capacitors of other integrators are progressively downsized for power saving.

4. Experimental results

A discrete-time delta–sigma modulator was designed in SMIC 0.13 μm mixed signal CMOS technology. Figure 9 shows a fabricated chip with the test board, of which the core occupies an active area of 0.98×0.46 mm^2.

Both modes are measured for comparison. In 16 kHz mode, sinusoidal input signals with a peak amplitude differential of 1.76 V are supplied to the converter. The captured output bitstream sized 8192 points are processed by a Hanning window and a Fourier transformation is applied. The spectral can be observed in Fig. 10. The peak SNR measures 89.3 dB when the differential input signal is 1.24 V. Figure 12 presents the SNR versus signal amplitude. The dynamic range is 90.2 dB.

In 8 kHz mode, sinusoidal input signals with a peak amplitude differential of 1.63 V are provided to the ADC. Power spectral density (PSD) is plotted in Fig. 11. We can see from the spectrum that the SNR measures 90.2 dB to the maximum

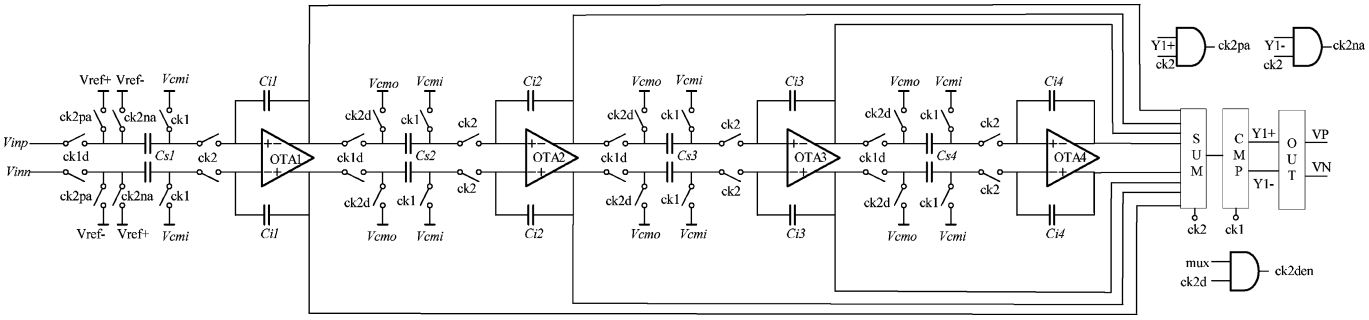

Fig. 8. Schematic of the overall modulator.

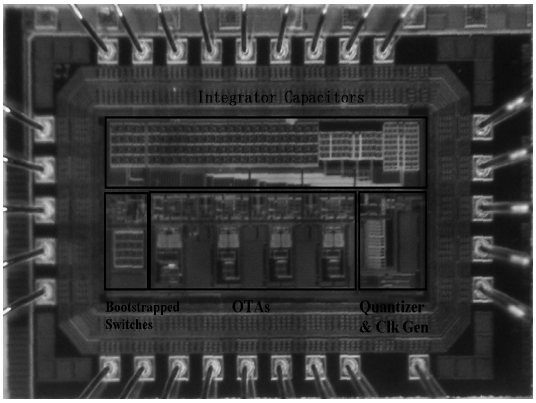

Fig. 9. The modulator chip.

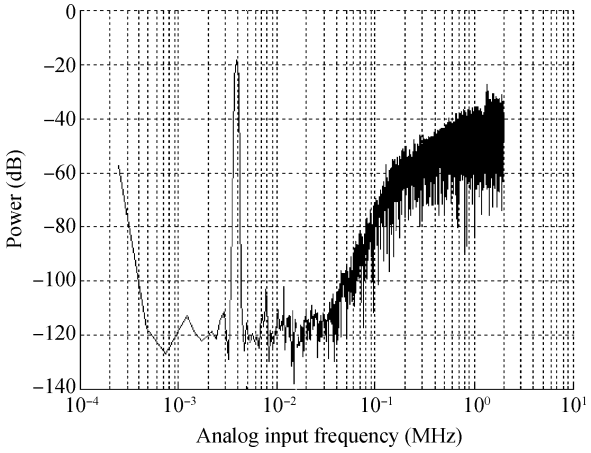

Fig. 10. The measured spectrum in 16 kHz mode.

when the input differential signal is 1.34 Vpp and the dynamic range reaches 86 dB.

A summary, in the form of Table 1, is given to summarize the performance of the modulator. The figure of merit (FOM) is defined as:

$$\mathrm{FOM} = \frac{P}{2 \times f_{\mathrm{B}} \times 2^{(\mathrm{DR}-1.76)/6.02}}, \qquad (2)$$

in which P, f_{B} and DR denote the power dissipation, signal bandwidth and dynamic range, respectively.

Table 1. Performance summary of the modulator.

Parameter	Value	
Signal bandwidth (kHz)	16	8
Clock frequency (MHz)	4.096	2.048
Technology	SMIC mixed-signal	0.13 μm
Supply voltage (V)	1	1
Power consumption (μW)	153.6	131.4
Active area (mm^2)	0.98×0.46	
SNR/DR (dB)	89.3/90.2	90.2/86
FOM (pJ/level)	0.1815	0.5036

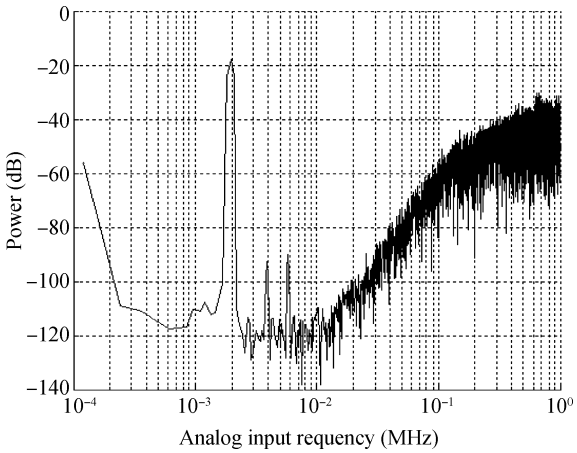

Fig. 11. The measured spectrum in 8 kHz mode.

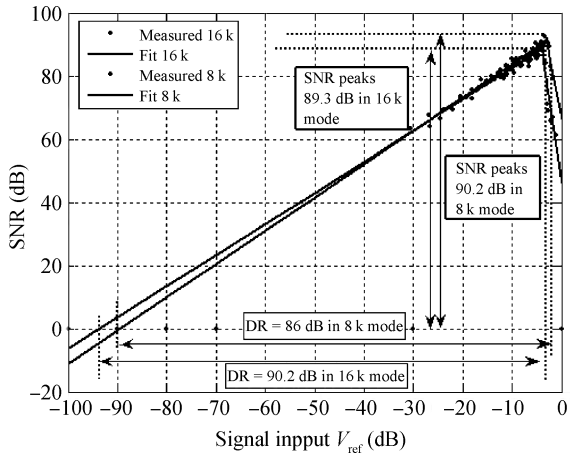

Fig. 12. SNR versus signal amplitude.

Table 2. Performance comparison of low voltage modulators.

Parameter	Process (μm)	SNR (dB)	Signal Bandwidth (kHz)	Power Dissipation (μW)	Supply Voltage (V)	FOM (pJ)
Ref. [2] (2010)	0.25	89	20	457	1.5	0.49
Ref. [12] (2011)	0.18	70.2	10	60	0.9	1.13
Ref. [13] (2004)	0.09	88	20	140	0.9	0.17
Ref. [14] (2007)	0.18	74	25	300	0.5	0.732
This work (16kHz)	0.13	89.3	16	153.6	1	0.182
(8kHz)	0.13	90.2	8	131.4	1	0.504

5. Conclusion

The DT delta–sigma modulator presented in this paper features low voltage and low power for audio applications. A fourth-order single loop filter with feedforward architecture is implemented in switched capacitors.

A reconfiguration mechanism is proposed in this work to accommodate the different input modes. In order to achieve low FOM, a low power design is carried out throughout the design procedure. The prototype was fabricated in SMIC mixed-signal 0.13 μm technology and the test results show that an 89.3 dB SNR and a 90.2 dB DR are measured in 16 kHz mode, while a 90.2 dB SNR and an 86 dB DR are obtained in 8 kHz mode. The chip occupies a small area of 0.98×0.46 mm^2. When operated in 8k mode, the core dissipates 131.4 μW, saving 14.45% power compared with that in the 16 k mode.

A performance comparison between our modulator and that of the other state-of-the-art modulators is summarized in Table 2. The presented modulator shows a rather low FOM value, which can be explained by several reasons. The power efficiency of OTA circuits benefit from low voltage swings of the modulator with feedforward architecture, and another reason comes from the simplicity of other circuit blocks requiring no quiescent current.

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