Hot-carrier reliability in OPTVLD-LDMOS*

Cheng Junji(程骏骥)† and Chen Xingbi(陈星弼)

State Key Laboratory of Electronic Thin Films and Integrated Devices of China, University of Electronic Science and Technology of China, Chengdu 610054, China

Abstract: An improved structure that eliminates hot-carrier effects (HCE) in optimum variation lateral doping (OPTVLD) LDMOS is proposed. A formula is proposed showing that the surface electric field intensity of the conventional structure is strong enough to make a hot-carrier injected into oxide. However, the proposed structure effectively reduces the maximum surface electric field from 268 to 100 kV/cm and can be realized without changing any process, and thereby reduces HCE significantly.

Key words: hot-carrier effects; OPTVLD LDMOS; surface electric field intensity
DOI: 10.1088/1674-4926/33/6/064003 **PACC:** 7300; 7200

1. Introduction

It has been proposed in Refs. [1–3] that the technique of OPTVLD can be used to improve the trade-off between breakdown voltage and on-resistance in LDMOS by conventional CMOS technology, and accordingly makes smart power ICs (SPICs) better and cheaper. However, in the case of increasing reverse bias in an OPTVLD-LDMOS, a high surface electric field would occur. It may cause the HCE, which seriously decreases the reliability of devices[4−8]. As SPIC is widely used in the high-tech fields of spaceflight, military affairs, *etc.* at present, it is desirable to explore power devices with not only better electrical performance but also higher reliability. Therefore the study of hot-carrier reliability in OPTVLD-LDMOS is very important and urgently needed. However, so far there are no papers published on this problem.

In this paper, the probability of hot-carrier injection is analyzed in detail. Then, an improved OPTVLD-LDMOS which uses variation lateral doping in the p-top layer without adding or modifying the process is proposed. According to the simulation by MEDICI TCAD, the proposed structure effectively reduces the maximum surface electric field and thus significantly suppresses hot-carrier effects.

2. Structure and analysis

A conventional OPTVLD-LDMOS is illustrated in Fig. 1. The idea of optimum VLD is realized mainly through a variation on a lateral doped p-bury layer, which makes the effective acceptor dose of the surface voltage-sustaining region vary with the demanding profile[6, 9].

The process starts from an n-epitaxial wafer, whose orientation is <100>, the impurity is phosphorus and the resistivity is 30 Ω·cm.

Table 1 lists the parameters of the key implantation processes which contribute to generating p-top, p-bury and n-well layers.

Due to the uniform doping of the p-top layer, there are two areas (A and B shown in Fig. 1) containing the peaks of surface electric field when the highest reverse bias (approach breakdown voltage) is applied to the device. Figure 2 shows electric field distribution on the surface of the semiconductor.

The maximum surface electric field intensities of A ($|E|_{\mathrm{Amax}}$) and B ($|E|_{\mathrm{Bmax}}$) are 268 and 120 kV/cm, respectively. Although such a strong electric field would cause hot-carriers, the problem is whether those hot-carriers have enough energy for injection into oxide. In order to answer this question, we need to derive the relationship between surface electric field intensity and hot-carrier injection density.

It is known that the effective temperature T_{e} of a hot-carrier can be expressed as[10]:

$$T_{\mathrm{e}} = \frac{8q^2\lambda^2\,|E|^2}{9\pi m_{\mathrm{n}}^* k_0\,(v_{\mathrm{d}})^2}, \quad |E| \geqslant 20\,\mathrm{kV/cm}, \tag{1}$$

where k_0 and q have the conventional meanings, m_{n}^* is the electron effective mass, λ is the hot-electron mean free path, v_{d} is the saturated electron drift speed, and $|E|$ is the surface electric field intensity.

According to the theory of electron motion, the distance

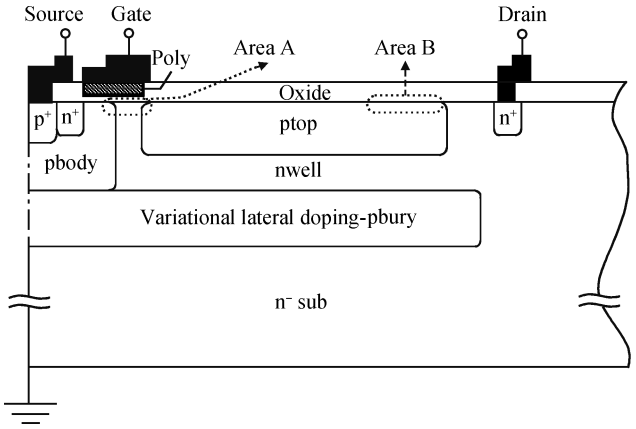

Fig. 1. Conventional structure of OPTVLD-LDMOS.

* Project supported by the PhD Program Foundation of the Ministry of Education of China (No. 20110185110003).
† Corresponding author. Email: chengjunji2005@126.com
Received 15 December 2011, revised manuscript received 20 January 2012

Table 1. Key implantation parameters.

Mask name	Impurity	Dose (10^{12} cm^{-2})	Energy (keV)	Title (°)
p-bury	Boron	6.0	160	0
n-well	Phosphorus	3.7	330	7
p-top	Boron	2.9	160	7

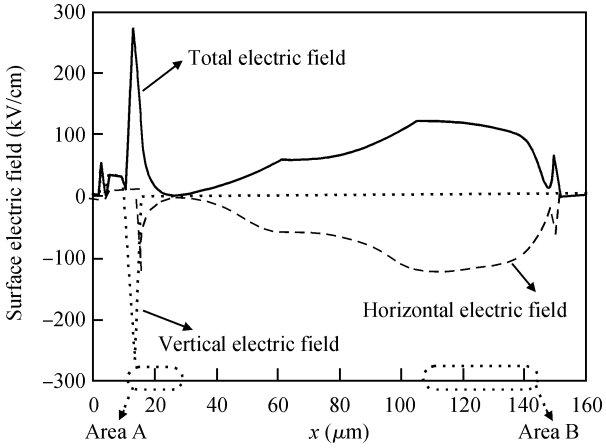

Fig. 2. Surface electric field distribution of a conventional structure (x is the horizontal distance from the source electrode shown in Fig. 1).

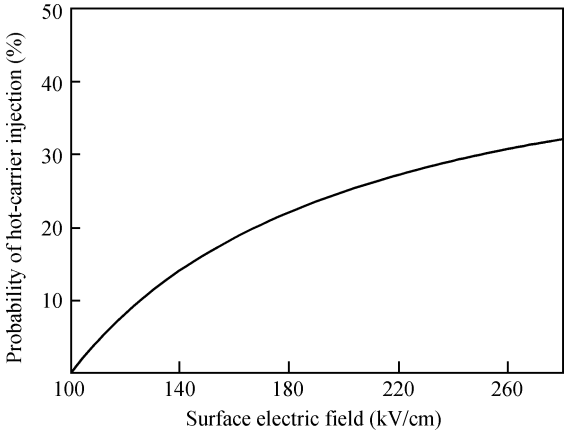

Fig. 3. Probability of hot-carrier injection varies with surface electric field.

that an electron moves between two scatterings is constant no matter whether the electron is energetic or not. In other words, λ is approximately the same as the electron mean free path λ_0 in a condition of thermal equilibrium, namely

$$\lambda \approx \lambda_0 = v_{\rm th}\tau = \frac{\mu_0}{q}\sqrt{3k_0Tm_{\rm n}^*}, \tag{2}$$

where T has the conventional meaning, $v_{\rm th}$ stands for electron speed of random thermal motion, τ stands for mean free time, μ_0 stands for the low-field electron mobility.

Substituting λ from Eq. (2) into Eq. (1), the energy of the hot-electron can be approximately calculated as:

$$E_{\rm h} = k_0T_{\rm e} = \frac{8\mu_0^2|E|^2}{3\pi\,(v_{\rm d})^2}k_0T. \tag{3}$$

In order to compare the strength of the hot-electron energy and the Si/SiO_2 potential barrier, a factor α is introduced which can be expressed as:

$$\alpha = \frac{E_{\rm h}}{\phi_{\rm Si/SiO_2}} = \frac{8\mu_0^2|E|^2}{3\pi\,(v_{\rm d})^2}\frac{k_0T}{\phi_{\rm Si/SiO_2}}, \tag{4}$$

where $\phi_{\rm Si/SiO_2}$ is the Si/SiO_2 potential barrier.

The probability that an electron will acquire enough kinetic energy to surmount the Si/SiO_2 potential barrier, and retain the appropriate momentum after re-direction can be approximately calculated as[11]:

$$p = \frac{1}{2}\left(1-\sqrt{1/\alpha}\right). \tag{5}$$

In the case of $T = 300$ K and surface concentration is approximately 2×10^{16} cm^{-3}, $\mu_0 = 1200$ cm^2/(V·s), $v_{\rm d} = 1\times10^7$ cm/s, $\phi_{\rm Si/SiO_2} = 3.2$ eV[12]. By putting these values of the parameters into Eqs. (4) and (5), we obtain the dependency of that probability on surface electric field which is shown in Fig. 3.

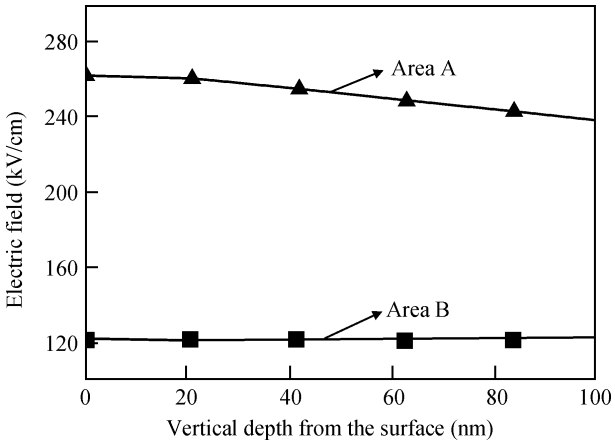

Fig. 4. Electric field versus vertical depth from the surface in areas A and B.

Obviously, in order to effectively suppress the HCE, the surface electric field should be smaller than 100 kV/cm in the case of $T = 300$ K.

In addition, the electric field intensities in areas A and B shown in Fig. 1 remain strong within the 100 nm range of depth as shown in Fig. 4. According to Eq. (2), the hot-electron mean free path $\lambda = 82.35$ nm, therefore it is obvious that there is a wide range of high electric field that injects hot-electrons into oxide and the HCE will inevitably be triggered.

As discussed above, the reason that HCE occurs in the conventional structure is due to too strong surface electric field peaks. Therefore, for the sake of surface electric field optimization, an improved structure is proposed, as depicted in Fig. 5.

The electric field peak in area A can be reduced by a

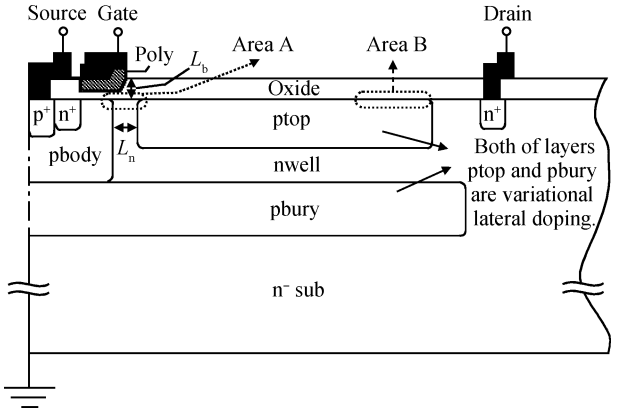

Fig. 5. The proposed structure of OPTVLD-LDMOS.

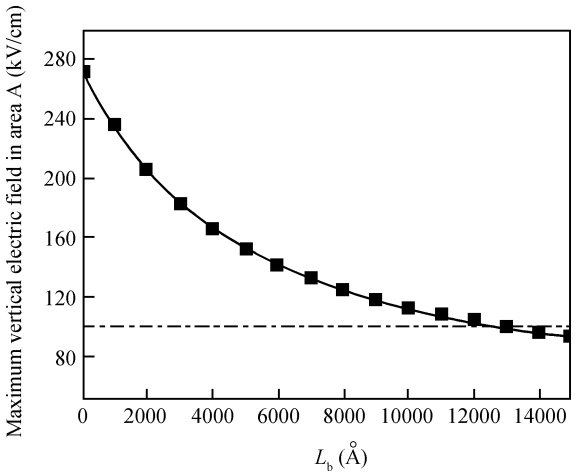

Fig. 6. $|E|_{Avmax}$ as a function of the L_b (L_b is thickness of the beaklike oxide as shown in Fig. 5).

beaklike oxide below the gate poly, and can also be optimized by delicate adjustment of L_n (L_n is shown in Fig. 5). Most distinctively, a variation on the lateral doping of the p-top layer can optimize the horizontal electric field of area B.

3. Results and discussion

In the proposed structure, the thicker the beaklike oxide, the lower the maximum vertical electric field $|E|_{Avmax}$ can achieve. The relationship is illustrated in Fig. 6 when L_n = 4.0 μm.

The positive charges after depletion of n-type Si around area A are determined by L_n. The shorter the L_n, the smaller the positive charges that exist, which is beneficial to the reduction of both the vertical and horizontal surface electric field peaks in area A. However, current density falls simultaneously, and thereby results in an increase of on-resistance. Figure 7 shows that the dependence of the maximum surface electric field intensity in area A and the on-resistance on L_n when L_b = 15000 Å.

As depicted in Fig. 7, maximum horizontal and vertical surface electric field intensities both fall to below 100 kV/cm when L_n is 2.4 μm, while nearly no impact is imposed upon on-resistance ($\Delta R_{on} \approx 1.5\%$).

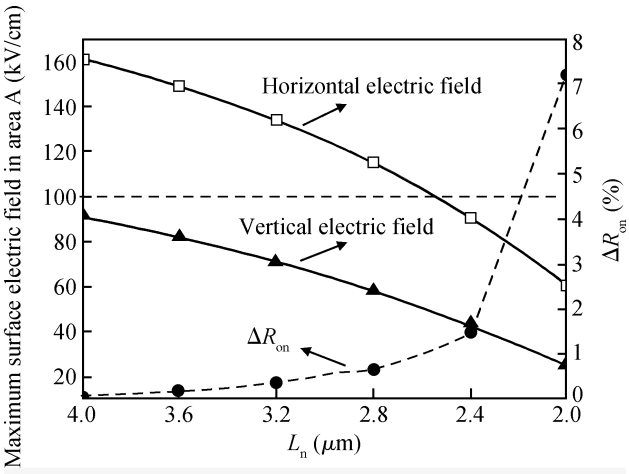

Fig. 7. $|E|_{Ahmax}$ and $|E|_{Avmax}$ versus L_n (L_n is shown in Fig. 5).

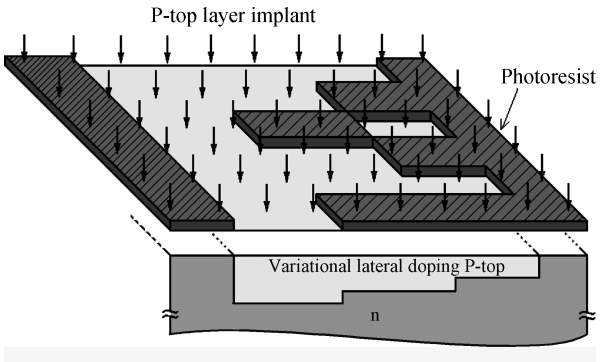

Fig. 8. The implantation of the p-top layer in the proposed structure.

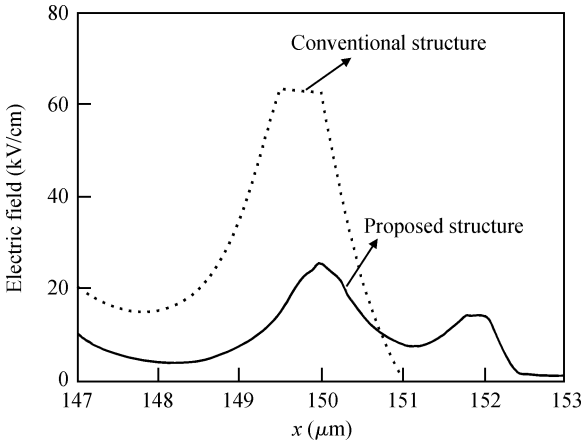

Fig. 9. The obvious reduction of surface electric field peak on the boundary of the p-top and n-well in area B.

Besides, by lateral variational doping instead of uniform doping to the p-top layer, the horizontal electric field peak of the boundary between the p-top and n-well in area B can not only be effectively reduced, but also the whole horizontal surface electric field on p-top can be optimized. Moreover, this is realized solely by mask optimization without process modification, which can be seen in Fig. 8.

Figure 9 reveals that with p-top variational lateral doping,

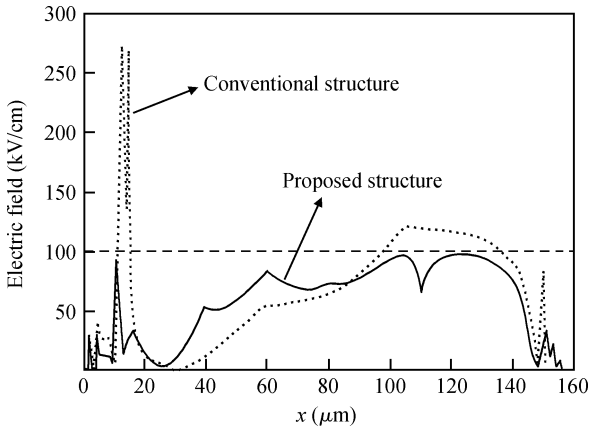

Fig. 10. Comparison of surface electric field distribution between a conventional structure and the proposed structure.

there is an obvious reduction of surface electric field peak on the boundary of the p-top and n-well in area B.

Last, by refining the placement of a variation on lateral doping of the p-top layer, a comparison between the surface electric field distribution of conventional and proposed structures is obtained when $L_b = 15000$ Å, $L_n = 2.4$ μm, as shown in Fig. 10. It intuitively demonstrates that the proposed structure effectively reduces the maximum surface electric field and thus significantly suppresses hot-carrier effects.

4. Conclusions

A hot-carrier effect in the OPTVLD-LDMOS is studied, and an improved structure is proposed. The key feature of the proposed structure is the variation in the lateral doped p-top layer, which can provide a more uniform distribution of surface electric field. It is demonstrated, by combining theoretical analysis and simulation results, that the proposed structure effectively suppresses hot-carrier effects.

Acknowledgment

The authors would like thank to Chen Xingbi's team, Du Cheng, China, in particular to Chen Zao, Du Wenfang, Zhu Liheng and LXinjiang for their advice and help for improving the paper.

References

[1] Chen X B, Zhang B, Li Z J. Theory of optimum design of reverse-biased p–n junctions using resistive field plates and variation lateral doping. Solid-State Electron, 1992, 35(9): 1365
[2] Chen X B, Mawby P A, Salama C A T, et al. Lateral high-voltage devices using an optimized variational lateral doping. Int J Electron, 1996, 80(3): 449
[3] Chen X B, Fan X F. Optimum VLD makes SPIC better and cheaper. IEEE Proc ISCICT, 2001
[4] Versari R, Pieracci A. Experimental study of hot-carrier effects in LDMOS transistors. IEEE Trans Electron Devices, 1999, 46(6): 1228
[5] Cheng C C, Wu J W, Lee C C, et al. Hot carrier degradation in LDMOS power transistors. IEEE Proceedings of 11th IPFA, Taiwan, 2004: 283
[6] Chen X B. Surface voltage sustaining structure for semiconductor devices. USA Patent, No. 5726469, 1998
[7] Sun Zhilin, Sun Weifeng, Yi Yangbo, et al. Study of high reliability P-LDMOS. Chinese Journal of Semiconductors, 2004, 25(12): 1690
[8] Dai Mingzhi, Liu Shaohua, Cheng A, et al. Substrate current and hot-carrier-injection in high voltage asymmetrical n-channel MOS transistor technology. Journal of Semiconductors, 2008, 29(4): 757
[9] Chen X B. Lateral low-side and high-side high-voltage devices. USA Patent, No. 6998681B2, 2006
[10] Liu Enke, Zhu Bingsheng, Luo Jinsheng. Physics of semiconductor. Publishing House of Electronics Industry, 2003: 133
[11] Cao Jianmin, Wu Chuanliang, Zhang Wenjun, et al. Numerical simulation of hot-carrier currents in thin-film SOI/MOSFET. Chinese Journal of Semiconductors, 1998, 19(3): 206
[12] Sze S M, Ng K K. Physics of semiconductor devices. Taiwan: John Wiley & Sons, 2007