A uniform phase noise QVCO with a feedback current source

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Abstract: A novel integrated quadrature voltage controlled oscillator (QVCO) with a feedback current source is presented in this paper. Benefiting from the current adjusting function of the feedback current source, the proposed QVCO exhibits a uniform phase noise over the entire tuning range. This QVCO is implemented in 65-nm CMOS technology. The measurement results show that it draws less than 3-mA average current from a 1.2-V supply and the phase noise is less than −110 dBc/Hz @1MHz offset over the entire tuning range. The fluctuation of phase noise @1MHz offset from the center frequency of 2.84-GHz to 3.27-GHz is less than 1 dBc/Hz, which validates the correctness of the proposed current source feedback technique.

Key words: QVCO; uniform phase noise; current source feedback; CMOS
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1. Introduction

Voltage controlled oscillators (VCOs) are extensively used in frequency synthesizers[1−5] and also used as a local oscillator (LO) directly in wireless communication systems with on-off-keying (OOK) modulation[6].

In frequency generation systems for multi-band and multi-standard wireless communications, the VCO frequency tuning range should cover several hundreds of MHz or even GHz by varactors with a large tuning cap ability or by using digital tuning techniques[7]. However, due to the variation of the Q-factor of the inductors and the effects of switches in digital tuning, the phase noise of a VCO has several dB variations in the required wide tuning range. It turns out that phase noise is always worse in the high operation frequency versus its low frequency counterpart if the highest Q-factor of the inductor is located in the low frequency. In order to improve the phase noise at the high operation frequency, more current has to be added in the tail source, which cannot be achieved in the conventional topology with fixed bias current.

Therefore, a QVCO with a separate bias current transistor is presented in this paper. In this case, the current of the proposed QVCO can be adjusted by the control voltage V_c and thus can ensure a uniform phase noise in the whole frequency tuning range. The proposed QVCO is implemented in a 65-nm CMOS process and validated by measurement results. This paper is organized as follows. Section 2 shows the circuit implementation and design consideration of the proposed QVCO. The measurement results and discussions will be given in Section 3. Section 4 draws some conclusions of this work.

2. Circuit implementation and design

Although a QVCO has a larger chip size and more power consumption than a VCO, as it has two VCO cells and coupling cells composed of active or passive components[8, 9], it is still widely used in the communication systems required of quadrature local oscillation signals. With a proper coupling method and coefficient, a QVCO can realize a perfect quadrature output, which is very important in transceivers with an advanced modulation scheme, such as QAM64, QAM128, and so on. However, the phase noise of a QVCO with a wide band has large fluctuations over the whole tuning range. Therefore, a QVCO with dynamic current bias is proposed to acquire a uniform phase noise in this paper, shown in Fig. 1. M_{i2}, M_{i3}, M_{q2}, and M_{q3} are the cross-coupled transistor pairs of the I part and Q part, respectively. I and Q parts are coupled with transistors M_{i1}, M_{i4}, M_{q1}, and M_{q4}, which are in parallel with cross-coupled transistor pairs. This coupling scheme is suitable for low voltage applications[9].

Unlike conventional structures with fixed bias current, the current sources in the proposed QVCO are divided into two parts, M_i and M_{if} (M_q, M_{qf}). M_i is for the fixed bias current, and M_{if} is for the dynamic current adjusting which is achieved by the controlled voltage V_c of the QVCO.

In order to relax the modulation effect of V_c on the QVCO, a first-order low pass filter (LPF) composed of R_i and C_i (R_q and C_q) is added before the gate of the feedback current transistor M_{if} (M_{qf}). The band width of the LPF is designed with the value of the 1/20 reference frequency used in the phase-locked loop (PLL) to reduce the high frequency component of V_c as much as possible.

When the PLL is locked at a low frequency, The control voltage V_c is low and the feedback current source M_{if} or M_{qf} provides a small current for the QVCO. When the PLL works at a higher frequency, an extra bias current provided by the feedback source M_{if} or M_{qf} can flow into the proposed QVCO and the phase noise will be improved at higher working frequency.

According to the Leeson–Cutler phase noise model[10, 11], the phase noise is proportional to the output signal power and thus the current flowing through the tuning tank when the QVCO operates in a current-limited region, as shown in the following equation.

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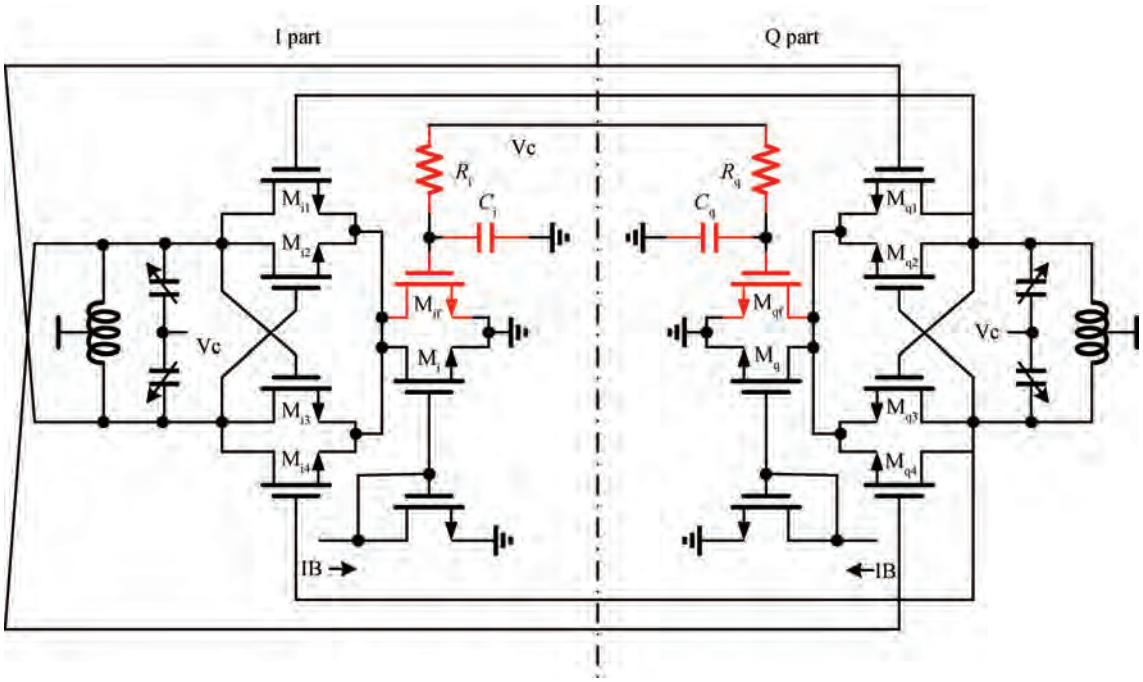

Fig. 1. Proposed QVCO with feedback current source.

$$\mathcal{L}(\Delta\omega) = 10\lg\left\{\frac{2FkT}{P_{\rm s}}\left[1+\left(\frac{\omega_0}{2Q_{\rm L}\Delta\omega}\right)^2\right]\times\left(1+\frac{\Delta\omega_{1/f^3}}{|\Delta\omega|}\right)\right\}, \quad (1)$$

where k is Boltzmann's constant, T is the absolute temperature, F is the empirical parameter, $P_{\rm s}$ is the average power dissipated in the resistive part of the tank, $Q_{\rm L}$ is the effective quality factor of the tank, ω_0 is the oscillation frequency, $\Delta\omega_0$ is the offset from the carrier and $\Delta\omega_{1/f^3}$ is the frequency of the corner between the $1/f^2$ and $1/f^3$ regions. Without loss of generality, we assume that the fixed and feedback currents are $I_{\rm fix}$, $I_{\rm feedback}$, respectively. K_I is defined as $I_{\rm feedback}/I_{\rm fix}$. Based on the analysis and assumptions above, the phase noise is improved with feedback current source by

$$\Delta\mathcal{L}(\Delta\omega) = 20\lg(1+K_I). \quad (2)$$

The simulated fixed and feedback currents are shown in Fig. 2. In our design, the max K_I is chosen with 0.4, and the phase noise at the highest frequency is enhanced by around 3-dB based on past simulations, as shown in Fig. 3. Therefore the introduced feedback current source improves the phase noise over the entire tuning range and keeps phase noise with less than 1-dB fluctuations based on simulation, as may be seen in Fig. 4.

It is worth pointing out that this feedback configuration is suitable for wide band VCO design. The point of the peak Q value of the inductor should be set to the lowest frequency of the operating range. In this case, the feedback current source can also ensure that the phase noise at higher working frequency is as good as its lower frequency counterpart, even with the decreasing Q factor of the inductor in the tank.

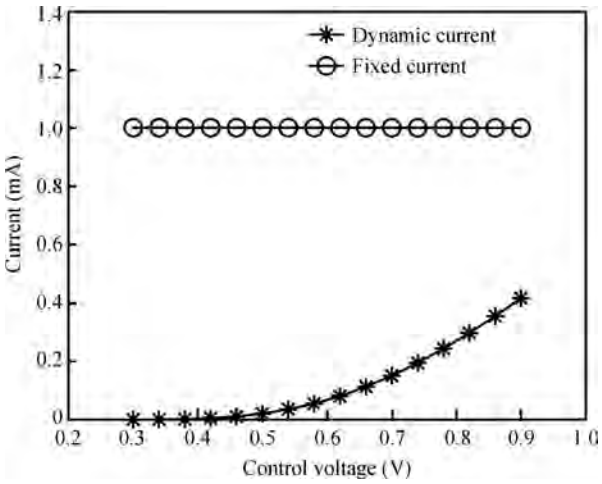

Fig. 2. Simulated currents versus control voltage $V_{\rm c}$.

Quadrature signal mismatch is very significant for the design of QVCO. With a 0.25 coupling coefficient, defined as Eq. (3), and careful layout symmetry considerations, 2° mismatch of the quadrature outputs is achieved in the proposed QVCO.

$$k = \frac{W_1}{W_2}, \quad (3)$$

where W_1 and W_2 are the width of coupling transistor M_{i1} and M_{i2}, respectively.

3. Measurement results and discussions

In order to validate the proposed feedback current scheme, the QVCO is implemented in a 65-nm CMOS process. The core circuit (excluding pads) only occupies an 800 × 300 μm^2 of chip area. The chip micrograph is shown in Fig. 5.

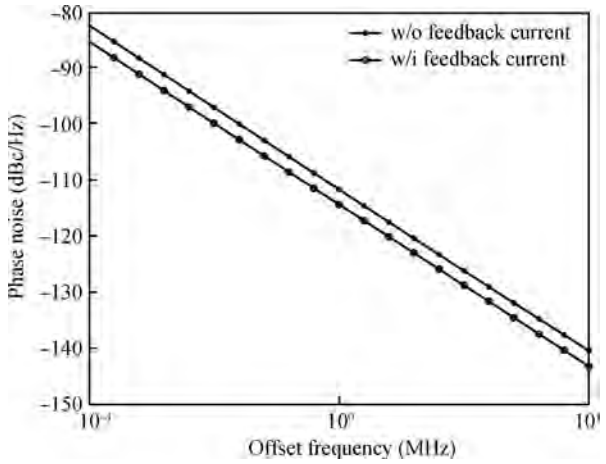

Fig. 3. Simulated phase noise at 3.27-GHz with and without a feedback current source.

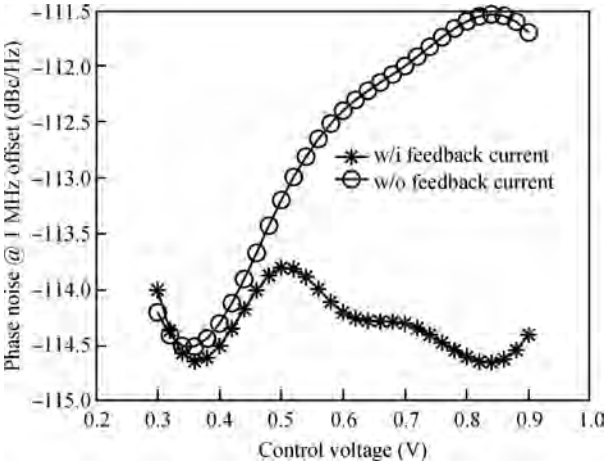

Fig. 4. Simulated phase noise over the control voltage range with and without a feedback current source.

The chip is wire-bonded to a printed circuit board (PCB). The DC voltages and bias currents are offered by a supplier board and the output is measured by a spectrum analyzer.

Figure 6 shows the tuning range of the proposed QVCO, which is from 2.84-GHz to 3.27-GHz. The relative tuning range is 14%. The power spectrum density of the QVCO at 2.884-GHz is shown in Fig. 7 and the measured phase noise at 2.874-GHz is shown in Fig. 8, which is below −110 dBc/Hz@1MHz offset even with a 1-V supply voltage.

The measured phase noise at 1-MHz offset in the whole control voltage range from 0.3 to 0.9 V is shown in Fig. 9, which shows that the variation of the phase noise is lower than 1-dB from 2.84-GHz to 3.27-GHz, which validates the proposed current source feedback scheme. The measured performance of the proposed QVCO is summarized in Table 1.

In order to compare the phase noise variation of different works, a parameter is defined as the follows.

$$m = \frac{\Delta\mathcal{L}(\Delta\omega)\cdot f_{\rm c}}{\Delta{\rm BW}}, \tag{4}$$

where $\Delta\mathcal{L}(\Delta\omega)$ is the phase noise variation in the frequency tuning band, $f_{\rm c}$ is the center frequency of the tuning range, and

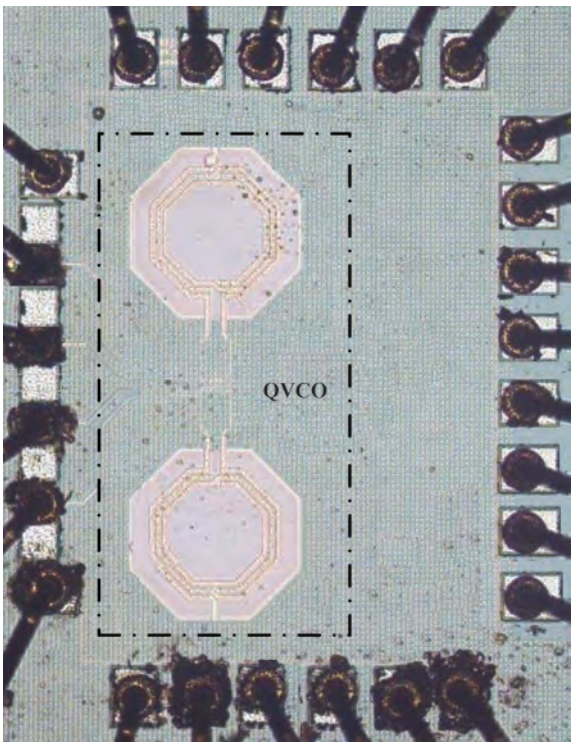

Fig. 5. Chip micrograph of the proposed QVCO.

Table 1. Summary of measurement results.

Parameter	Value
Power @ $V_{\rm DD}$ (mW @ V)	< 3.6 @ 1.2
Tuning range (GHz)	2.84–3.27
Phase noise (dBc/Hz @ 1 MHz)	< −110
Phase noise fluctuation (dBc/Hz)	< 1
Chip size (mm^2)	0.24
Technology	65-nm CMOS

ΔBW is the frequency tuning range. Based on the Eq. (4) and measurement results, a summary of performance comparisons with previously published literatures are listed in Table 2. To the best knowledge of the author, the fluctuation of the phase noise in the whole tuning band is the smallest in the reported works.

4. Conclusion

A novel integrated QVCO using a current feedback technique is proposed in this paper. It is implemented in 65-nm CMOS technology. It draws less than 3-mA from a 1.2-V supply and has achieved 2° phase mismatch between the quadrature outputs. Benefiting from the feedback current source, the phase noise at the higher operating frequency is as good as that at low frequency. The measurement results show that the fluctuation of the phase noise over the entire tuning range from 2.84-GHz to 3.27-GHz is no larger than 1-dB, which validates the correctness of the proposed feedback current scheme.

References

[1] Park E C, Ryu I, Koh J, et al. A 3-10 GHz flexible CMOS LO generator for MB-OFDM UWB application using wide tunable

Table 2. Performance comparison with a state-of-the-art LC-QVCO.

Parameter	Tuning range (GHz)	Phase noise (dBc/Hz)	m (dB)	DC power consumption (mW)	Chip area (mm^2)	Technology
Ref. [12]	3–4	−113.5 @ 1 MHz	—	14.6	—	0.18-μm CMOS
Ref. [13]	Around 1.5	−118 @ 1 MHz	—	28.8	—	0.25-μm CMOS
Ref. [14]	1.64–1.97	−140 @ 3 MHz	16.7	50	0.2	0.35-μm CMOS
Ref. [15]	7.03–7.26	−111.2 @ 1 MHz	—	2.2	0.48	0.18-μm CMOS
This work	2.84–3.27	< −110 @ 1 MHz	7	< 3.6	0.24	65-nm CMOS

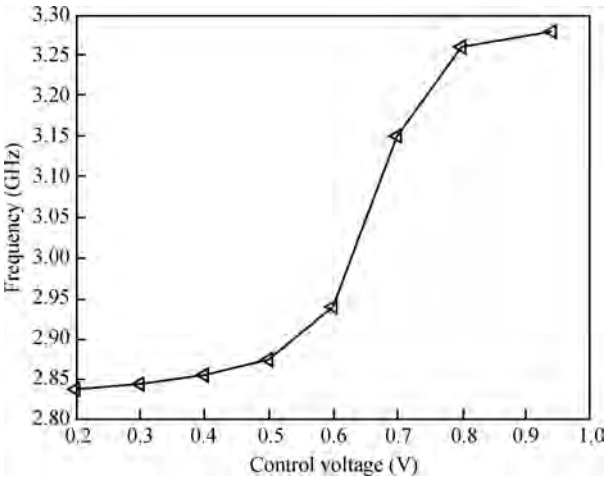

Fig. 6. Measured tuning range of the proposed QVCO.

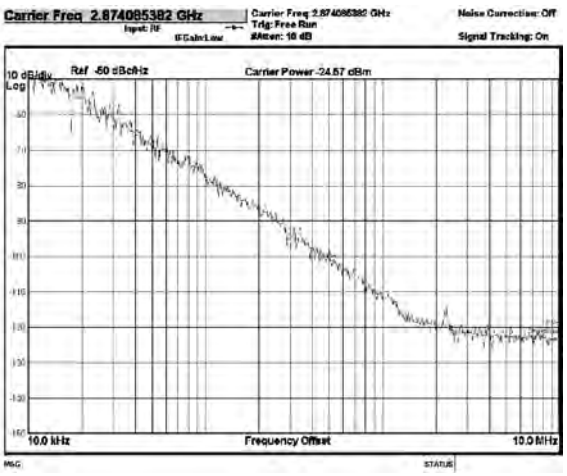

Fig. 8. Measured phase noise at 2.874 GHz.

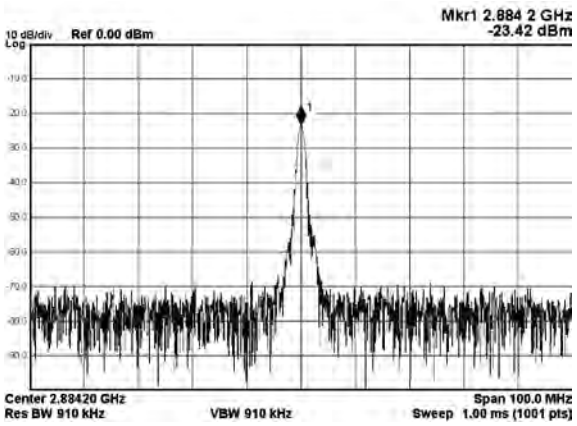

Fig. 7. Measured power spectrum density of the proposed QVCO.

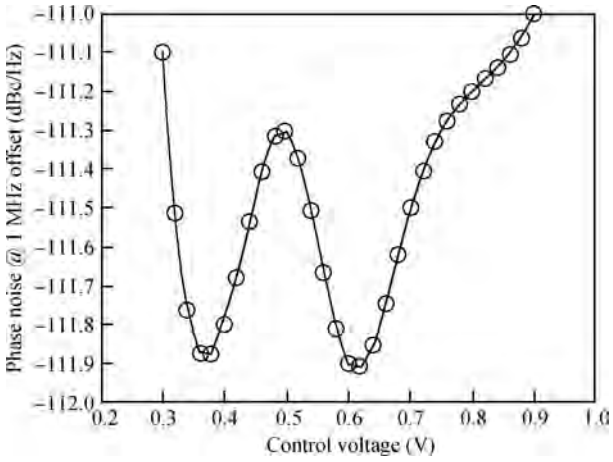

Fig. 9. Measured phase noise at 1 MHz offset versus control voltage.

VCOs. ESSCIRC Dig Tech, 2008: 338

[2] Zhou C, Li G, Zhang C, et al. A fractional-N frequency synthesizer for WCDMA/Bluetooth/ZigBee applications. Journal of Semiconductors, 2008, 29(7): 075008

[3] Yu X, Sun Y, Rhee W, et al. A 65 nm CMOS 3.6 GHz fractional-N PLL with 5th order $\Delta\Sigma$ modulation and weighted FIR filtering. IEEE Asian Solid-State Circuits Conference, 2009: 77

[4] Yu X, Sun Y, Rhee W, et al. A $\Delta\Sigma$ Fractional-N synthesizer with customized noise shaping for WCDMA/HSDPA applications. IEEE J Solid-State Circuits, 2009, 44(8): 2193

[5] Zhang L, Yu Y, Sun Y, et al. A hybrid spur compensation technique for finite-modulo fractional-N phase-locked loops. IEEE J Solid-State Circuits, 2009, 44(11): 2922

[6] Lee J, Huang Y, Chen Y, et al. A low-power fully integrated 60 GHz transceiver systems with OOK modulation and on-board antenna assembly. IEEE ISSCC Dig Tech, 2009: 361

[7] Berny A D, Niknejad A M, Meyer R G. A 1.8-GHz LC VCO with 1.3-GHz tuning range and digital amplitude calibration. IEEE J Solid-State Circuits, 2005, 40(4): 909

[8] Ng A W L, Luong H C. A 1-V 17-GHz 5-mW CMOS quadrature VCO based on transformer coupling. IEEE J Solid-State Circuits, 2007, 42(9): 1933

[9] Lee S Y, Chen C Y. Analysis and design of a wide-tuning-range VCO with quadrature outputs. IEEE Trans Circuits Sys II, 2008, 55(12): 1209

[10] Cutler L S, Searle C L. Some aspects of the theory and measurement of frequency fluctuations in frequency standards. Proc IEEE, 1966, 54: 136

[11] Leeson D B. A simple model of feedback oscillator noises spectrum. Proc IEEE, 1966, 54: 329

[12] Ramiah H, Zainal T, Zulkifli A. Design of 3–4 GHz tunable low

noise LC-QVCO for IEEE 802.11a WLAN application. IEEE Asia Pacific Conference on Circuits and Systems, 2006: 506
[13] Choi H C, Shin S B, Lee S G. A low-phase noise LC-QVCO in CMOS technology. IEEE Microwave and Wireless Components Letters, 2004, 14(11): 1209
[14] Andreani P, Bonfanti A, Romano L, et al. Analysis and design of a 1.8-GHz CMOS LC quadrature VCO. IEEE J Solid-State Circuits, 2002, 37(12): 1737
[15] Huang T H, Tseng Y R. A 1 V 2.2 mW 7 GHz CMOS quadrature VCO using current-reuse and cross-coupled transformer-feedback technology. IEEE Microwave and Wireless Components Letters, 2008, 18(10): 698