A 20-GHz ultra-high-speed InP DHBT comparator

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Abstract: An ultra-high-speed, master-slave voltage comparator circuit is designed and fabricated using InP/GaInAs double heterojunction bipolar transistor technology with a current gain cutoff frequency of 170 GHz. The complete chip die, including bondpads, is 0.75×1.04 mm^2. It consumes 440 mW from a single –4 V power supply, excluding the clock part. 77 DHBTs have been used in the monolithic comparator. A full Nyquist test has been performed up to 20 GHz, with the input sensitivity varying from 6 mV at 10 GHz to 16 mV at 20 GHz. To our knowledge, this is the first InP based integrated circuit including more than 70 DHBTs, and it achieves the highest sampling rate found on the mainland of China.

Key words: InP; comparator; HBT; emitter coupled logic; latched comparator; sensitivity
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1. Introduction

The analog to digital convertor (ADC) is a bridge between the real continuous world and the digital discrete world. Nowadays, vast amount of the real world analog data needs to convert into digital ones in a very short time period. High-speed analog-to-digital converters (ADCs) are crucial components in a number of electronic applications, such as high-performance real-time oscilloscopes, software-defined radio, high-speed communication systems, and electronic warfare. The comparators in these ADCs play a key role in determining the overall sampling rates and resolutions of the converter, and must be able to compare the input signal against the reference voltage quickly. Therefore, an excellent comparator should have a high sampling rate, high bit resolution, and low power consumption.

Presently, the main technologies used in high-speed integrated circuits are Si MOSFETs, SiGe HBTs and InP HBTs. Compared with Si MOSFETs, bipolar technologies still have their intrinsic advantages in analog/mixed-signal circuits. The high transconductance, high breakdown voltage and precisely controlled DC parameters of bipolar transistors provide great potential for high-precision mixed-signal circuits[1]. Monolithic high-speed comparators fabricated in HBTs with sampling rates of up to 32 GHz, has been reported[2]. The main advantages of InP-based HBTs compared to SiGe HBTs are their higher breakdown voltage and higher electron mobility, which are beneficial to both speed and resolution.

In this paper, we present an ultra-high-speed, medium resolution comparator that has been designed and fabricated in in-house using InGaAs/InP DHBTs. The comparator employs a broadband preamplifier with a Cherry–Hooper structure and master–slave latches with an emitter coupled logic configuration. Its measured input sensitivity voltage has reached 16 mV_{pp} at 20 GS/s, which means that it has 6 bits of resolution at 20 GS/s with a differential input dynamic range of 1 V peak-to-peak. The comparator is well-suited for use in medium resolution, ultra-high-speed ADCs.

2. InP DHBT technology and circuit design

The comparator was designed and fabricated using an InP DHBT with an emitter size of 1×15 μm^2. The DHBTs are characterized by a current gain cutoff frequency f_T of 170 GHz, a maximum oscillation frequency f_{max} of 253 GHz, and a breakdown voltage BV_{CEO} of 6 V[3]. The technology includes two interconnection levels, thin-film TaN resistors (50 Ω/□), and metal–insulator–metal (MIM) capacitors. The HBT device model used in our circuit design was established and discussed in detail in Ref. [4]. Our group has designed and demonstrated a number of high-speed circuits in this technology, such as a 40 GHz static frequency divider[5].

As illustrated in Fig. 1, the comparator consists of a preamplifier, a clock buffer, bias current generators, a D-FF (master/slave latch), and an output buffer. The clock buffer converts the input sine wave into Track/Latch control signals with low jitter.

2.1. Preamplifier

The preamplifier, shown in Fig. 2, was employed to match the input source with 50 Ω pull-up resistors and increase the comparator's sensitivity. The emitter-followers before the differential Cherry–Hooper amplifier help to realize the level shift and reduce the kickback noise created by the switching of the latch in the following stage. The Cherry–Hooper amplifier is used as the preamplifier because it has a high gain-bandwidth product and is easy to implement in our technology without inductively peaked gain stages with active or passive inductors. The gain A of the amplifier can be written as[6]:

$$A = \frac{(R'_f + r_{d5})(R_1 + R_2)}{r'_{d1}(r'_{d3} + R_1)}, \quad (1)$$

where $r_{dk} = 1/g_{mk}$, $r'_{dk} = 1/g_{mk} + r_{ek}$, g_{mk} is the transconductance of transistor k, r_{ek} is the parasitic emitter resistance

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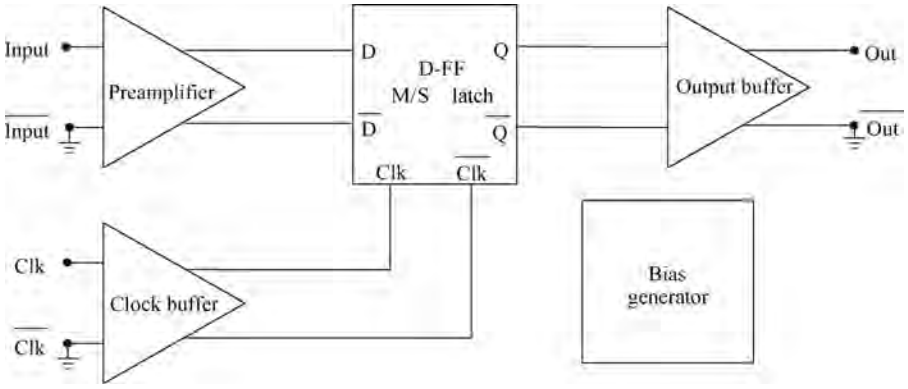

Fig. 1. Block diagram of the comparator.

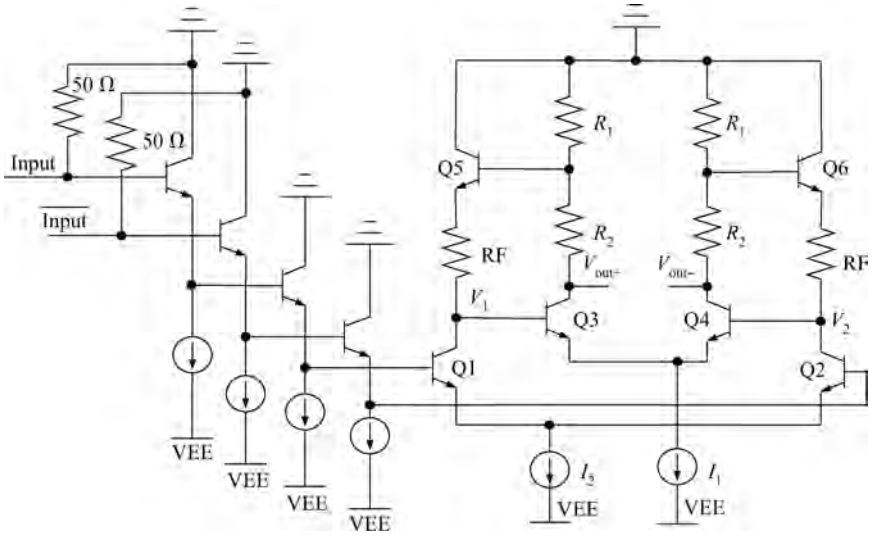

Fig. 2. Cherry–Hooper preamplifier.

of transistor k, and $R'_{\rm f} = R_{\rm f} + r_{\rm e5}$. The bandwidth of the amplifier can be decided by the pole frequency ω_0 which is given by[6]:

$$\omega_0 = \left[\frac{r'_{\rm d3} + R_1}{r'_{\rm d3} C_1 C_{\rm L}(R'_{\rm f} + r_{\rm d5})(R_1 + R_2)}\right]^{1/2}, \qquad (2)$$

where C_1 represents the sum capacitance of node V_1, $C_{\rm L}$ is the capacitance of load. From Eqs. (1) and (2), the value of $R_{\rm f}$ and R_2/R_1 should be optimized with consideration of a proper trade-off between the gain and the bandwidth. Fortunately, we can adjust the feedback resistor $R_{\rm f}$ and load resistors (R_1 and R_2) to obtain the desired gain and bandwidth. In our design, the value of R_1, R_2 and $R_{\rm f}$ has been fixed at 30 Ω, 30 Ω and 25 Ω, respectively.

2.2. Comparator core

The schematic of the M/S latch is shown in Fig. 3. Each latch consists of a differential pair (Q7 and Q8), a cross-coupled differential pair (Q9 and Q10) and an emitter follower pair (Q13 and Q14). The emitter follower pair can be employed to reduce the loading effect of the following stage, accelerate the regeneration process, and increase the output voltage swing[7]. The maximum sampling rate of the latch is determined by the sum of the recovery time and regeneration time. The recovery time $t_{\rm reg}$ is defined as the time that the differential pair's output voltage changes from a full logic swing to zero when the latch is switching from the latch phase to the track phase. The recovery time $t_{\rm reg}$ can be given by[2]

$$t_{\rm rec} = R_{\rm L} C_{\rm total} \ln\left[1 + \frac{1}{\tanh(V_{\rm in}/2V_{\rm T})}\right], \qquad (3)$$

where $C_{\rm total}$ is the total load capacitance at the output of the differential pair, $R_{\rm L}$ is the load resistor, $V_{\rm in}$ is the differential input voltage of the latch, and $V_{\rm T}$ is the thermal voltage. The regeneration time is the time required for the latching pair to fully switch from an initial voltage to full scale output, given by[7]

$$t_{\rm reg} = \frac{R_{\rm L} C_{\rm total}}{g_{\rm m} R_{\rm L} - 1} \ln \frac{\Delta V}{\delta v}, \qquad (4)$$

where $g_{\rm m}$ is the transconductance of the HBTs in the second differential pair (Q9 and Q10), ΔV is the maximum output voltage amplitude, δv is the initial voltage difference in latch process. In general, $g_{\rm m} R_{\rm L} \gg 1$, the regeneration time is much lower than the recovery time from Eqs. (3) and (4). Therefore, the recovery time is the dominant factor in the response time of the latch. A small $R_{\rm L}$ can make $t_{\rm reg}$ shorter. However, a small $R_{\rm L}$ also limits the output swing of the latch and degrades the

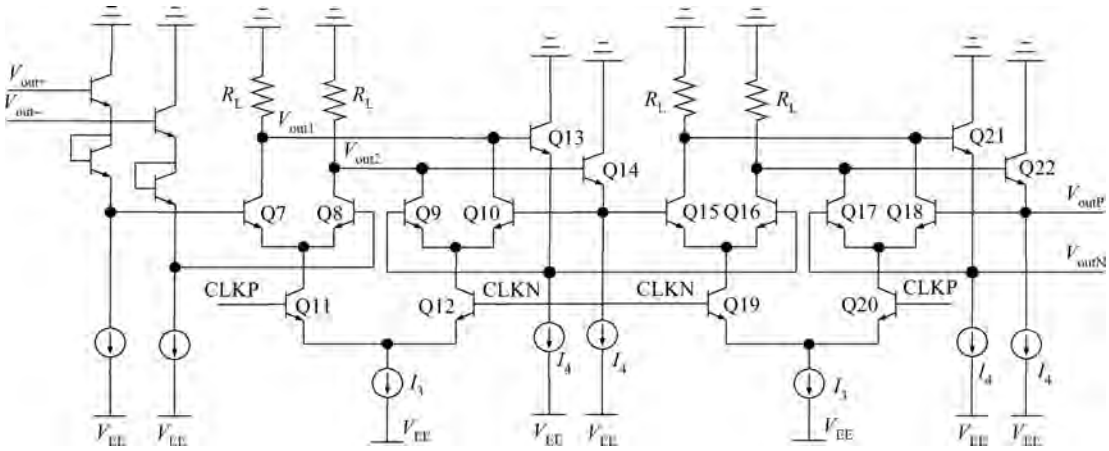

Fig. 3. Master/Slave latch.

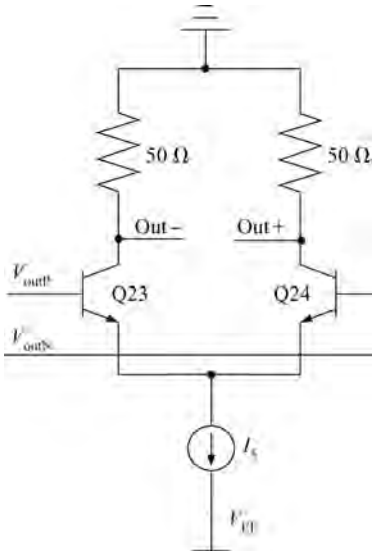

Fig. 4. Output buffer.

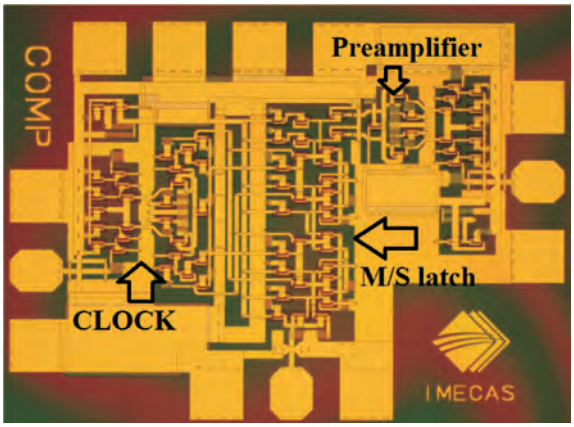

Fig. 5. Microphotograph of the chip.

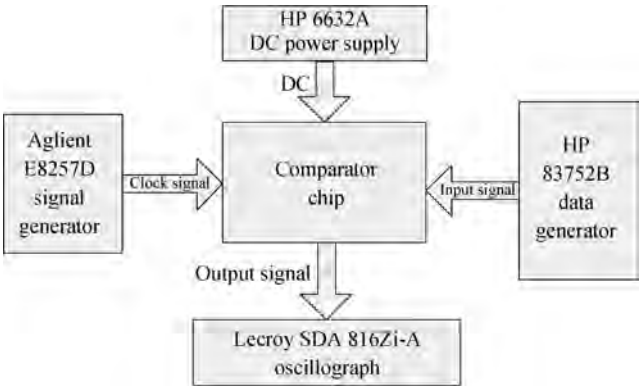

Fig. 6. Schematic diagram of the measurement system.

driving ability to the slave latch. In our design, a trade-off was made with an R_L of 20 Ω. Simulations show that a 12 ps recovery time can be achieved at a V_{in} of 20 mVpp, and it is sufficient for operation at a 20 GHz sampling rate.

2.3. Output buffer

Figure 4 shows a simple output buffer with two collector load resistors of 50 Ω matched to the input impedance of the test instrumentation. A tail current I_5 is provided to keep the moderate output amplitude, with a value of $R_{Load}I_5$. The R_{Load} is about 25 Ω, which originates from the parallel connection of a 50 Ω internal resistance and the 50 Ω impedance of the measurement instrument. We can adjust the value of I_5 to obtain a desired logic swing.

2.4. Layout

The chip micrograph of the comparator is shown in Fig. 5. The total die area is 0.75 × 1.04 mm^2, including bondpads. Proper layout is very important in ultra-high-speed circuits when operating up to GHz frequency range. Parasitics introduced by layout can heavily degrade the performance of high-speed circuits, and special care must be taken to minimize their impact. The layout is made as symmetrical as possible in order to reject common-mode noise, and the length of interconnects in the critical path are kept short to reduce layout parasitics.

3. Measurements and results

The schematic diagram of the on-wafer measurement system is shown in Fig. 6. The clock input signal and the input sig-

Table 1. Comparison with published high-speed comparators.

Parameter	Technology/ f_T (GHz)	Power consumption (mW)	Power supply (V)	Sampling rate (GS/s)	Sensitivity (mV)	Chip area (mm^2)	Location
Ref. [9]	Si–SiGe/55	80[a]	N/A	16	20	N/A	San Diego, USA
Ref. [10]	SiGe/120	82[a]	3.5	18	8.9	1.80	Atlanta, USA
				20	40.8		
Ref. [2]	SiGe/200	405	3.5	20	12	1.975	Atlanta, USA
				32	30		
Ref. [8]	InP/300	336[b]	6	20	10	1.00	Haifa, Israel
Ref. [11]	GaAs/60	N/A	–5.2 & +3.3	12.5	35.6	5.29	Beijing, China
This	InP/170	180[b]	–4	20	16	0.78	Beijing, China
work		440[c]		10	6		

[a] Preamplifier and M/S latches only. [b] M/S latches only. [c] Excluding clock part.

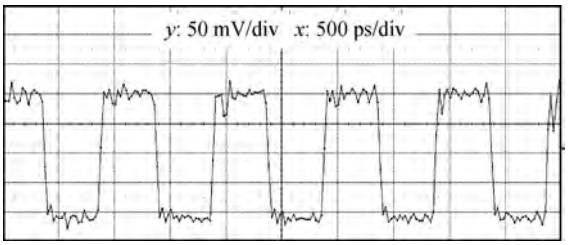

Fig. 7. Measured output waveform with a 20 GHz clock and 1 GHz input.

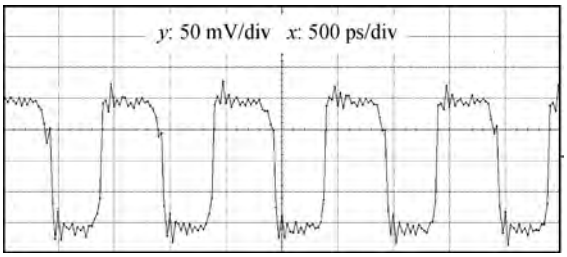

Fig. 8. Measured output waveform with a 20 GHz clock and 19 GHz input.

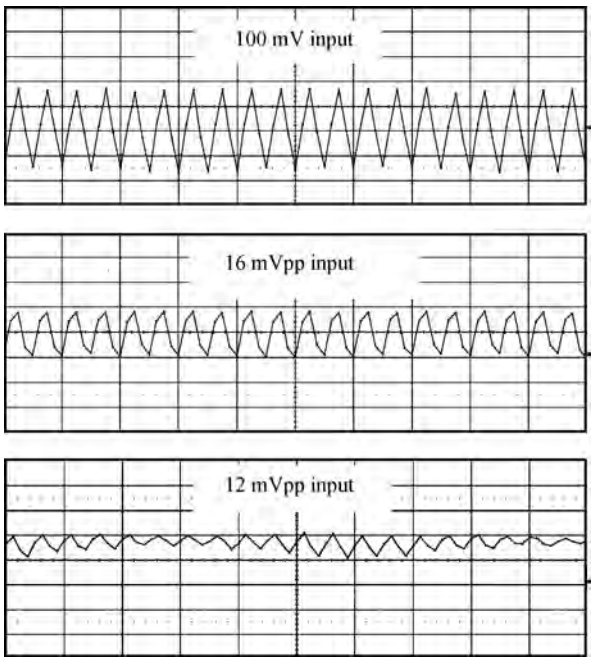

Fig. 9. Measured waveforms of the comparator differential output at 20 GS/s at various input amplitudes. *y*: 50 mV/div. *x*: 200 ps/div.

nal were generated by an Aglient-E8257D, and an HP-83752B signal generator, respectively. The output signals were sampled and analyzed by using a Lecroy SDA 816Zi-A real-time oscilloscope (40 GS/s). All these signals were connected by high-frequency probes and cables. The circuit was tested with sine wave input and clock.

The measured output waveform (single-ended) of the comparator operating at a clock frequency of 20 GHz, with an input frequency of 1 GHz, is shown in Fig. 7. The measured output waveform (single-ended) of the comparator operating at a clock frequency of 20 GHz, with an input frequency of 19 GHz, is shown in Fig. 8. This comparator works well and has broad bandwidth due to the broadband preamplifier. Operating at Nyquist, the output waveforms (single-ended) of the comparator at 20 GHz sampling rate are shown in Fig. 9.

Generally, the input sensitivity of the comparator is defined to be the minimum differential input peak-to-peak voltage that can be detected, which is a critical parameter in high-speed and high-precision data conversion applications. However, to facilitate the measurement of the sensitivity of the comparator, another definition of the sensitivity is introduced in our measurement, which is the input peak-to-peak voltage when the output amplitude was reduced by a factor of two[8]. The differential input voltage at which the simulated output amplitude dropped by a factor of two was 10 mVpp. Experimentally, the differential input peak-to-peak voltage was 16 mVpp, as shown in Fig. 9. This demonstrates that the comparator is well-suited for ultra-high-speed, medium-resolution ADCs.

Numerous comparators have been published in the literature. Comparisons of this work to other high-speed stand-alone comparators are shown in Table 1. The comparators integrated in ADCs are not included due to lack of direct measurement results on the comparators. Due to the use of a broadband Cherry–Hooper preamplifier to create a large bandwidth instead of using a traditional differential amplifier, the gain of preamplifier is less than in Ref. [2]. Some sensitivity enhancement techniques have been used in Ref. [8], such as introducing peaking inductors and using emitter degeneration resistors. The sensitivity of our comparator is fairly good, but inferior

to Refs. [2, 8] at a similar sampling rate. To the best of our knowledge, the comparator in Ref. [11] had the highest sampling rates in mainland China before the fabrication of our comparator. The possible reasons why our proposed comparator is not better than the comparator using SiGe are as follows. In our process, only two layers of gold interconnect were used and a comparatively large scale device was adopted to ensure the high yield. So the interconnect between devices and the interstage interconnect of the comparator was long, which may introduce more layout parasitics and increase transmission delay. For the consideration of high reliability, DHBTs in this design were biased at a comparatively low bias point other than the high current bias point where the maximum f_T was measured.

Finally, power consumption is a very important parameter in integrated circuits. Operating off a -4 V power supply, the comparator dissipates a total power of 840 mW, with the M/S latch core consuming 180 mW. Due to the absence of a variable high frequency square wave source, a clock generator circuit converting the input sine wave into Track/Latch control signals consuming 400 mW (approximately half of the total power) was fabricated, which is not required in the other comparators listed in Table 1.

4. Conclusions

An ultra-high-speed comparator has been designed and fabricated in an in-house InGaAs/InP DHBT. The comparator has a measured input sensitivity of 16 mV at 20 GS/S and a differential input dynamic range of 1 Vpp, equivalent to 6.0 bits of ADC resolution. Therefore, this comparator is well-suited to ultra-high-speed, medium resolution ADCs. To the best of our knowledge, this comparator achieves the highest sampling rate in mainland China. Although the performance of the circuit is limited by the interconnection and our test equipment, the circuit makes great progress in InP-based ultra-high-speed circuits. It demonstrates that our InP technology can be used to design and fabricate fairly complex circuits.

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