A 2-mW 50-dB DR wideband hybrid AGC for a GNSS receiver in 65 nm CMOS*

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Abstract: A low-power wideband hybrid automatic gain control (AGC) loop for a GNSS receiver is presented. Single AGC in the I/Q path is composed of four-stage programmable gain amplifiers (PGAs), a differential peak detector, two comparators, a control algorithm logic, a decoder and the reference voltage source. Besides being controlled by an AGC loop, the gain of PGAs could alternatively be controlled by an off-chip digital baseband processor through the SPI interface. To obtain low power consumption and noise, an improved source degenerated amplifier is adopted, and the I/Q path phase mismatch within the $\pm 5^\circ$ range is calibrated with 0.2° accuracy. Implemented in 65 nm CMOS, the measured PGA total gains range from 9.8 to 59.5 dB with an average step of 0.95 dB and simulated bandwidth of more than 110 MHz. The settling time is about 180 μs with 80% AM input with measured signal power from –76.7 to –56.6 dBm from a radio-frequency amplifier (RFA) input port, and also reduces to 90 μs with clock frequency doubling. The single AGC consumes almost 0.8 mA current from the 2.5-V supply and occupies an area of 750×300 μm^2.

Key words: AGC; hybrid; GNSS; PGAs; I/Q phase calibration; settling time

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1. Introduction

Nowadays, the global navigation satellite system (GNSS) has been developed rapidly for civil use. Currently, the GNSS contains the global positioning system (GPS), Galileo, GLONASS and Compass. With the increasing demands for low cost, low power and high accuracy, highly integrated receivers with multi bands and modes such as dual-band[1, 2], dual-mode[3] and even tri-mode[4] have been reported.

Due to the complicated application environment, the received signal power at the antenna varies with a large range. Taking GPS as an example, the minimum input power is about –130 dBm for L1-band and –133 dBm for L2-band, respectively, and typically there is a great deal of interference (GSM at 825 MHz, DCS1800/AWS at 1710 MHz and WiFi/Bluetooth at 2.4 GHz co-existing around GPS bands[5]), which will degrade the total noise figure (NF) and gain of the whole receiver. To correctly demodulate the received signal with different strengths, the total gain of the receiver should be adjusted automatically according to the input signal strength. So an AGC loop with a large gain range and low NF is essential in a GNSS receiver.

Figure 1 shows the whole block diagram of the proposed dual-channel reconfigurable receiver which supports all GNSS modes[6] and incorporates the AGC loop in both in-phase (I) and quadrature (Q) paths. To lower the dynamic range requirement for the analog-to-digital converter (ADC), the AGC loop automatically adjusts the total gain to keep the input signal amplitude of the ADC approximately constant.

According to the flexible frequency plan in Ref. [6], the receiver could switch between low intermediate frequency (LIF) and zero-IF architecture in different modes. When GPS L2 W-band (IF 0 MHz, BW 18 MHz) & GLONASS L2 W-band (IF 18.4 MHz, BW 18 MHz) mode operates simultaneously in dual channels, the highest analog baseband signal with 18.4 MHz IF and 18 MHz bandwidth after down-conversion arises. To make the bandwidth of the whole analog baseband only up to the IF filter, the total PGAs should have low attenuation at the highest signal frequency, which requires wide bandwidth. In addition, because I and Q signals pass through separate paths, it is difficult to keep I and Q baseband signals having perfect balance in magnitude and phase, causing SNR degradation to the digital baseband, which makes I/Q calibration and a small gain step extremely necessary in PGAs.

This paper presents a low-power AGC loop containing four-stage PGAs with wide bandwidth, 50 dB gain range and 1 dB step, a wideband differential peak detector and algorithm logic. The I/Q phase calibration is also achieved in the last stage. The algorithm logic generates gain control codes according to the output signal amplitude. The whole circuits are implemented in a 65 nm CMOS process, and all transistors are adopted by 2.5-V thick gate transistors for better linearity and the avoidance of gate-leakage issues.

2. Architecture description

The block diagram of the single AGC loop is shown in Fig. 2, which adopts hybrid architecture combining the analog differential peak detector and threshold comparators with digital algorithm logic to generate gain control codes, which are then decoded to control the total gain of the PGAs. The

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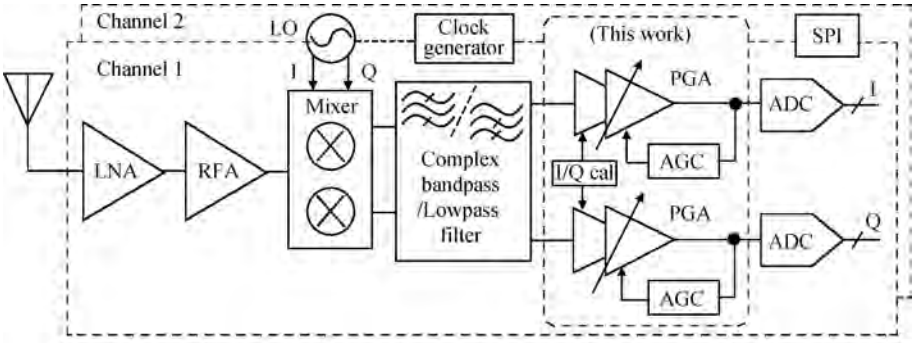

Mode	GPS			Compass			GLONASS		Galileo		
Band	L1	L2	L5	B1	B2	B3	L1	L2	E1	E5a	E5b
BW (MHz)	2.2/18	18	18	4.2	4.2/18	18	10/18	8/18	2.2	18	18

Fig. 1. The dual-channel multi-mode GNSS receiver incorporating I/Q AGC loops.

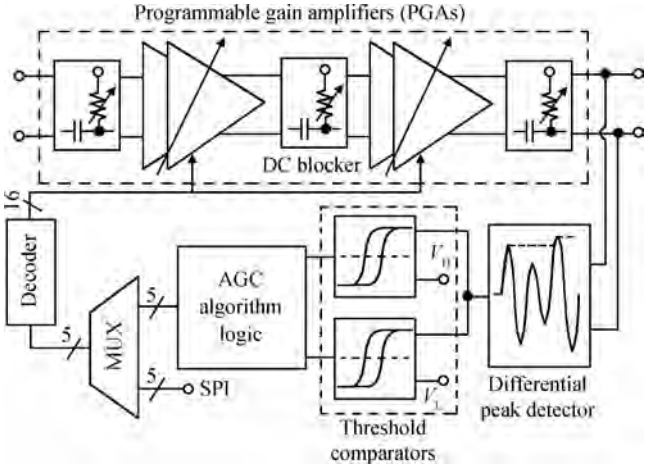

Fig. 2. Block diagram of the single AGC loop.

PGAs contain four stages and DC blockers are inserted to remove DC offset from preceding stages. In addition, the gain control codes could alternatively come from the off-chip digital baseband processor through the SPI interface.

Compared with the analog AGC circuit[7] which adopts variable gain amplifiers (VGAs) to amplifier signals and sets total gains with an analog open-loop gain-control algorithm, the proposed architecture consumes less power and makes it easier to maintain the stability of the AGC loop.

When the signals are filtered by the complex bandpass/lowpass filter and enter into the PGAs, the amplified output signals are caught and held at the maximum amplitude by the differential peak detector. The held peak voltage is then compared to two threshold reference voltages. And then the AGC algorithm logic generates gain control codes according to digital outputs of the threshold comparators. The decoder translates 6-bit gain control codes to 16-bit gain control words to control the corresponding switches in the PGAs.

Due to the possible out-band strong interference and to keep the AGC loop stable, the AGC loop has hysteresis change configuration implemented by setting a programmable high or low threshold voltage for the comparators. The gap between the high $V_{\rm H}$ and low $V_{\rm L}$ threshold voltage is 2.5 dB and 6 dB optionally with a constant upper threshold. Once the peak amplitude steps into the range between the lower and upper threshold, the logic will hold the gain control codes.

Table 1. The distributed gain range and step of each PGA.

Stage	Gain range (dB)	Step (dB)
PGA1	0–12	6
PGA2	2–18	4
PGA3	8–16	1
PGA4	0–16	8

Taking the non-ideal effects of MOS switches into consideration, to attain a high gain range from 10 to 60 dB with 1 dB step, several dB gain margins should be set aside, and Table 1 shows the distributed gain range and step of each PGA stage.

To obtain low power consumption, the previous three stages adopt a source degenerated amplifier. The resistor-feedback amplifier with I/Q phase calibration is implemented in the last stage to balance the signal phase mismatch between the I and Q paths. Only the third stage has a gain step of 1 dB and other stages more than 1 dB, which will shorten the response time when adjusting gains, and the total switch numbers will be reduced, thus lowering the effects of the PGA switches on performances. The gain of the first stage (PGA1) is relatively high to suppress noise contributed by the following stages. The gain range and step of each stage are combined to achieve the whole gains from 10 to 62 dB with 1 dB step. Assuming that the allowable gain attenuation is less than 1 dB at the highest signal frequency, each PGA should have a bandwidth of more than 110 MHz according to the single-pole response analysis.

The differential peak detector should catch the maximum amplitude of the amplified signals at the highest signal frequency with little error. According to the maximum signal frequency and to make enough margins, the peak detector should operate at more than 30 MHz normally. Considering the response time of the peak detector and the fast-settling time of the AGC loop, the clock period of the AGC algorithm logic is set to 10.5 μs with $^1/_{21}$ duty cycle, which is generated by a clock generator (illustrated in Fig. 1) with a default output frequency of 24.6 MHz through divide-by-12 and then divide-by-21 counters successively. Besides being controlled by AGC

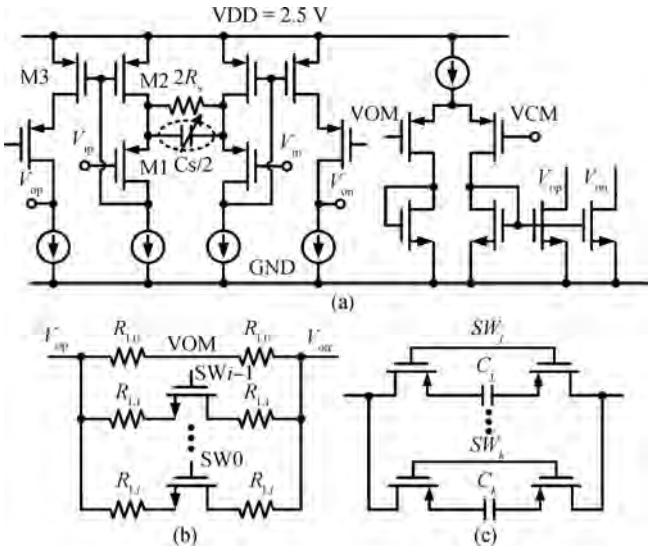

Fig. 3. The improved source degenerated amplifier. (a) Main amplifier with CMFB. (b) Load resistors R_L array. (c) Source degenerated capacitor C_s array.

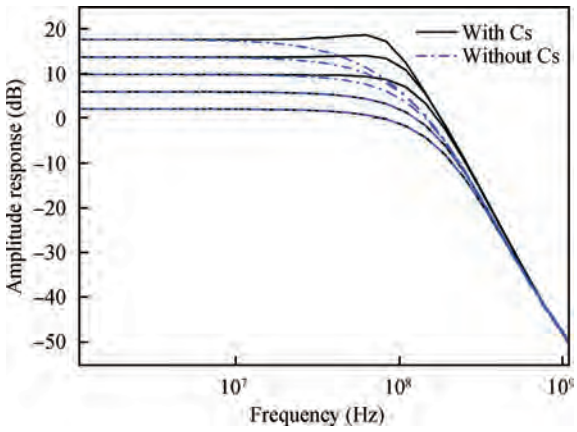

Fig. 4. The simulated amplitude response of the second stage (PGA2) with and without C_s.

loop, the PGA gains are controlled by the off-chip digital baseband processor through the SPI interface, while the peak detector, comparators and algorithm logic are shut down to save power.

3. Circuit implementation

The main circuits in a single AGC loop contain four-stage PGAs, the differential peak detector and the AGC algorithm logic.

3.1. Programmable gain amplifier (PGA)

Considering low power consumption and the high output 1 dB compression point, both source-degenerated and resistor-feedback amplifier topologies are adopted to achieve 10 to 60 dB gains with 1 dB step. The simulated total NF and output 1 dB compression point at 4 MHz and maximum gain are 31.9 dB and 17.0 dBm, respectively, which satisfy the requirements for the GNSS receiver.

3.1.1. Improved source degenerated amplifier

Based on the g_m-boosted source degenerated differential amplifier with resistive loads[8], an improved source degenerated amplifier is proposed to save power consumption, as shown in Fig. 3, which consumes about 130 μA in total.

The source degenerated capacitors (shown in Fig. 3(c)) are inserted to introduce an additional zero to extend the bandwidth without extra power consumption, as expressed in Eq. (1). The source degenerated resistor R_S is fixed at a relatively small value to produce less noise and achieve a larger g_m to suppress other noise in the amplifier.

To eliminate the body effect of the input transistor, the input pairs choose PMOS with source and bulk connected. Transistors M1–M2 (shown in Fig. 3(a)) form a local negative feedback loop which reduces the equivalent source resistance of M1, value given by $1/g_{m2}g_{m1}r_{o1}$ approximately, where g_{m1} and g_{m2} are the transconductances of M1 and M2, respectively. During the design, M3 has the same parameters as M2.

Considering the finite output resistor r_o of the transistors, from the small-signal equivalent circuit analysis, the gain of the overall amplifier is expressed approximately by

$$A_V \approx \frac{R_L}{\left(R_s||\frac{1}{sC_s}\right)+\frac{1}{g_{m2}g_{m1}r_{o1}}} \approx \frac{R_L}{R_S}(1+sR_sC_s), \quad (1)$$

where $1/g_{m2}g_{m1}r_{o1} \ll R_S$ and the load resistor R_L arrays are controlled by switches to attain gain range and steps as listed in Table 1.

The simulated amplitude response of the second stage of PGAs with and without C_s is shown in Fig. 4. The –3 dB bandwidth is obviously extended to more than 110 MHz with programmable C_s arrays without extra power consumption.

3.1.2. Resistor feedback amplifier with I/Q phase calibration

To achieve a high output 1 dB compression point, the last stage adopts resistor feedback amplifier architecture, as shown in Fig. 5, which consumes about 280 μA. To eliminate the phase mismatch between the I and Q paths, the I/Q phase calibration[9] is also implemented in this stage without extra power consumption.

The operational amplifier utilizes two-stage Miller compensated OTA and the Miller capacitors C_C are programmable to maintain the stability of the closed-loop and save power in different gains. The feedback resistors R_f (dashed in Fig. 5) are configured by switches to achieve the proposed gain range and step as listed in Table 1. The cross-coupling resistor R_C arrays are programmable and connected from I (Q) input to Q (I) virtual ground node for phase calibration.

Different from the method in Ref. [9], the phases of the I and Q paths are shifted in the opposite direction synchronously. When the switches SP1 are ON and SP0 OFF, the total phase shift between I and Q path is negative, while SP1 are OFF and SP0 ON, the total phase shift is positive.

We now analyze the condition when SP1 are ON and SP0 are OFF. Let $V_{Iip} = \cos(\omega t)$ and $V_{Qip} = \sin(\omega t)$, then the simplified output voltage of the I and Q paths could be written as

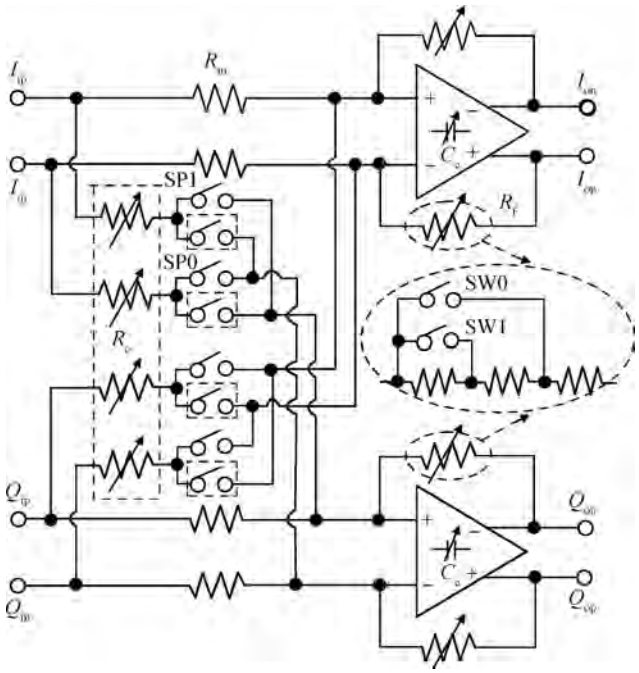

Fig. 5. The resistor feedback amplifier with I/Q phase calibration.

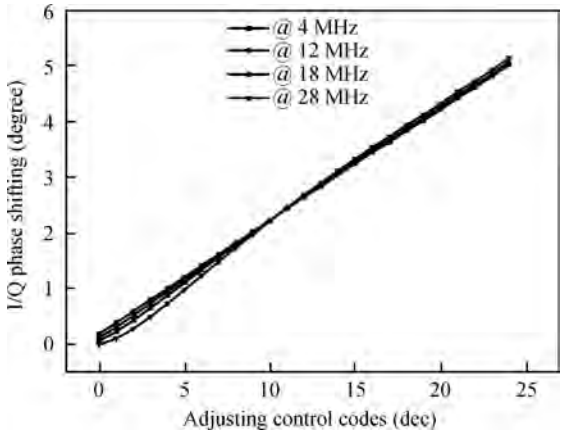

Fig. 6. Phase shift range at different frequencies.

$$V_{\mathrm{Iop}} = \sqrt{G_{\mathrm{I}}^2 + G_{\mathrm{C}}^2}\cos(\omega t - \phi), \quad \tan\phi = G_{\mathrm{I}}/G_{\mathrm{C}}, \tag{2}$$

$$V_{\mathrm{Qop}} = \sqrt{G_{\mathrm{I}}^2 + G_{\mathrm{C}}^2}\sin(\omega t + \phi), \tag{3}$$

where $G_{\mathrm{I}} = R_{\mathrm{f}}/R_{\mathrm{in}}$, $G_{\mathrm{C}} = R_{\mathrm{f}}/R_{\mathrm{C}}$, $G_{\mathrm{I}} \gg G_{\mathrm{C}}$, then $\tan\phi = R_{\mathrm{in}}/R_{\mathrm{C}}$. From Eqs. (2) and (3), the total phase shift $\Delta\theta = -2\phi$.

Using the same method as above, the output voltage of the I and Q paths when SP1 are OFF and SP0 are ON could be written again as

$$V'_{\mathrm{Iop}} = \sqrt{G_{\mathrm{I}}^2 + G_{\mathrm{C}}^2}\cos(\omega t + \phi), \tag{4}$$

$$V'_{\mathrm{Qop}} = \sqrt{G_{\mathrm{I}}^2 + G_{\mathrm{C}}^2}\sin(\omega t - \phi). \tag{5}$$

From Eqs. (4) and (5), the total phase shift $\Delta\theta = +2\phi$.

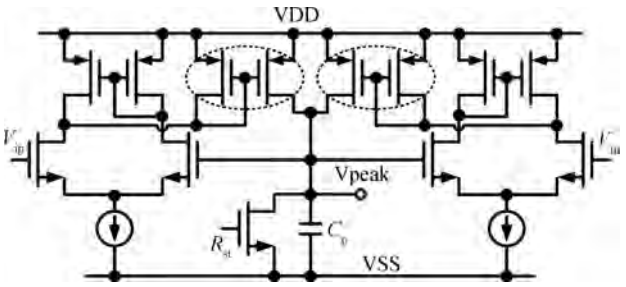

Fig. 7. The differential peak detector.

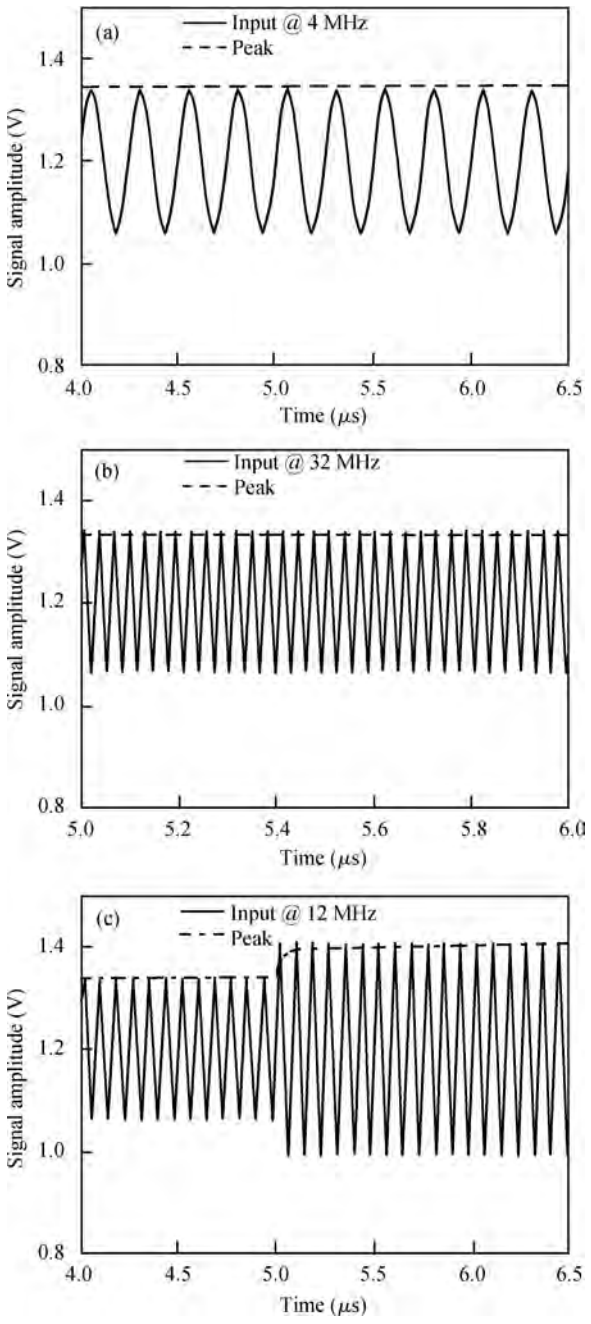

Fig. 8. Signals operating at different frequencies. (a) 4 MHz. (b) 32 MHz. (c) 12 MHz.

For 0.2° phase shifting, $R_{\mathrm{in}}/R_{\mathrm{C}} = \tan(0.1°)$, so $R_{\mathrm{C}} = 573R_{\mathrm{in}}$. The simulated phase shift range at different frequen-

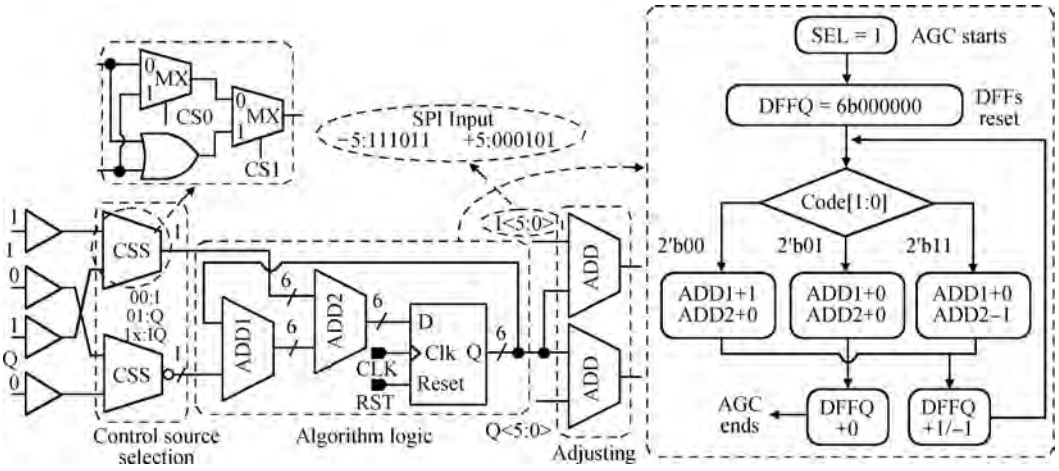

Fig. 9. Block and flowchart of the AGC algorithm logic.

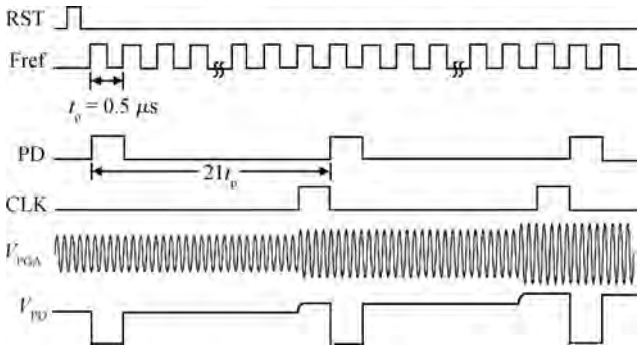

Fig. 10. Timing and signal waveforms of the AGC.

cies is depicted in Fig. 6, which could be configured by the off-chip digital baseband processor through the SPI interface. The total phase shift range is within ±5° with 0.2° accuracy, and the shifting phases only have small differences between different frequencies with good linearity.

3.2. Differential peak detector

Considering that random noise extremely interferes with the positive and negative output, it is unreasonable to catch and hold the maximum amplitude only through the single-end output, thus a differential peak detector[10] is adopted, as shown in Fig. 7, which consumes about 25 μA.

Unidirectional current mirrors (dashed in Fig. 7) are operated as the ideal diode. When the input amplitude V_i is smaller than the peak V_p, the transconductance stage charges the hold capacitor C_p until V_i is nearly equal to V_p, while the current mirrors are shut down to prevent charging C_p. The switch R_{st} shunting with C_p is reset periodically to the ground VSS to discharge C_p. Figure 8 shows the simulated signals of the peak detector operating at frequencies of 4 MHz, 12 MHz and 32 MHz. The peak detector could quickly catch and hold the maximum amplitude even though the input signal is stepped, as shown in Fig. 8(c), and the gaps between V_i and V_p are less than ±9 mV, which are small enough for the threshold comparators.

Table 2. Operations according to input codes.

Amplitude	Code	Operation
$V_p < V_L$	00	+1
$V_L < V_p < V_H$	01	0
$V_p > V_H$	11	−1

3.3. AGC algorithm logic

AGC algorithm logic ensures the maximum output signal of PGAs within the range between V_L and V_H. If the held voltage of differential peak detector V_p is lower than V_L, the AGC algorithm logic will adjust its output data to increase the PGAs gain to further amplify the signal. And in the opposite situation, if V_p is higher than V_H, the gain of PGAs will be reduced. Compare the held output voltage of the differential peak detector with two default threshold voltages V_H and V_L, thus a 2-bit thermometer code is acquired. In this design, an effective linear-adjusting method is adopted to implement the AGC algorithm with a few logic units, which means that the gain of the PGAs is reduced or enhanced by only one step in an adjusting period. In addition, the process will not stop until the signal amplitude is suitable. Table 2 gives the operations according to the output digital codes of the threshold comparators.

To relax the complexity, basic digital logic cells are utilized to implement the AGC algorithm, as shown in Fig. 9, and Figure 10 illustrates the timing of the control signals and the output waveforms of the PGAs and peak detector. The control source selection (CSS) determines the digital input codes of the algorithm logic whether up to the I or Q path according to a 2-bit control code. Assume that the CSS code is equal to 2′b00, which means that the digital input of the AGC algorithm logic depends on the I path. When DFFs are reset initially, the PGAs are provided with the minimum gain of about 10 dB, and meanwhile, the output amplitude of the PGAs is very small after being amplified. Then, captured by the following differential peak detector, the held voltage is compared with threshold voltage V_H and V_L, respectively, to obtain a 2-bit code, which is 2′b00 in this case. Therefore, the output of ADD1 will plus 1 and ADD2 remains constant, then the output data will increase by one at the rising edge of the input clock CLK and the gain of the PGAs will increase by one step of approximately 1 dB.

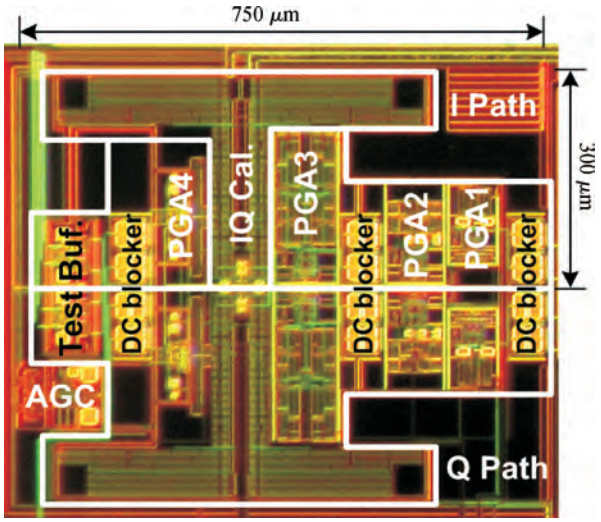

Fig. 11. Die micro photograph.

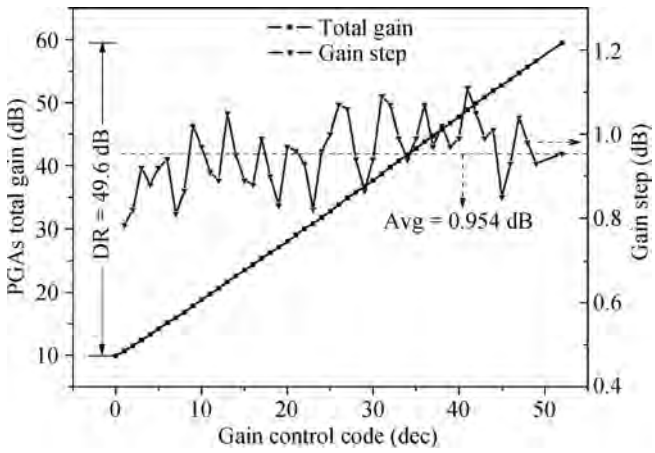

Fig. 12. The measured total gains and step of PGAs.

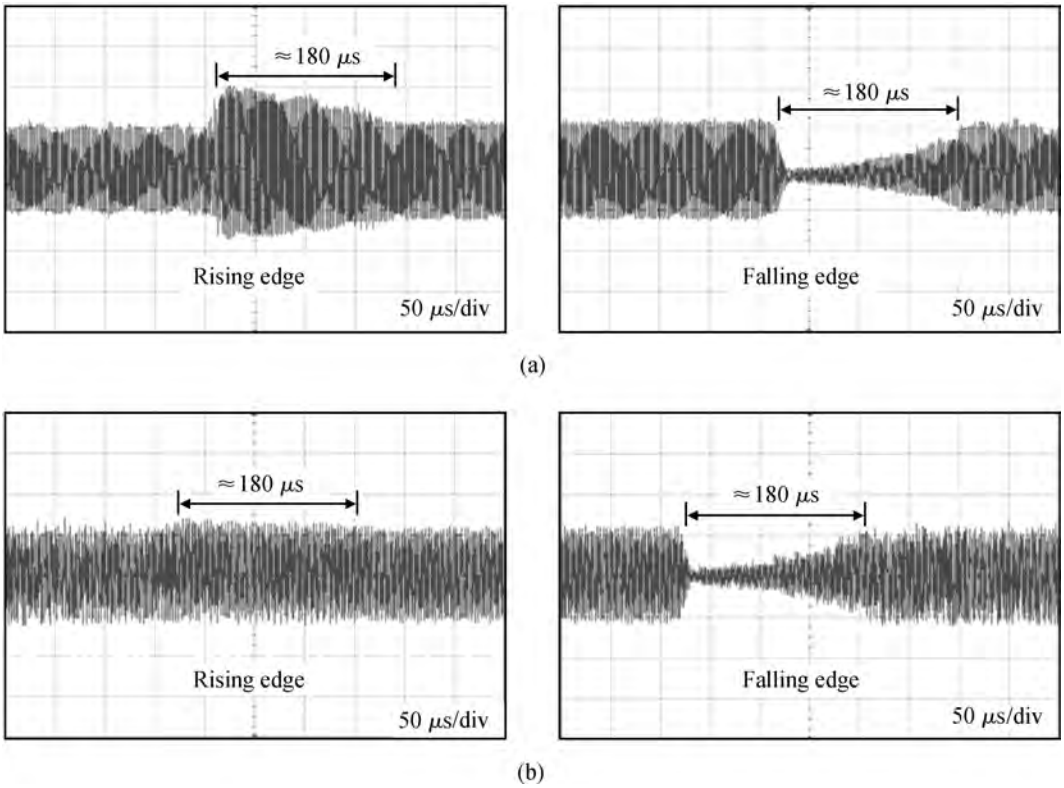

Fig. 13. PGA output signals with AM RF input with AGC at (a) 3.995 MHz and (b) 21.561 MHz.

Then the signal amplitude is enhanced and caught by the peak detector in the next period. This process will continue until the maximum output signal voltage of the PGAs is higher than V_L for the first time. In the case that the input signal suddenly steps into a higher amplitude, the adjusting process will be opposite and finish until the maximum output signal voltage of PGAs is little lower than V_H.

Adopting the complement number form, the addends of two ADDs for adjusting are configured between –5 and +5 by an off-chip digital baseband processor through the SPI interface.

4. Measurement results

The presented AGC has been implemented in 65 nm CMOS, and Figure 11 gives the die micro photograph including both the I and Q paths. A single path occupies an area of 0.23 mm^2. The whole current from a 2.5-V supply is almost 0.8 mA.

A test tone is fed into an RF terminal, and observed at the PGA output. By configuring the local oscillator (LO) and IF complex bandpass filter to operate in GPS L1 N-band (IF 4.092 MHz, BW 2.2 MHz) mode to make analog baseband signal at

Table 3. Performance summary and comparison.

Index	This work	ASSCC'10[2]	JSSC'06[7]
Process	65 nm CMOS	0.18 μm CMOS	0.18 μm CMOS
Architecture	Hybrid	Analog & Hybrid	Analog
Frequency (MHz)‡	27.4	15	16.6
Bandwidth (MHz)	110*	—	18
Gain range (dB)	50	55	40
Output (V_{pp})	0.96–1.28	0.15–0.25	0.5
Settling time (μs)	90–180	900†	—
Power (mA)	0.8 @ 2.5 V	2 @ 1.8 V	5.8 @ 1.8 V
Area (mm^2)	0.23	—	0.56

‡ The maximum frequency of signals after being attenuated by IF filter.
* The simulated frequency response of total PGAs, couldn't be measured due to preceding IF filter.
† Input single-tone signal from –110 to –55 dBm.

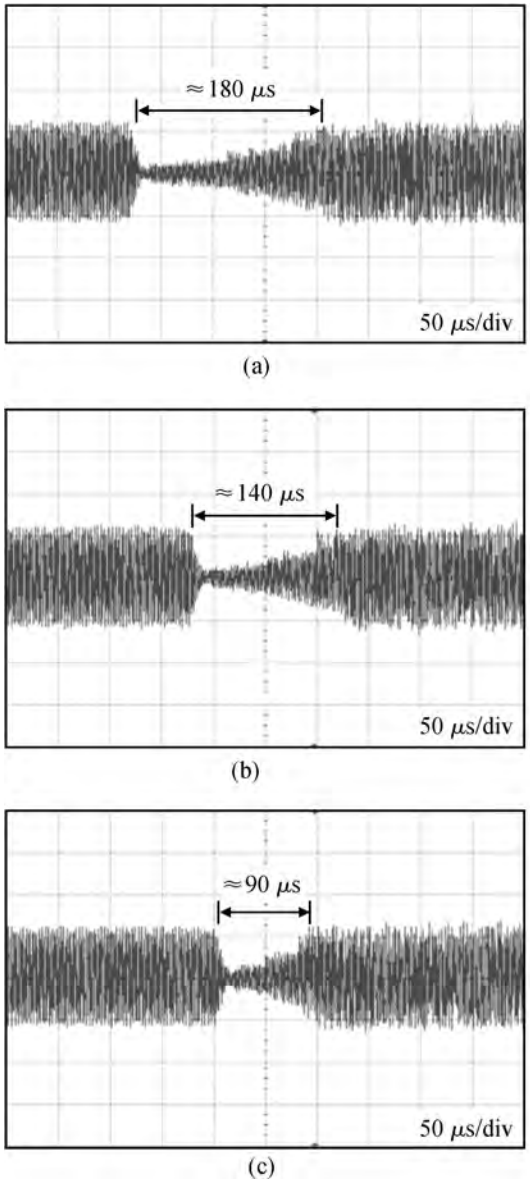

Fig. 14. PGA output signals with programmable reference frequency of (a) 24.6 MHz, (b) 32.7 MHz, and (c) 49.1 MHz.

4.645 MHz from RFA input, the total gains of the PGAs are measured and plotted in Fig. 12. The total gains range from 9.8 to 59.5 dB and the step varies between 0.8 dB and 1.1 dB with an average of 0.95 dB. Then, configuring the LO and IF filter to operate in GPS L2 W-band & GLONASS L2 W-band mode, the bandwidth of the IF filter also satisfies the performance requirements, and the measured baseband amplitude response of several wideband modes has been shown in Ref. [6]. Since there are no independent test ports for IF blocks, the NF and bandwidth of the PGA cannot be directly measured; however, the whole NF of the GNSS receiver is about 2.2 dB in Ref. [6].

Configure the LO and IF filter to operate in GPS L1 N-band & Compass B1 N-band (IF –10.23 MHz, BW 4.2 MHz) mode and the clock generator with output frequency of 24.6 MHz, and make analog baseband signal at 3.995 MHz with –61.9 dBm and 400 Hz 80% AM RF input signal from RFA with measured signal power from –76.7 to –56.6 dBm. Then configure in GPS L2 W-band & GLONASS L2 W-band mode, and make the analog baseband signal at 21.561 MHz with the same method above. Turn the AGC on, and capture the PGAs output signals by using the oscilloscope, as shown in Fig. 13 and the settling time is about 180 μs.

Then configure the clock generator with an output frequency of 32.7 MHz and 49.1 MHz, respectively, and then capture the PGAs' output signals, as shown in Fig. 14. The settling time reduces linearly from 180 to 90 μs with the clock frequency doubling.

The performance of the presented AGC and comparison with other results are summarized in Table 3. This work achieves low power consumption, a short settling time and high output voltage owing to the adoption of hybrid AGC architecture and improved amplifiers.

5. Conclusion

A low-power wideband hybrid AGC loop for a GNSS receiver is implemented in 65 nm CMOS. The PGAs achieve 50 dB gain range from 9.8 to 59.5 dB with an average step of 0.95 dB and its frequency response has little attenuation at the maximum frequency of IF filter. The I/Q phase mismatch is calibrated within the $\pm 5°$ range and 0.2° accuracy in the last PGA stage. The settling time is about 180 μs with 80% AM input from the RFA with measured signal power from –76.7 to –56.6 dBm, while it will reduce to 90 μs with the clock frequency of AGC algorithm logic doubling. A single AGC occupies an area of 0.23 mm^2 and consumes almost 0.8 mA current

from a 2.5 V supply.

References

[1] Ko J, Kim J, Cho S, et al. A 19-mW 2.6-mm^2 L1/L2 dual-band CMOS GPS receiver. IEEE J Solid-State Circuits, 2005, 40(7): 1414

[2] Wang C, Shi C Y, Ye L, et al. A 31 mA CMOS wideband BD-II B2&B3 mode receiver with 55 dB gain dynamic range. IEEE Asian Solid-State Circuits Conference, 2010: 4

[3] Jo J, Lee J, Park D J, et al. A L1-band dual-mode RF receiver for GPS and Galileo in 0.18 μm CMOS. IEEE Radio Frequency Integrated Circuits Symposium, 2008: 21

[4] Chen D P, Pan W J, Jiang P C, et al. A reconfigurable dual-channel tri-mode all-band RF receiver for next generation GNSS. IEEE Asian Solid-State Circuits Conference, 2010: 1

[5] Yu P, Sepke T, Helal B, et al. A 1.2 mm^2 fully integrated GPS radio with Cellular/WiFi co-existence. IEEE Custom Integrated Circuits Conference, 2010: 1

[6] Qi N, Xu Y, Chi B Y, et al. A dual-channel GPS/Compass/Galileo/GLONASS reconfigurable GNSS receiver in 65 nm CMOS. IEEE Custom Integrated Circuits Conference, 2011: 1

[7] Jeon O, Fox R M, Myers B A. Analog AGC circuitry for a CMOS WLAN receiver. IEEE J Solid-State Circuits, 2006, 41(10): 2297

[8] Calvo B, Celma S, Martinez P A, et al. 1.8 V 100 MHz CMOS programmable gain amplifier. IEEE International Symposium on Circuits and Systems, 2006: 1555

[9] Kim S, Jeong M, Kim Y, et al. A complex band-pass filter for low-IF conversion DAB/T-DMB tuner with I/Q mismatch calibration. IEEE Asian Solid-State Circuits Conference, 2008: 474

[10] Cheung H Y, Cheung K S, Lau J. Low power monolithic AGC with automatic DC offset cancellation for direct conversion hybrid CDMA transceiver used in telemetering. IEEE International Symposium on Circuits and Systems, 2001: 391