A high-speed mixed-signal down-scaling circuit for DAB tuners[*]

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Abstract: A high-speed mixed-signal down-scaling circuit with low power consumption and low phase noise for use in digital audio broadcasting tuners has been realized and characterized. Some new circuit techniques are adopted to improve its performance. A dual-modulus prescaler (DMP) with low phase noise is realized with a kind of improved source-coupled logic (SCL) D-flip-flop (DFF) in the synchronous divider and a kind of improved complementary metal oxide semiconductor master-slave (CMOS MS)-DFF in the asynchronous divider. A new more accurate wire-load model is used to realize the pulse-swallow counter (PS counter). Fabricated in a 0.18-μm CMOS process, the total chip size is 0.6×0.2 mm^2. The DMP in the proposed down-scaling circuit exhibits a low phase noise of -118.2 dBc/Hz at 10 kHz off the carrier frequency. At a supply voltage of 1.8 V, the power consumption of the down-scaling circuit's core part is only 2.7 mW.

1. Introduction

With the rapid development of new types of transmission methods, digital audio broadcasting (DAB)[1] has become the best choice to overcome the weaknesses associated with traditional analog radio broadcasting. DAB covers band III (174–240 MHz) and band L (1.452–1.492 GHz). Thus, RF tuners must operate over a wide frequency range to be compatible with DAB. The down-scaling circuit plays an important role in the PLL-type frequency synthesizers used in RF tuners.

A down-scaling circuit mainly includes an analog-circuit-like dual modulus prescaler (DMP) and a digital circuit like the sequential pulse-swallow counter (PS counter). A high-speed DMP is usually made up of two parts: synchronous dividers and asynchronous dividers. Both of which are based on D-flip-flops (DFFs). Optimization of the DMP is focused on the DFF structures in the different parts of the circuit to obtain high speed, low phase noise and lower power consumption[2]. The DMP is utilized to reduce the input operation frequency of the PS counter, while the aim of the PS counter is to acquire a series of continuous division ratios by working together with the DMP. The design of PS counters has always been done using the traditional full custom method. And the work of the design of the part is a difficult part in the PLL design.

This paper presents the design of a down-scaling circuit with low power consumption, and low phase noise and its applications in the PLL-type frequency synthesizers used in DAB tuners. First, the structure of the PLL is introduced. Next, new DMP circuit techniques, such as using an improved D-latch and a kind of improved CMOS MS-DFF, are proposed. Then, a new method realizing the PS counter is introduced and the realization and measurement of the down-scaling circuit are discussed. Finally, conclusions are presented.

2. Circuit design

The architecture of the PLL-type frequency synthesizer used for DAB systems containing the down-scaling circuit based on pulse-swallow topology is shown in Fig. 1. The down-scaling circuit commonly consists of a DMP and a PS counter made up of a counter-M and a counter-A.

The values of A and M are initialized to counter-A and counter-M, and both counters begin to count up. The DMP divides the output by $P+1$ until counter-A counts up to A. At this point it switches over and begins to be divided by P until counter-M counts up to M. Then, the two counters are reset and the DMP switches back to divide-by-$(P+1)$ at the same time. The total division ratio of the down-scaling circuit is

$$N = PM + A. \qquad (1)$$

As shown in Fig. 1, in order to cover the required carriers and operate from an input frequency of approximately 3 GHz, the modulus N of the down-scaling circuit has to be programmed from 6368 to 6903 while the reference frequency is set to be 458 kHz. In the proposed frequency synthesizer, $P = 32$ is selected. According to Eq. (1), M is set to be from 199 to 205, and A is set to be from 0 to 31. In-phase and quadrature (IQ) signals are generated in L-band by a frequency divider (/2) at the output of VCO.
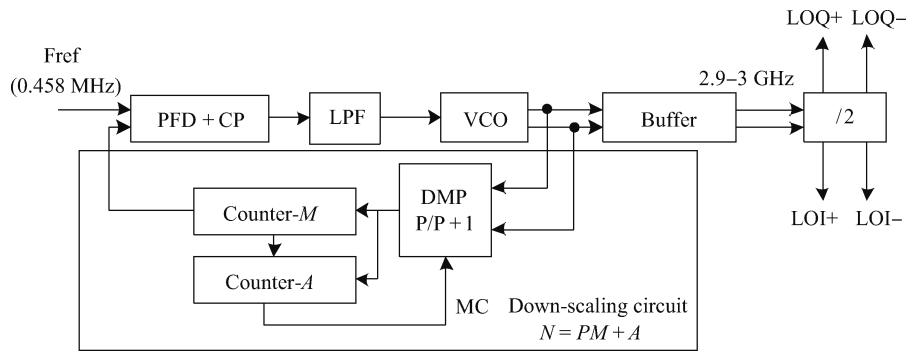
Fig. 1. Block diagram of the frequency synthesizer and the proposed down-scaling circuit.
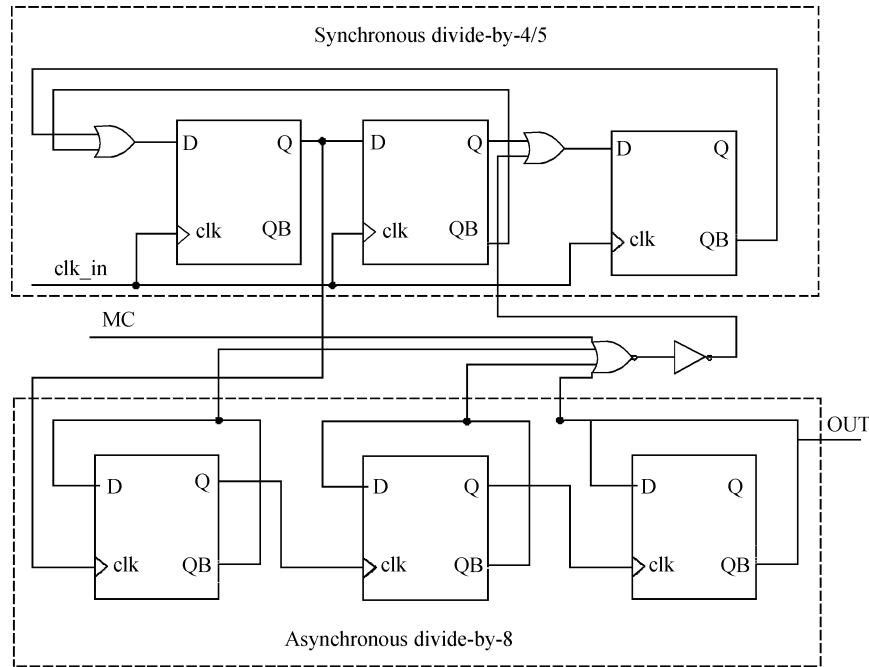

Fig. 2. Block diagram of the proposed 32/33 DMP.

2.1. DMP

The block diagram of the proposed DMP is shown in Fig. 2. It is made up of a synchronous divided-by-4/5 circuit, three asynchronous divided-by-2 circuits made up of several master/slave DFFs, and some control logic gates. The signal MC is used to select the dual modulus division ratio. When the control signal MC is at logic high (MC = 1), the division ratio of the synchronous divided-by-4/5 circuit is equal to 4 and the total division ratio of the DMP is 32. Otherwise, the division ratio of the synchronous divided-by-4/5 is equal to 5, and the total division ratio of the DMP is equal to 33.

The synchronous divided-by-4/5 circuit consists of three DFFs and two OR gates working at the highest frequency and therefore consumes significant power. Since the SCL DFF has features of higher speed, lower consumption, and higher anti-interference ability, the SCL DFFs are used as the basic units of the synchronous divider. A SCL DFF is made up of two D-latches with the same structure, one works as the master-latch, and the other works as the slave-latch. Several techniques are adapted to improve the circuit's performance.

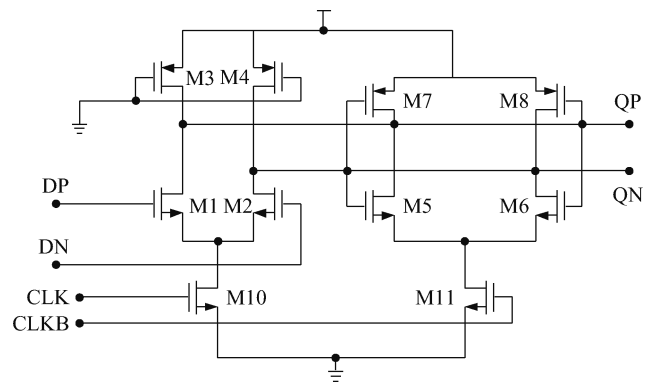First, an improved D-latch is utilized to realize the mas-

Fig. 3. Schematic diagram of the improved D-latch.

ter/slave DFF in the DMP. As shown in Fig. 3, an improved D-latch is utilized to realize the master/slave DFF in the DMP. The proposed latch includes two differential pairs and a cross-coupled pair. The differential pair of M10 and M11 is a clocking pair, while the pair of M1 and M2 is a tracking pair, the cross-coupled pair of M5 and M6 is a holding pair. The master
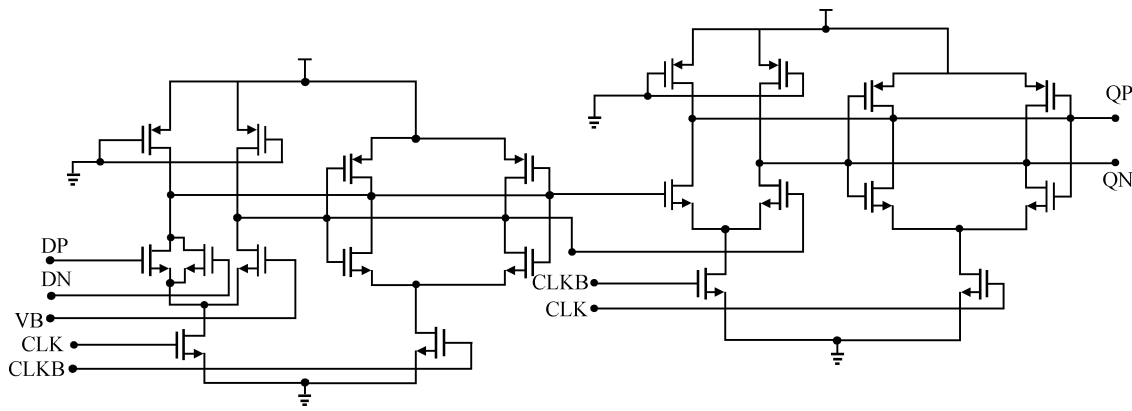
Fig. 4. Schematic diagram of the D-latch architecture integrated with an 'OR' logic.

latch and the slave latch operate in tracking mode and latching mode alternately to accomplish a cycle of DFF. Compared to the conventional D-latch, the gates of load transistors M3 and M4 in the proposed D-latch are connected to the ground instead of the drains in order to the power supply instead of a transistor to lower the power consumption and increase the swing of the output signals. Transistors M7 and M8 are coupled with M5 and M6 in the CMOS configuration, which upgrades the swing of the output as much as possible without prejudice to the operation speed of the circuit. As a result, this kind of DFF can drive the load without a separate boost.

Second, the OR gate is integrated with the master-latch of the DFF to reduce additional gate delays. As shown in Fig. 4, the synchronous divider is commonly made up of SCL DFFs and several logic gates. In this work, the OR gate is integrated with the master-latch of the DFF to reduce additional gate delays[3]. This leads to a higher operating speed as compared to the conventional topology, and at the same time the power consumption is reduced. The voltage VB is biased at the midway between the high and low levels of inputs DP and DN.

The asynchronous divide-by-8 circuit is cascaded with three divide-by-2 circuits which operate at different frequencies, as shown in Fig. 2. Each divide-by-2 circuit must be designed and optimized carefully. Since the asynchronous divide-by-8 works at a lower frequency and high speed is not required, the DFF optimization in this stage is focused on the reduction of power consumption.

In many previous works, the TSPC (true single phase clock) structure was used to realize the DFF in the asynchronous dividers. But the topology of a TSPC has a fatal defect in that it is sensitive to the edge slope of the clock. When the clock-edge is not negligible, conventional TSPC DFFs will be triggered not only by the rising-edge but also by the falling-edge, as illustrated in Fig. 5. The clock edge can be expressed with the formula of

$$T_{rise} = KC_{load}/I_{ss}, \qquad (2)$$

where I_{ss} is the front-drive current, and C_{load} is the load capacitor. If we want to decrease T_{rise}, considering the same C_{load}, the only solution is to increase I_{ss}. So a number of buffers should be added to the dividers in order to speed up the alteration of clock. But the consumption of the circuit will be raised at the same time.
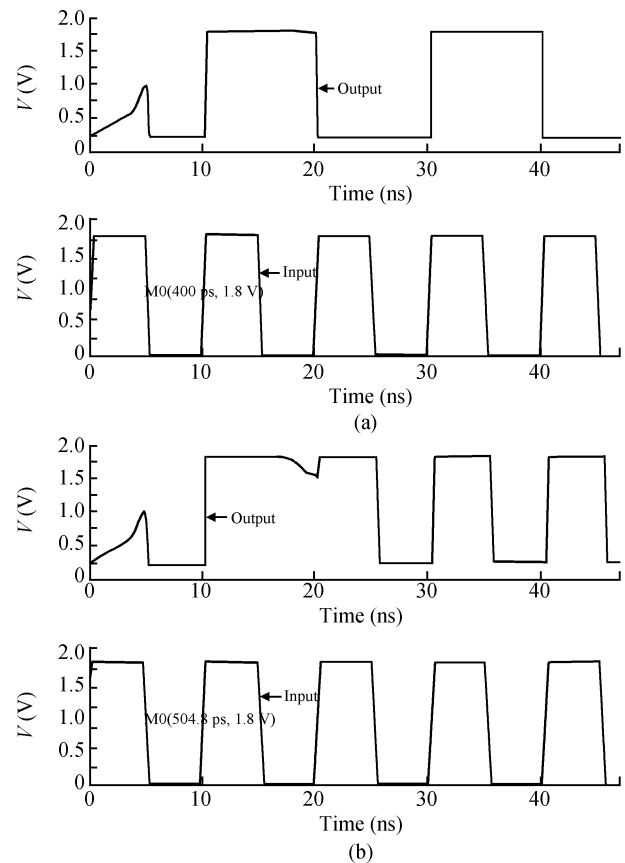

Fig. 5. Simulation results of an asynchronous divide-by-2 circuit based on TSPC DFFs. (a) Precise when clock edge is 400 ps @ TSPC. (b) With error when clock edge is 500 ps @ TSPC.

A kind of improved CMOS MS-DFF is used as the asynchronous divider unit. It is optimized by reducing the positive-feedback of the master-latch of the conventional architecture, as shown in Fig. 6(a)[4]. The schematic diagram of the proposed improved CMOS MS-DFF is illustrated in Fig. 6(b). Compared with the conventional TSPC structure[5], the proposed CMOS MS structure is sensitive to the edge slope of the clock. When they have the same size, the clock-edge-tolerance of the proposed CMOS MS-DFF is nearly as 6 times that of the TSPC DFF, as shown in Fig. 7. So less buffers or no buffer will be used in the CMOS MS-DFF. Meanwhile, the CMOS MS-DFF
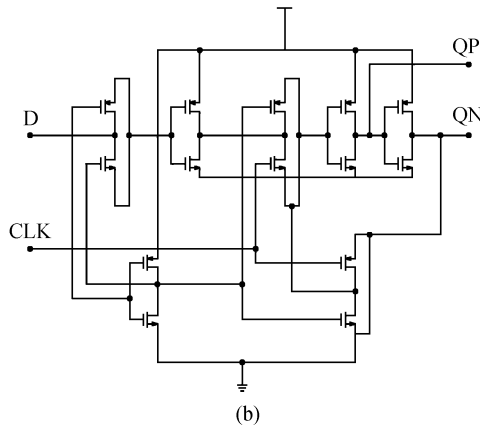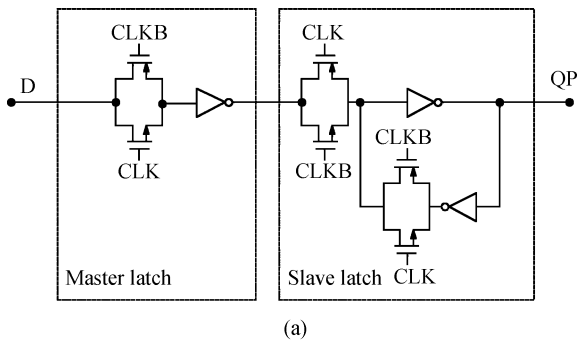
(a)

(b)

Fig. 6. (a) Block diagram of the improved CMOS MS-DFF. (b) Schematic diagram of the proposed improved CMOS MS-DFF.
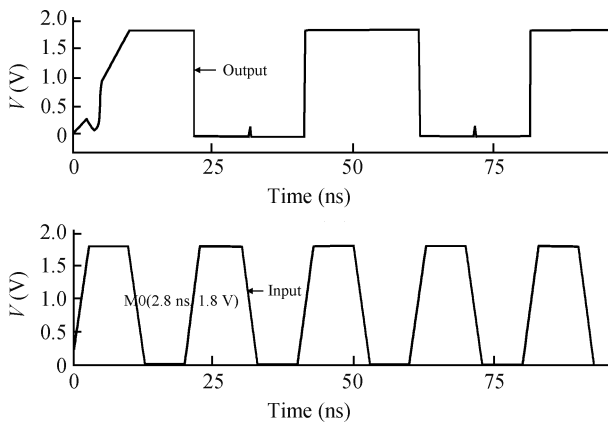

Fig. 7. Simulation results of an asynchronous divide-by-2 circuit based on CMOS MS-DFFs (precise when the clock-edge is 2800 ps).

is a quasi-static structure, which will reduce the power dissipation.

2.2. Programmable frequency divider

In this work, the pulse-swallow counter is designed based on the Artisan 0.18-μm standard cell library. First, the function is realized in Verilog-HDL. Then, a design compiler synthesis tool is used to synthesize the design in the first step. In this step, a wire load model is required for the design compiler to predict the signal delay. The more precise the wire load model is, the more perfect the design that can be obtained in submicron technology, especially in deep submicron. In most cases, however, the linear wire load models are provided by synthesis
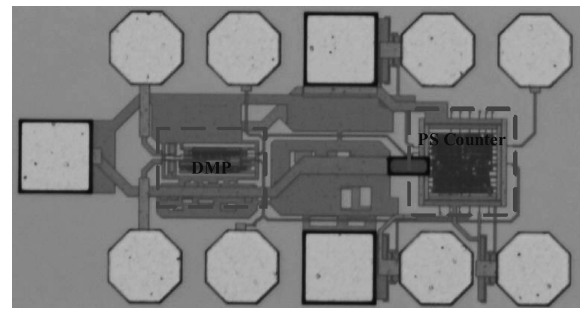

Fig. 8. Chip microphotograph of the down-scaling circuit.

tools, in which the path delay, wire load and wire length have linear relationships with the fan-out of the circuits. Therefore, it is better to generate a precise wire load model to improve the synthesis results for a specific design. In order to create the custom wire load model before detailed synthesis, initial synthesis and initial place and routing are required. In these two steps, the 'initial' means that not much attention is paid to the timing since they are just for creating a practical wire load model. Then, the obtained RC parameters, wire load delay and the results of initial place and routing, are back-annotated to the design compiler. The wire load is created with a command and used to create the custom wire load model in the design compiler. In the custom wire load model, the wire length, resistance, capacitance and area do not have the linear relationships with the fan-out. After obtaining the custom wire load model, the design can be moved to the detailed synthesis. The next steps of the design are place and routing, which are back-end designs and can be completed in Apollo, the Synopsys VLSI implementation program. The last step of the design flow is the verification. In this step, the layout information is imported from Apollo into Cadence Virtuoso, and processes such as the design rule check (DRC) and layout vs. schematic (LVS) can be done to verify the correction of the design. It was finally realized in a 0.18-μm CMOS process.

3. Experimental results

The down-scaling circuit is implemented in a 0.18-μm CMOS process with 1.8-V power supply. The chip microphotograph is shown in Fig. 8. The chip area is about 0.6×0.2 mm^2.

The performance of the down-scaling circuit chip was tested on-wafer on a probe station. The set-up of the measurement system is shown in Fig. 9. The input signals are generated by an ultra-high-speed signal generator. The output signals are measured by using a high-speed oscilloscope and a spectrum analyzer.

The measurement of the chip includes two parts.

In the first part of the measurement, the part of DMP was tested alone. The results indicate that the proposed DMP can divide accurately in the range from 10 MHz to 3.5 GHz. Figure 10 shows the measured spectrum of the proposed DMP on a 50-Ω load of measurement equipment at the division ratio of 33 when the input signal is at 3 GHz. It can be seen from the figure that the center frequency is 90.9 MHz. It can be seen that the phase noise is as low as –118.2 dBc/ Hz at 10 kHz off the
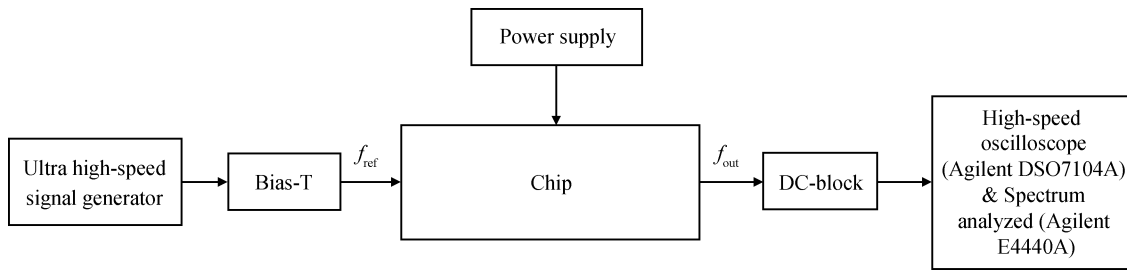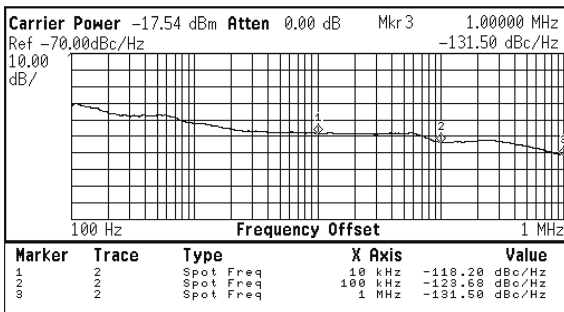
Fig. 9. The measurement sysytem architecture.

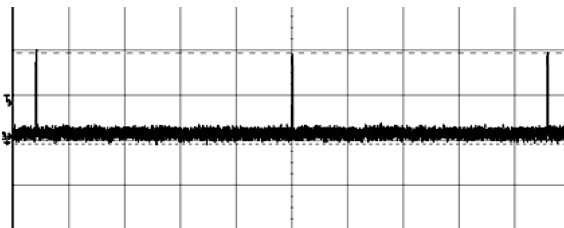Fig. 10. Measured spectrum of the DMP's output signal.

Fig. 11. Measured output signal of the down-scaling circuit (x axis, 500 ns/div).

Table 1. Performance comparison with other published works.

Reference	Tech. (μm)	f_{max} (GHz)	Power supply (V)	Division ratio
Ref. [6]	0.18	3.5	1.8	8–510
Ref. [7]	0.09	3.5	1	24–27
Ref. [8]	0.18	2.4	1.8	1024–1048
Ref. [9]	0.18	2.5	1.8	573–575
This work	0.18	3.5	1.8	6368–6903

show that the phase noise of the DMP's output signal is only −118.2 dBc/Hz at 10-kHz off the center frequency. The power consumption of the down-scaling circuit's core part is only 2.7 mW under a 1.8-V power supply. The experimental results also indicate that the DMP works well with the PS counter in the down-scaling circuit. The performance of the proposed circuit is summarized in Table 1 with several recently published works for comparison. All of the above shows that the proposed DMP and the down-scaling circuit are suitable for application in DAB tuners.

center frequency.

In the second part of the measurement, the down-scaling circuit including the DMP and the PS counter was tested. The core part of the down-scaling circuit only draws 1.5 mA from the power supply of 1.8 V. Figure 11 shows the measured output signal of the down-scaling circuit with an input signal of 3 GHz while the total division ratio is set to be 6884. The measured output frequency is 436 kHz. The measurement results show that the PS counter can work well with the DMP as desired.

4. Conclusions

A high-speed mixed-signal down-scaling circuit for DAB tuners has been proposed in this paper. In the synchronous divider of the DMP, an improved D-latch is utilized to realize the master/slave D-flip-flop (MS-DFF) and the OR gate is integrated with an improved D-latch to reduce additional gate delays. In the asynchronous divider of the DMP, a kind of improved CMOS MS-DFF is used as the unit to optimize the topology. The DMP is integrated with the PS counter to realize the down-scaling circuit. A new more accurate wire-load model is used to realize the PS counter. The measured results

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