A 10-Gb/s inductor-less variable gain amplifier with a linear-in-dB characteristic and DC-offset cancellation

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Abstract: This paper presents a broadband inductor-less variable gain amplifier (VGA) with a linear-in-dB gain control characteristic and DC-offset cancellation. The proposed VGA is composed of a variable gain block, an exponential voltage generator, a DC-offset canceller with common-mode voltage correction, and a gain peaking block. To achieve the broad band and reduce the chip area, the gain peaking block employs an inductor-less gain peaking scheme to compensate the high frequency gain drop of the variable gain block and the DC-offset canceller. The VGA fabricated in 0.13 μm SiGe BiCMOS technology achieves a 3-dB bandwidth of 7.5 GHz and a variable gain range from –10 to 30 dB. Due to the inductor-less design, the die area is only 0.53 × 0.27 mm^2 which is the smallest among other similar reported works. At 10-Gb/s, the VGA consumes 50 mW power from a single 1.2 V supply and exhibits an output data jitter of less than 30 ps_{pp}.

Key words: VGA; broad band; DC-offset cancellation; gain peaking
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1. Introduction

A variable gain amplifier (VGA) is the key building block in most communication systems. According to the strength of the incoming signal, the VGA adjusts its gain to avoid saturation of the system. Hence, it is indispensible for a system to attain a wide dynamic range and an optimum linearity.

With the increasing demands for huge data traffic in the internet, multimedia communication and mm-wave imaging systems, the VGA is required to achieve a broad bandwidth. Broadband techniques using inductor peaking[1] occupy a large area. While the methods of inductor-less bandwidth enhancement, such as the Cherry–Hooper amplifier[2] and transimpedance circuit peaking[3], save the chip area but stack too many transistors in the same current branch. These inductor-less techniques are complex and not suitable for low power supply applications. Therefore, a broad band VGA that can operate at a low supply voltage is imperative.

In this paper, a broadband inductor-less VGA with a linear-in-dB characteristic and DC-offset cancellation is presented. The proposed VGA consists of four stages. The flat and broad bandwidth is guaranteed through compensating the high frequency gain drop in the first two stages by the gain peaking of two cascaded post stages, called the gain peaking block. This bandwidth enhancement scheme relaxes the bandwidth requirement of a single amplifier and allows realizing circuits in a simple way that could work under a low supply voltage condition.

2. Architecture

The architecture of a VGA is presented in Fig. 1. A cascade of gain stages is employed to achieve the broad band necessary for this low supply voltage condition. The first stage is a variable gain block for gain adjustment which provides a variable gain range from −40 to 0 dB. The exponential voltage generator converts the gain control voltage V_{ctrl} to differential exponential control voltages, which control the gain of the VGA to realize the linear-in-dB gain-control characteristic in decibel scale. The second gain stage is the DC-offset canceller. The common-mode voltage correction is introduced to the DC-offset canceller for achieving an appropriate common-mode voltage to ensure the dynamic range of the following stages. The gain peaking block follows the DC-offset canceller. It consists of two stages of fixed gain amplifiers. To broaden the bandwidth, the inductor-less active feedback scheme is adopted for the two fixed gain amplifiers. The inherent high

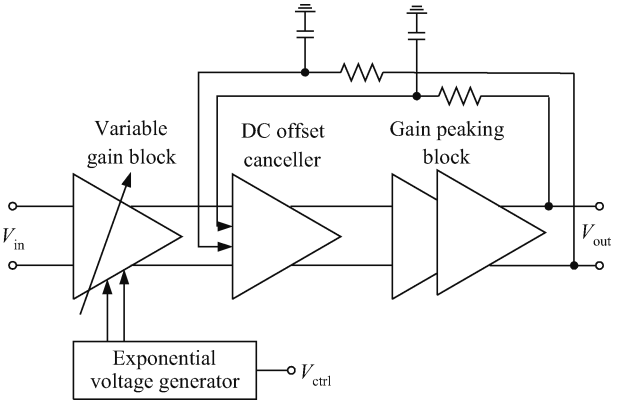

Fig. 1. Architecture of VGA.

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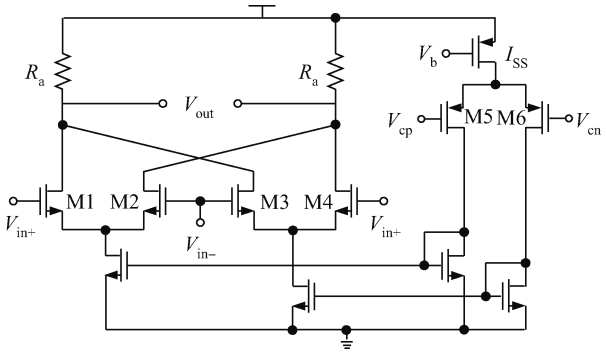


Fig. 2. The circuit of variable gain block.

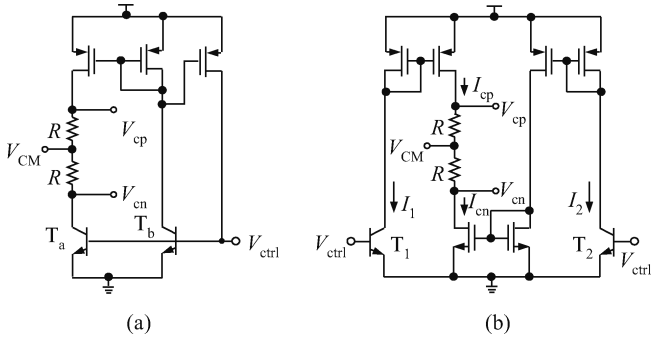


Fig. 3. Exponential voltage generator. (a) Conventional structure. (b) Proposed structure.

frequency gain peaking in this scheme compensates the gain drop of the variable gain block and DC-offset canceller in high frequency, hence attainting excellent gain flatness over the frequency range. The simulated gain of the gain peaking block is 30 dB with about 5 dB gain peaking at 8.5 GHz. The DC coupling topology adopted is to ensure an optimum jitter performance.

3. Circuit design

3.1. Variable gain block and exponential voltage generator

The variable gain block and the exponential voltage generator realize the linear-in-dB characteristic between the gain and the control voltage. The linear-in-dB characteristic achieves a constant gain settling time and permits the AGC loop's bandwidth to be maximized for fast signal acquisition while maintaining stable overall operating conditions[4].

Figure 2 shows the circuit of the variable gain block. The folded Gilbert structure[5] is adopted for this block dependent on the broad bandwidth and low power supply consideration. The relationship between the inputs and outputs can be given as:

$$\begin{aligned} V_{\text{out}} &= (g_{\text{m1,2}} - g_{\text{m3,4}})R_{\text{a}}(V_{\text{in+}} - V_{\text{in-}}) \\ &= \sqrt{\frac{\mu_{\text{n}}C_{\text{ox}}\,(W/L)_{1\sim4}}{2I_{\text{SS}}}}\,g_{\text{m5,6}}R_{\text{a}}(V_{\text{cp}} - V_{\text{cn}})(V_{\text{in+}} - V_{\text{in-}}), \end{aligned} \tag{1}$$

where V_{cp} and V_{cn} are generated by the exponential voltage generator and they manipulate the gain of the variable gain block. Figure 3(a) depicts a conventional exponential voltage generator[5]. T_a and T_b are vertical NPN BJTs and generate the exponential current. However, T_a is saturated due to the low collector voltage in a 1.2 V supply voltage, which results in a non-exponential relationship between the control voltage and the collector current of T_a. Therefore a symmetrical exponential voltage generator needs to be developed to ensure that both BJTs work in the active region, as shown in Fig. 3(b). In the proposed structure, no BJT is used in the output branch to avoid the exponential voltage generator from being saturated by the output voltage. Figure 4 shows the simulated results of V_{cp} and V_{cn} in the conventional and proposed structure, respectively.

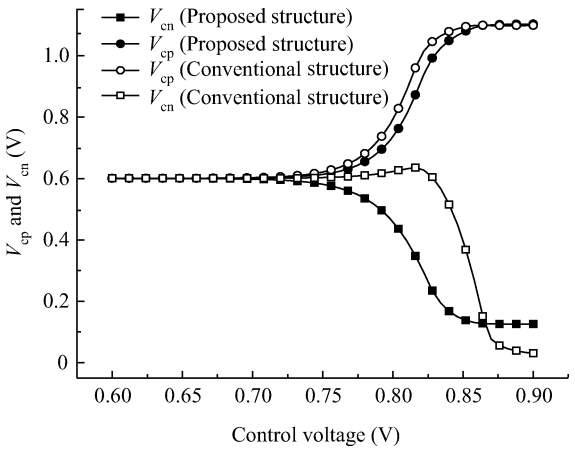


Fig. 4. Simulated results of V_{cp} and V_{cn} versus control voltage (V_{ctrl}) in proposed and conventional structure respectively.

It is obvious that V_{cp} and V_{cn} are asymmetrical in the conventional structure while symmetrical in the proposed one.

As shown in Fig. 3(b), T_1 and T_2 both operate in the active region. The difference between V_{cp} and V_{cn} can be expressed as follows:

$$V_{\text{cp}} - V_{\text{cn}} = R(I_{\text{cp}} + I_{\text{cn}}) = 2RI_{\text{s}} \exp\frac{V_{\text{ctrl}}}{V_{\text{T}}}, \tag{2}$$

where I_{s} is the saturation current and V_{T} is the thermal voltage. Then, substituting Eq. (2) into Eq. (1):

$$\text{Gain (dB)} = K_1 + K_2 V_{\text{ctrl}}, \tag{3}$$

where

$$K_1 = 20\lg\left[\sqrt{\frac{\mu_{\text{n}}C_{\text{ox}}\,(W/L)_{1-4}}{2I_{\text{SS}}}}\,g_{\text{m5,6}}R_{\text{a}}2RI_{\text{s}}\right],$$

$$K_2 = \frac{20\lg e}{V_{\text{T}}}.$$

From Eq. (3), a linear relationship between the amplifier gain and the control voltage is shown in decibel scale.

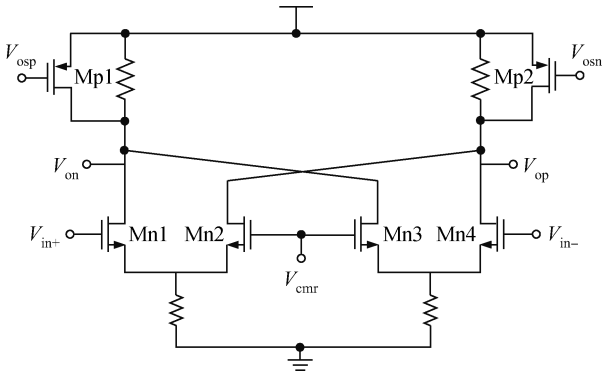


Fig. 5. Circuit of a DC-offset canceller.

3.2. DC-offset canceller

In the direct-conversion receivers, DC offset is a critical problem, which is introduced mainly by self-mixing in the mixer, I/Q mismatch, and even order distortion. Meanwhile, for high speed applications, the lack of a common-mode feedback scheme that shrinks the bandwidth due to the parasitic impedance results in the drift of the common voltage of signals, which deteriorates the dynamic range of the following amplifiers.

The proposed DC-offset canceller introduces the f_T doubler scheme. This structure cancels the DC offset voltage and at the same time corrects the common-mode voltage of the outputs to a desired level. Figure 5 shows the circuit of the proposed DC-offset canceller. Mp1 and Mp2 remove the offset voltage according to the feedback DC voltages of outputs. Mn1,4 and Mn2,3 are the high speed signal input, and the common-mode voltage input, respectively.

3.3. Gain peaking block

To enhance the gain and broaden the bandwidth, a gain peaking block is introduced following the DC-offset canceller. This block consists of two stages of fixed gain amplifiers. Without using a large area on the chip inductors for gain peaking[1], a third-order gain stage with an active feedback structure[6] is adopted for each fixed gain amplifier, as shown in Fig. 6(a). This kind of fixed gain amplifier is suitable for low supply voltage applications and has an associated high frequency gain peaking which compensates the inherent gain drop of the variable gain block and DC-offset canceller in the high frequency. The generic block diagram of this scheme is illustrated in Fig. 6(b) where G_1, G_2, and G_3 are the gain cells and G_f is the feedback cell. The overall transfer function can be given as:

$$H(s) = \frac{G_m^3(s)R^3}{(1+sRC)^3 + G_m^2 G_{mf} R^3}, \tag{4}$$

where R and C are resistive and capacitive loads of the differential pairs, respectively, and the transconductances of the cells ($G_{1,2,3}$ and G_f) are represented by G_m and G_{mf}. The associated peaking frequency (ω_{peak}) could be derived by calculating:

$$\left.\frac{d(H(j\omega))}{d\omega}\right|_{\omega=\omega_{peak}} = 0. \tag{5}$$

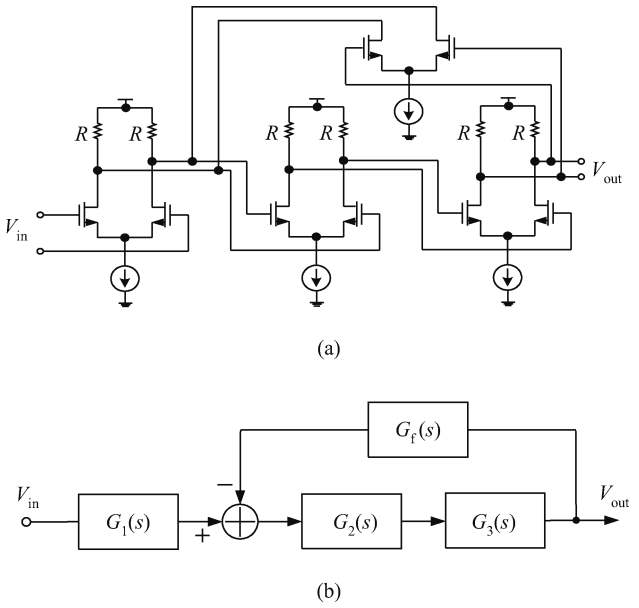


Fig. 6. (a) Circuit of the conventional third-order gain stages with active feedback. (b) The generic block diagram of the conventional structure.

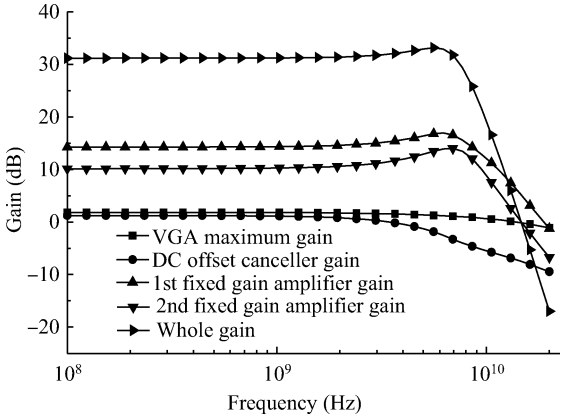


Fig. 7. The simulated frequency response of the amplifier gain.

The simulated frequency response of the cascaded gain cells is shown in Fig. 7. The peaking gain of the two fixed gain amplifiers compensates the gain drop from the first two stages, and the VGA achieves a broad bandwidth with excellent gain flatness. Besides, the stability problem of each fixed gain amplifier also needs to consider the feedback structure. The simulated open-loop phase margin of each fixed gain amplifier is about 45 as shown in Fig. 8.

4. Measurement results

The proposed broad bandwidth VGA was implemented in IHP's 0.13-μm SiGe BiCMOS process. This VGA occupies 0.53×0.27 mm^2 area, as shown in Fig. 9. It consumes 50 mW with 1.2 V power supply. The 3-dB bandwidth is from 200 kHz to 7.5 GHz.

The transient response of the VGA is measured by using a pseudo-random bit sequence (PRBS) signal at 10 Gb/s. Figure 10 depicts the measured linear-in-dB gain-control charac-

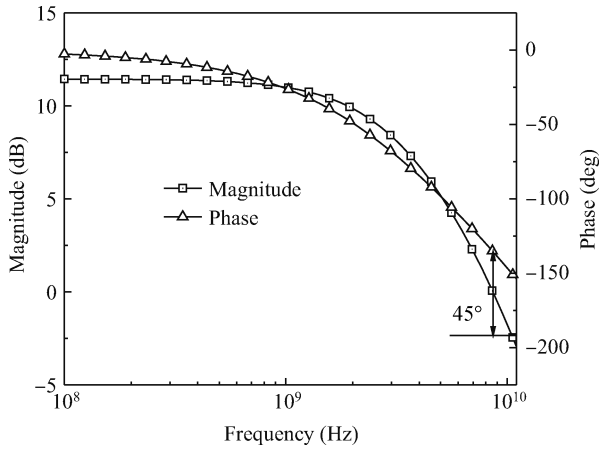


Fig. 8. The open loop frequency response of each fixed gain amplifier.

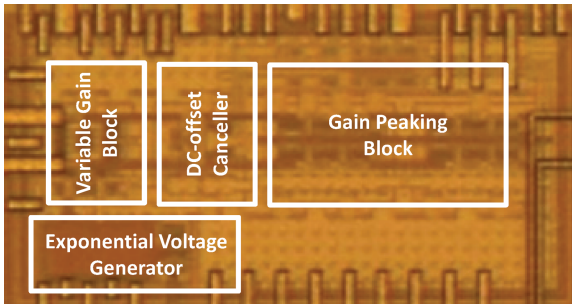


Fig. 9. Micrograph.

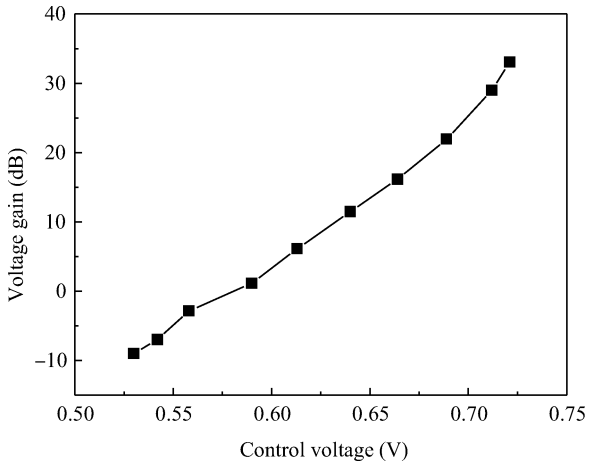
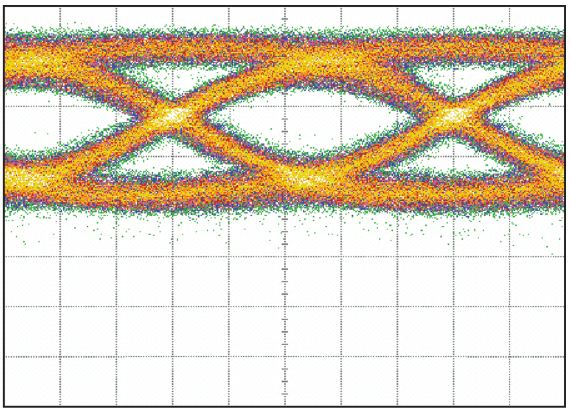


Fig. 10. Measured gain versus control voltage.

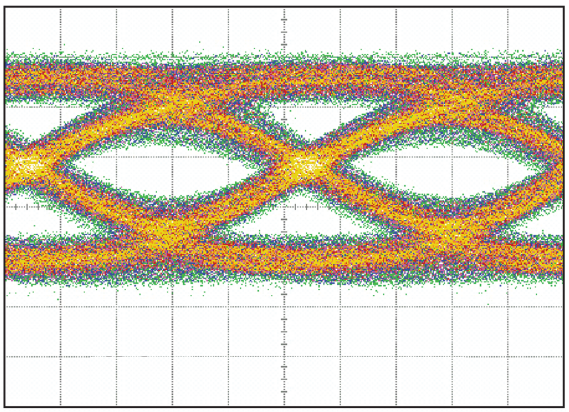
teristic. The variable gain range is from –10 to 30 dB. The proposed exponential voltage generator ensured this linear relationship between the control voltage and the gain at 1.2 V supply voltage.

Figure 11 shows the single-end output eye diagrams with 10 Gb/s $2^{15} - 1$ PRBS for input signal with 5 mVpp and 100 mVpp, respectively.

Table 1 summarizes the performance of this work and compares it with other published broad band VGA. Due to the structure gain compensation scheme, this work broadens the bandwidth to 7.5 GHz and simultaneously saves chip area dramatically as compared to prior studies[5, 7].



(a) $V_{in} = 5\ mV_{pp}$



(b) $V_{in} = 100\ mV_{pp}$

Fig. 11. Measured 10 Gb/s $2^{15} - 1$ PRBS data single-ended output eye diagrams. H scale: 20 ps/div, V scale: 66.3 mV/div in (a), 60.9 mV/div in (b).

Table 1. Measurement results and benchmarking.

Design	Ref. [5]	Ref. [7]	This work
Technology	0.18 μm CMOS	0.18 μm CMOS	0.13-μm SiGe BiCMOS
Tuning gain (dB)	50 (–16 to 34)	20 (0–20)	40 (–10 to 30)
Dynamic range (dB)	35	27.8	30
Data rate (Gb/s)	3.125	5	10
BW (GHz)	0.0004–2	4	0.0002–7.5
Peak-to-peak jitter (ps)	< 95	44.4	30
Inductors	N	Y	N
Power (mW)	40	55	50
Power supply (V)	1.8	1.8	1.2
Area (mm^2)	1.0 × 0.7	1.85 × 0.45	0.53 × 0.27

5. Conclusion

A 10-Gb/s inductor-less variable gain amplifier with a linear-in-dB characteristic and DC-offset cancellation has been demonstrated in this work. The scheme of internal-stages gain

peaking compensation broadens the bandwidth to 7.5 GHz and ensures a flat gain over a wide frequency range. The inductorless design reduces the chip area to 0.53×0.27 mm^2, which is the smallest among other similar prior studies. The measured peak-to-peak jitter of the output is lower than 30 ps_{pp} with 10 Gb/s 2^{15}-1 PRBS input signal The proposed VGA is workable at a low supply voltage and suitable for the high speed applications.

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