A low on-resistance SOI LDMOS using a trench gate and a recessed drain*

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Abstract: An integrable silicon-on-insulator (SOI) power lateral MOSFET with a trench gate and a recessed drain (TGRD MOSFET) is proposed to reduce the on-resistance. Both of the trench gate extended to the buried oxide (BOX) and the recessed drain reduce the specific on-resistance ($R_{\rm on,sp}$) by widening the vertical conduction area and shortening the extra current path. The trench gate is extended as a field plate improves the electric field distribution. Breakdown voltage (BV) of 97 V and $R_{\rm on,sp}$ of 0.985 m$\Omega\cdot$cm^2 ($V_{\rm GS} = 5$ V) are obtained for a TGRD MOSFET with 6.5 μm half-cell pitch. Compared with the trench gate SOI MOSFET (TG MOSFET) and the conventional MOSFET, $R_{\rm on,sp}$ of the TGRD MOSFET decreases by 46% and 83% at the same BV, respectively. Compared with the SOI MOSFET with a trench gate and a trench drain (TGTD MOSFET), BV of the TGRD MOSFET increases by 37% at the same $R_{\rm on,sp}$.

Key words: trench gate; recessed drain; on-resistance; breakdown voltage

DOI: 10.1088/1674-4926/33/7/074005 **EEACC:** 2560B; 2560P

1. Introduction

Silicon-on-insulator technology offers inherent advantages of high reliability, high speed, low power loss, and superior isolation[1, 2]. The SOI power LDMOS has been widely used in smart power IC's, but there is a Si-limit of the specific on-resistance ($R_{\rm on,sp}$) $\propto$ BV$^{2.5}$ between $R_{\rm on,sp}$ and the breakdown voltage (BV) for lateral power devices. This trade-off between $R_{\rm on,sp}$ and BV is thus the main issue for power MOSFETs[3, 4]. RESURF technology has been widely used in order to improve the trade-off[5, 6]. The channel resistance accounts for a large proportion in $R_{\rm on,sp}$ for medium- and low-voltage devices. A trench gate MOSFET can reduce channel resistance, eliminate the junction field effect transistor (JFET) effect and widen the vertical conduction area, resulting in a reduced $R_{\rm on,sp}$[7–9]. The trench drain can further reduce $R_{\rm on,sp}$ by widening the vertical conduction area and shortening the current path[10, 11].

We propose an SOI lateral MOSFET with a recessed drain and trench gate extended to the BOX. The trench gate plays two roles: the gate of MOSFET, and the dielectric isolation trench between the high voltage device and low voltage circuitry in the integrated circuitry. The P-type top layer is used to form the double RESURF and thus enhance the drift doping concentration. Then the $R_{\rm on,sp}$ further reduces. There are two merits compared with the conventional SOI LDMOSFET: (1) it dramatically reduces $R_{\rm on,sp}$ owing to the recessed drain, the trench gate and the double RESURF technology; (2) it removes the additional dielectric isolation trench which is needed in conventional SOI power integrated circuits.

2. Device structure and mechanism

Figure 1 shows the schematic cross section of the TGRD MOSFET. The TGRD MOSFET features a trench gate extended to the BOX and a recessed drain. In order to maintain a high BV, the drain does not extend to the BOX while emerging an N-layer below the drain. The doping concentration of the N-layer is optimized to reduce $R_{\rm on,sp}$ further. So the $R_{\rm on,sp}$ of the TGRD MOSFET is ultra low and the BV of the TGRD MOSFET is almost the same as that of a conventional MOSFET. $N_{\rm d}$

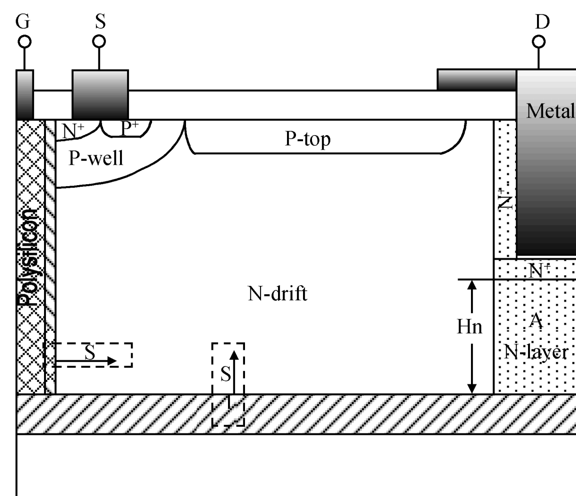

Fig. 1. Schematic cross section of the TGRD MOSFET.

* Project supported by the National Natural Science Foundation of China (Nos. 60976060, 61176069), the National Key Laboratory of Analog Integrated Circuit (NLAIC), China (No. 9140C090304110C0905), and the State Key Laboratory of Electronic Thin Films and Integrated Devices, China (No. CXJJ201004).

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Received 6 January 2012, revised manuscript received 19 February 2012 © 2012 Chinese Institute of Electronics

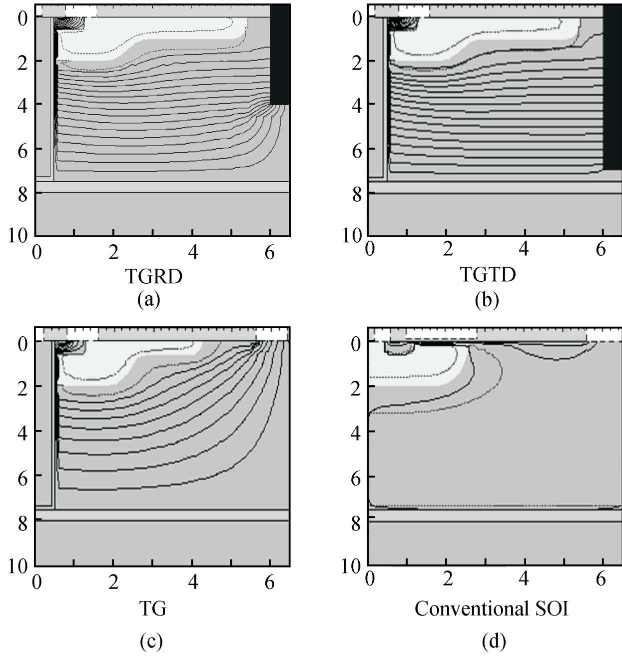

Fig. 2. Current flowline contours for (a) TGRD MOSFET (0.985 m$\Omega\cdot$cm^2), (b) TGTD MOSFET (0.931 m$\Omega\cdot$cm^2), (c) TG MOSFET (1.84 m$\Omega\cdot$cm^2), and (d) conventional MOSFET (5.93 m$\Omega\cdot$cm^2) (2×10^{-6} A/μm/contour with the optimal $N_{\rm d}$ for each device and the same cell pitch of 6.5 μm).

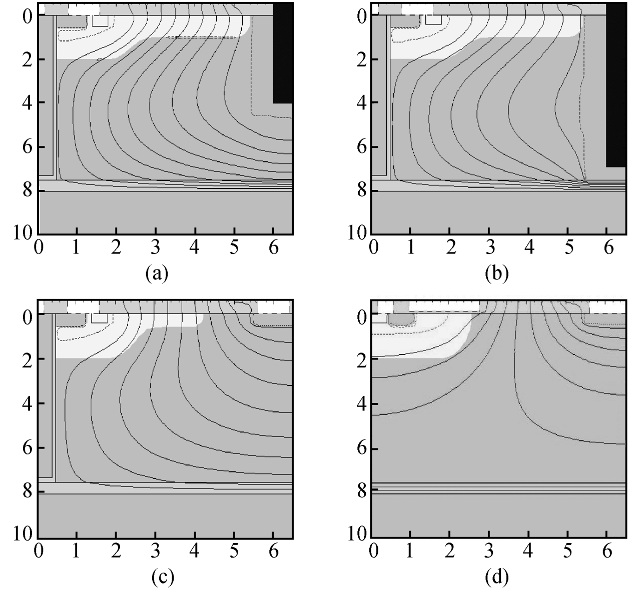

Fig. 3. Equi-potential contours at breakdown voltage for (a) TGRD (97 V), (b) TGTD (71 V), (c) TG (102 V), and (d) conventional MOSFET (91 V) (10 V/contour. The same structural parameters as those in Fig. 2).

and $N_{\rm n}$ are the doping concentrations of the N-drift and the N-layer (A region in Fig. 1), respectively. $H_{\rm n}$ is the thickness of the N-layer.

For the TGRD MOSFET, the P-top layer in the N-drift forms the double RESURF structure to reduce $R_{\rm on,sp}$. The multiple-directional depletion regions are caused and strengthened by two MIS-like structures in the dashed rectangle of Fig. 1 (the arrows show the depleting direction in the "S" layers of the MIS). It leads to an enhanced RESURF effect. The recessed drain widens the vertical conduction area and reduces the extra current path. The trench gate can reduce the on-resistance of the drift region. In the on-state, in addition to the vertical inversion layer channel, a long electron accumulation layer is formed beside the extended gate in the N-drift. All of these reduce $R_{\rm on,sp}$.

3. Results and discussion

Figure 2 shows the current flowline contours for a TGRD MOSFET, a TGTD MOSFET, a TG MOSFET and a conventional MOSFET. The TGTD MOSFET or the TGRD MOSFET minimizes the $R_{\rm on,sp}$ by shortening the extra current path and spreading the conduction area by the trench gate and a trench/recessed drain. The two kinds of devices have almost the same $R_{\rm on,sp}$ which is obviously lower than that of the TG MOSFET and conventional MOSFET. In simulation, there are the same device dimensional parameters for several structures as follows: the thicknesses of top silicon ($T_{\rm s} = 7.5$ μm) and buried oxide layer ($T_{\rm ox} = 0.5$ μm), the length of drift region ($L_{\rm d} = 3.5$ μm) as well.

Figure 3 shows the equi-potential contours of four different device structures. Compared with a TGTD MOSFET, the TGRD MOSFET has more equi-potential contours in the top Si layer below the drain. The field strengths are thus higher than zero, as illustrated in Figs. 3(a) and 3(b). The BV of the TGRD MOSFET can therefore reach 97 V, which is almost the same as a TG MOSFET and a conventional MOSFET.

Figure 4 shows the electric field and potential distributions on the surface and under the drain of four different devices structures. Although the electric field strength in the BOX of the TGTD MOSFET is higher than others, the electric field strength in the SOI layer and the voltage drop in the SOI layer below the drain region of the TGTD MOSFET are the lowest, as illustrated in Figs. 4(b) and 4(c). The BV of the TGTD MOSFET is thus the lowest. Relatively, the BV of the TGRD MOSFET is increased by smoothing the surface electric field distribution in Fig. 4(a) and enhancing the electric field strength in the BOX in Fig. 4(b). Therefore, the BV of the TGRD MOSFET is almost the same as that of the TG MOSFET, which is slightly higher than that of a conventional MOSFET.

The values of half-cell pitch, optimized $N_{\rm d}$, BV, $R_{\rm on,sp}$ and FOM (FOM $=$ BV$^2/R_{\rm on,sp}$) for the TGRD MOSFET, the TG MOSFET, the TGTD MOSFET and a conventional MOSFET are given in Table 1, respectively. The recessed drain decreases the $R_{\rm on,sp}$ from 1.84 m$\Omega\cdot$cm^2 of the TG MOSFET to 0.985 m$\Omega\cdot$cm^2 of the TGRD MOSFET at the same BV and $V_{\rm GS}$ (5 V) with the same cell pitch of 6.5 μm. The FOM of the TGRD MOSFET is higher than those of the other structures, as shown in Table 1.

Figures 5 and 6 show the influences of $N_{\rm d}$, $N_{\rm n}$ and $H_{\rm n}$ on BV and $R_{\rm on,sp}$. Figure 5 shows the trade-off between the optimized BV and $R_{\rm on,sp}$ for MOSFETs with different $N_{\rm d}$ and $N_{\rm n}$. The optimized doping concentration of the N-layer ($N_{\rm n}$) is higher than the doping concentration of the N-drift ($N_{\rm d}$) so as to reduce $R_{\rm on,sp}$. In Fig. 6, as the $H_{\rm n}$ increases, the BV increases due to the enlarged Si area below the drain while the $R_{\rm on,sp}$ increases owing to the extra current path. When $H_{\rm n}$ >

Table 1. Optimized N_d, BV and $R_{on, sp}$ for the four-type devices (Note: $R_{on, sp}$ is the specific on-resistance at $V_{GS} = 5$ V).

Device type	Half-cell pitch (μm)	Optimized N_d (cm^{-3})	BV (V)	$R_{on, sp}$ ($m\Omega\cdot cm^2$)	FOM ($BV^2/R_{on, sp}$) (MW/cm^2)
TGRD MOSFET	6.5	5.2×10^{15}	97	0.985	9.6
TG MOSFET	6.5	4.2×10^{15}	102	1.84	5.7
TGTD MOSFET	6.5	5.2×10^{15}	71	0.931	5.4
Conventional MOSFET	6.5	5×10^{14}	93	5.93	1.5

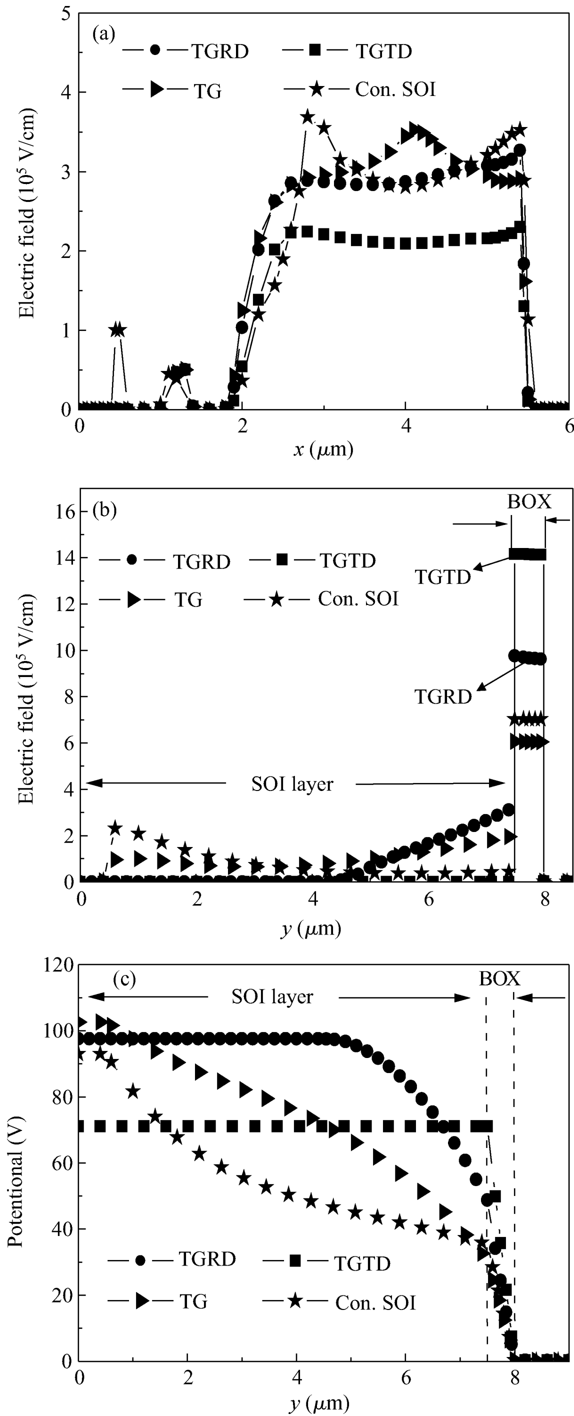

Fig. 4. Electric field distributions in (a) x-direction ($y = 0.01$ μm) and (b) y-direction ($x = 6.3$ μm). (c) Potential distributions in y-direction ($x = 6.3$ μm).

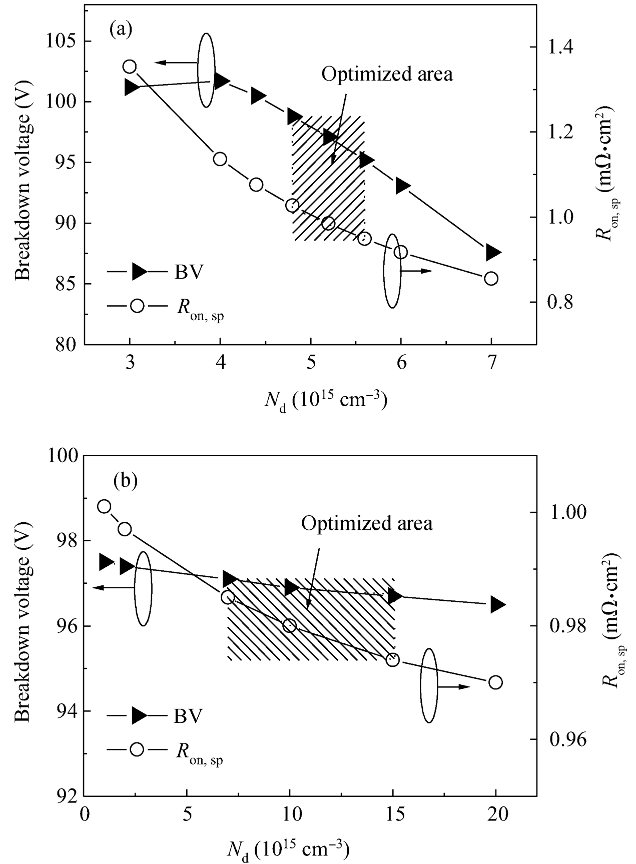

Fig. 5. Influences of (a) N_d and (b) N_n on BV and $R_{on, sp}$ for a TGRD MOSFET at a 6.5 μm half pitch.

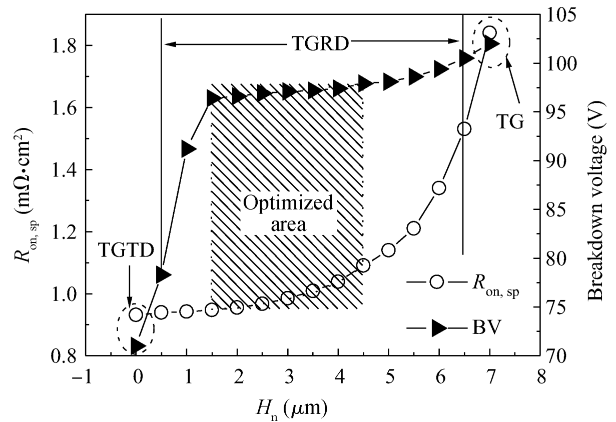

Fig. 6. Influences of the thickness the n-layer H_n on BV and $R_{on, sp}$ for TGRD MOSFET .

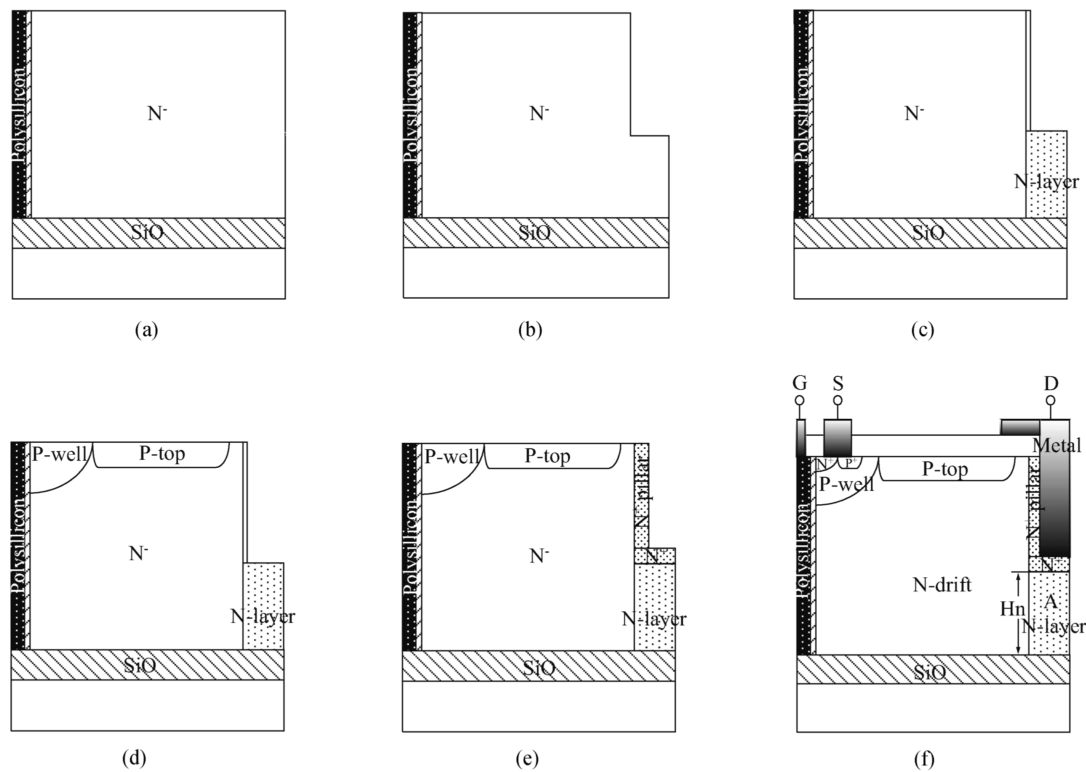

Fig. 7. Processes of the TGRD MOSFET.

4.5 μm, the extra current path increases significantly and the $N_{\rm n}$ decreases with the increased $H_{\rm n}$. It leads to the obviously increased $R_{\rm on,\,sp}$ and decreased FOM. Considering the FOM and process, the optimal ranges of $H_{\rm n}$ are 1.5 μm $\leqslant H_{\rm n} \leqslant$ 4.5 μm at $T_{\rm s}$ = 7.5 μm for a 6.5 μm half cell pitch. The optimal value of $N_{\rm d}$ and $N_{\rm n}$ are 5.2 $\times$ 10^{15} cm^{-3} and 1 $\times$ 10^{16} cm^{-3}, respectively.

Figure 7 shows the key fabrication steps for a TGRD MOSFET wafer: (a) etching the buried oxide layer, thermal oxidation to form the gate oxide layer, and deposition and planarization of poly-silicon to form the gate; (b) forming a shallow trench by RIE; (c) N-layer implantation and annealing; (d) P-top, P-well implantation and annealing; (e) shallow-angle ion implantation through the trench sidewalls to form the N^+ drain region; (f) P^+-contact and N^+-source implantation, formation of electrodes.

4. Conclusion

An SOI MOSFET with a trench gate and a recessed drain is proposed and investigated by simulation. The extended trench gate widens the vertical conduction area and the recessed drain shortens the extra current path, resulting in a minimized $R_{\rm on,\,sp}$. BV = 97 V and $R_{\rm on,\,sp}$ = 0.985 mΩ·cm^2 are obtained at 6.5 μm half-cell pitch. Compared with a TG MOSFET and a conventional MOSFET, the specific on-resistance of the TGRD MOSFET is decreased by 46% and 83%, respectively. The trench gate extended to the BOX synchronously acts as a dielectric isolation trench, simplifying the fabrication processes.

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