An 88 nm gate-length $In_{0.53}Ga_{0.47}As/In_{0.52}Al_{0.48}As$ InP-based HEMT with f_{max} of 201 GHz

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Abstract: An 88 nm gate-length $In_{0.53}Ga_{0.47}As/In_{0.52}Al_{0.48}As$ InP-based high electron mobility transistor (HEMT) was successfully fabricated with a gate width of 2×50 μm and source–drain space of 2.4 μm. The T-gate was defined by electron beam lithography in a trilayer of PMMA/Al/UVIII. The exposure dose and the development time were optimized, and followed by an appropriate residual resist removal process. These devices also demonstrated excellent DC and RF characteristics: the extrinsic maximum transconductance, the full channel current, the threshold voltage, the current gain cutoff frequency and the maximum oscillation frequency of the HEMTs were 765 mS/mm, 591 mA/mm, –0.5 V, 150 GHz and 201 GHz, respectively. The HEMTs are promising for use in millimeter-wave integrated circuits.

Key words: HEMT; gate-length; gate recess; InP; InAlAs/InGaAs
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1. Introduction

Millimeter and submillimeter-wave frequency ranges are of great interests for remote atmospheric sensing, next-generation automotive collision-avoidance radars, broadband satellite communications and low noise detectors. The InP-based high electron mobility transistors (HEMTs) have demonstrated high-frequency, lower microwave and millimeter wave noise and high-gain performance due to the high sheet carrier density, high peak drift velocity and high mobility in the channel. Therefore, the devices are considered to be one of the most promising devices for these applications. Excellent results of InP-based HEMTs have been reported by different groups, e.g., the current gain cutoff frequency (f_T) of 628 GHz, the maximum oscillation frequency (f_{max}) of 331 GHz, the extrinsic maximum transconductance ($g_{m,max}$) of 1.62 S/mm for 30-nm InAs pseudomorphic InP HEMTs[1] , $f_T = 385$ GHz, $f_{max} >$ 1 THz for sub 50 nm InP HEMTs[2] and $f_T = 644$ GHz, $f_{max} = 681$ GHz for 30 nm InAs PHEMTs[3]. These remarkable results stem from the combination of gate size scaling and increased Indium composition in the channel, which improves carrier transport properties. However, HEMTs with a high Indium content channel usually suffer from a serious kink-effect, low breakdown voltage and high output conductance, which are caused by the electron-hole pair generation created by impact ionization. This phenomenon is even more remarkable for short gate length devices, because a much greater electric field exists under the gate area. Adopting an $In_{0.53}Ga_{0.47}As$ channel and reducing the side etched region (L_{side}) in the gate recess process should be effective for avoiding the kink effect[4,5]. Considering that the DC and the RF characteristics of the HEMTs are directly dependent on the T-gate process, the gate size scaling and the optimizing of L_{side} would be effective methods to improve the performance of the HEMTs.

In this paper the design, fabrication and characteristics of 88 nm gate-length InAlAs/InGaAs InP-based HEMTs is described. They exhibit the RF characteristics of $f_T = 150$ GHz and $f_{max} = 201$ GHz. Excellent DC characteristics were also demonstrated with $g_{m,max}$ of 765 mS/mm and the full channel current of 591 mA/mm.

2. Material structures

Figure 1 shows a schematic cross-section of the InP HEMTs. The epitaxial layer structures were grown on 3 inch semi-insulating (100) InP substrates by molecular beam epitaxy (MBE). The epitaxial structure of the HEMTs employed in our study was designed and optimized with parameters shown in Table 1. The layers, from bottom to top, consist of an InAlAs buffer, an InGaAs channel, an unstrained InAlAs spacer layer, a Si-doped plane, a 12 nm thick unstrained InAlAs Schottky barrier layer, and a composite InGaAs cap layer consisting of a Si-doped InGaAs cap layer and a Si-doped $In_{0.53}Ga_{0.47}As$ transition layer. All InAlAs layers were lattice matched with the InP substrate. There is no InP etching-stopper layer in the epitaxial structure. This decreases the distance from the gate to the channel, which is good for the transconductance. Then, the excellent etching selectivity ratio of InGaAs over InAlAs will become crucial. The two-dimensional electron gas (2DEG) sheet density was 3.266×10^{12} cm^{-2} and the mobility was 8000 cm^2/(V·s) at room temperature.

3. Fabrication process

The HEMT fabrication was based on both optical and electron beam lithography. Firstly, device isolation was achieved through the mesa formation by means of a phosphorus acid-based wet chemical etching to expose the $In_{0.52}Al_{0.48}As$ buffer

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Table 1. Device epitaxial layer structure.

Layer	Material	Doping	Thickness (nm)
Cap layer	$In_{0.6}Ga_{0.4}As$	Si:N^{++}, 3×10^{19} cm^{-3}	15
Cap layer	$In_{0.53}Ga_{0.47}As$	Si:N^{+}, 5×10^{18} cm^{-3}	15
Barrier layer	$In_{0.52}Al_{0.48}As$	Undoped	12
Si planar-doped layer		5×10^{12} cm^{-2}	
Spacer layer	$In_{0.52}Al_{0.48}As$	Undoped	3
Channel	$In_{0.53}Ga_{0.47}As$	Undoped	15
Buffer layer	$In_{0.52}Al_{0.48}As$	Undoped	500
S.I. InP sub			

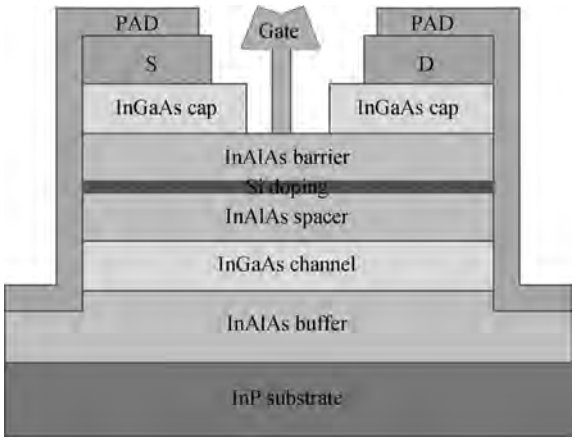

Fig. 1. Schematic cross-section of the InP-based HEMT.

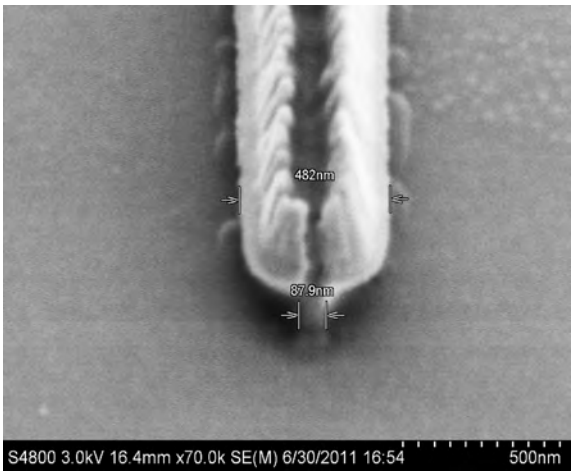

Fig. 2. SEM photograph of T-gate.

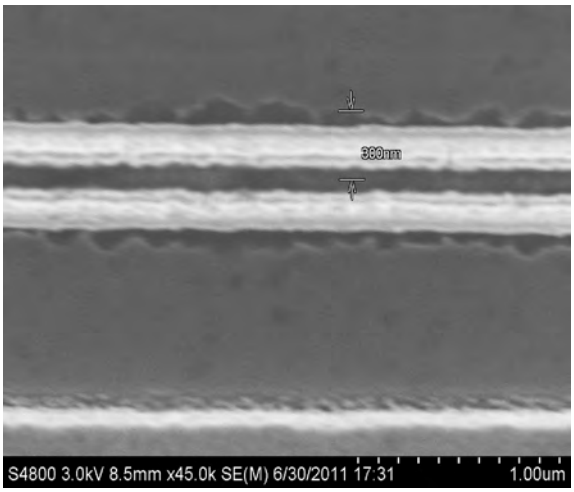

Fig. 3. SEM photograph of the gate recess region with L_{side} of 300 nm.

layer. Secondly, source and drain ohmic contacts were spaced 2.4 μm apart by a lift-off process. Then, Ti/Pt/Au was evaporated by an electron beam evaporator to achieve ohmic metallization without annealing. Transmission line method (TLM) measurements revealed the contact resistance of 0.032 Ω·mm and the specific contact resistivity of 1.03×10^{-7} Ω/cm^2 on linear TLM patterns. Thirdly, in order to measure on-wafer DC and RF characteristics, the coplanar waveguide bond pads were formed using photoresist AZ5214, and Ti/Au connection wires were evaporated.

The final and most important process in the HEMT fabrication was the gate process, which included gate lithography, recess, and metallization. The T-gate was defined by electron beam lithography in a trilayer of PMMA/Al/UVIII. The exposure dose and the development time were optimized, and followed by the residual resist removal process in Matrix105. An insufficient removal process will result in a large gate leakage current and, even worse, it will make the gate-metal break off. However, the removal time should not be too long, otherwise it will increase the gate-length. In the experiment, the removing time was a trade off between low gate leakage current and short gate-length. An 88 nm T-gate can be successfully formed as shown in Fig. 2. Subsequently, the gate recess was formed by wet chemical etching using an aqueous mixture of succinic acid and hydrogen peroxide. The etching selectivity ratio of InGaAs over InAlAs can exceed 100 by adjusting the mixing proportion. As in Ref. [5], the kink effect in the DC characteristics can be eased off by reducing the L_{side}. On the other hand, the reduction of L_{side} will enhance the electric field in the channel and hence cut down the electron transmission time. Also the access part of R_s and R_d would reduce with the decreasing of the recess region, thus increasing the transconductance, and finally improving the f_T and the f_{max}. However, the reduction of L_{side} will reduce the f_{max} by increasing the gate-to-drain capacitance (C_{gd}), and also it will degrade the breakdown voltage by increasing the electric field between the gate and drain. In order to get balance between the above DC and RF characteristics, the length of the side-etched region (L_{side}) was optimized to be about 300 nm (in Fig. 3) by controlling the gate recess etching time. Figure 4 shows a photograph of

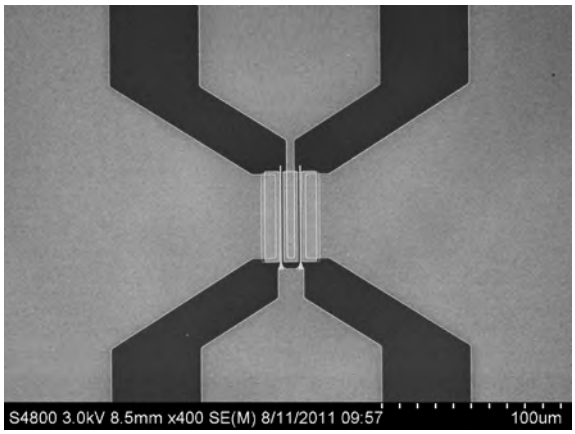

Fig. 4. Photograph of the HEMT with the gate length of 88 nm.

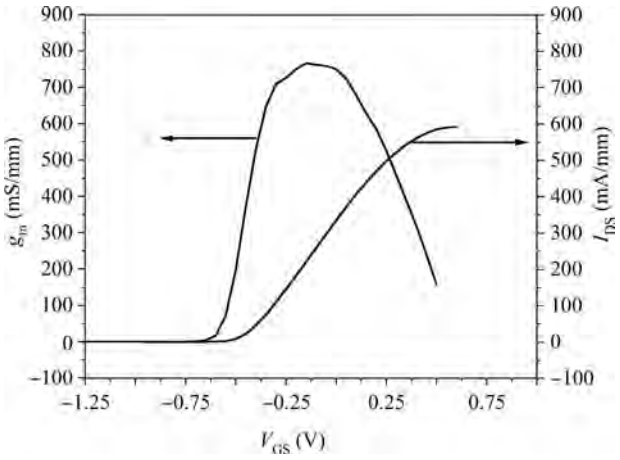

Fig. 6. Transfer characteristics of the HEMT.

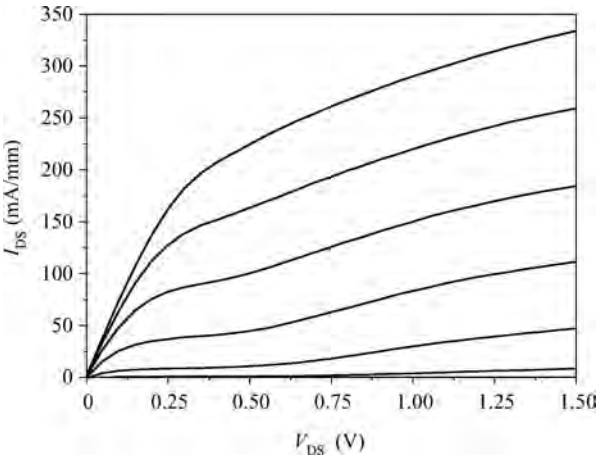

Fig. 5. DC characteristics of the HEMT.

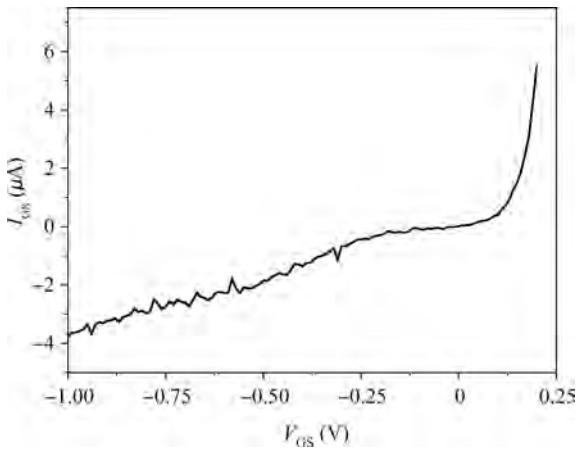

Fig. 7. Gate leakage current of the HEMT.

the device with a gate length of 88 nm, gate width of 2 × 50 μm and source–drain space (L_{ds}) of 2.4 μm. During the whole process, no surface passivation was performed, which would cause a parasitic gate-capacitance effect and weaken the high-frequency performance.

4. Results and discussion

On-wafer DC and RF characteristics were characterized by using the Agilent E8363B PNA series vector network analyzer and on-wafer probes at room temperature.

4.1. DC characteristics

Figure 5 shows current–voltage (I–V) characteristics at room temperature for the HEMTs. The gate–source voltage (V_{GS}) was increased from (bottom) −0.6 to (top) 0 V in 0.1 V steps, and the drain–source voltage (V_{DS}) increased from 0 to 1.5 V. Good pinch-off characteristics and saturation drain current were observed.

Figure 6 demonstrates the gate-bias dependence of transconductance and drain current of the HEMT. The pinch-off voltage V_T is about −0.5 V. The very small contact resistance of 0.032 Ω·mm will benefit $g_{m,max}$. Therefore, a $g_{m,max}$ of 765 mS/mm was obtained at V_{GS} = −0.15 V and V_{DS} = 1.5 V. The measured full channel current at V_{GS} of 0.6 V and saturation drain-to-source current (I_{DSS}) at a V_{GS} of 0 V were 591 mA/mm and 334 mA/mm, respectively.

The gate leakage current was very small (as seen in Fig. 7), which was crucial for the lower frequency LNA applications since gate current was a contributing component to shot noise[6].

4.2. RF characteristics

The measurements were carried out over the frequency range 0.1 to 40 GHz in 0.1 GHz step. S-parameter measurements for open and short pads were also performed on the same wafer in order to calibrate the parasitic capacitance and inductance components related to the pad metals. The value of the f_T was determined by extrapolating the current gain (H_{21}), and the f_{max} by extrapolating the maximum available/stable power gain (MAG/MSG) using a least-squares fitting with a –20 dB/decade slope after subtracting the parasitic parameters due to the probing pads.

As shown in Fig. 8, when the HEMT was approximately biased at the peak transconductance point of V_{GS} = –0.1 V and V_{DS} = 1.75 V, the extrapolated f_T from H_{21} and the extrapolated f_{max} based on MSG/MAG were 150 GHz and 201 GHz, respectively. However, an MSG of 14 dB was measured at the

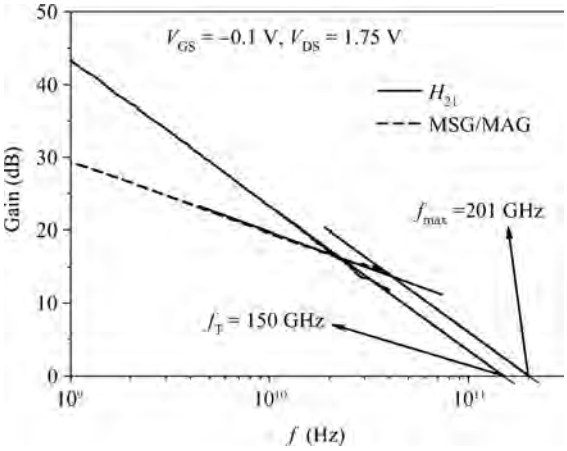

Fig. 8. H_{21}, MAG/MSG versus frequency.

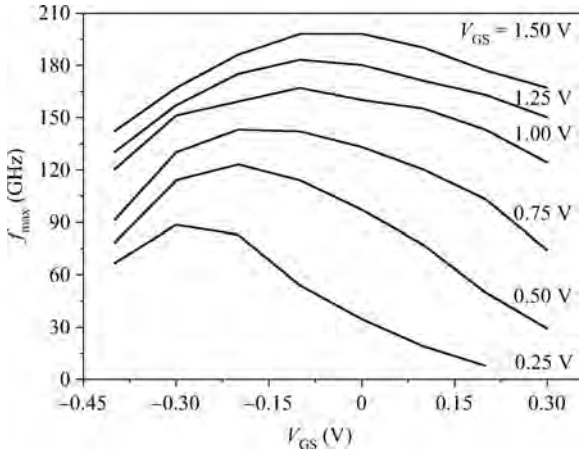

Fig. 9. Dependence of f_{max} on the bias: including V_{GS} and V_{DS}.

instrumentation limit of 40 GHz, at which the device was still potentially unstable ($K < 1$). Extrapolating the gain at –20 dB per decade from this point indicates a real f_{max} of more than 201 GHz.

Figure 9 demonstrates the variation of f_{max} with the bias of V_{GS} and V_{DS}. It saturates or continues to increase slightly above $V_{DS} = 1.0$ V. The explanation for this behavior could be that with increasing V_{DS}, the depletion region on the drain side will expand until the device saturates. As a result, C_{gd} will obviously decrease, finally remaining constant. On the other hand, C_{gs} has less of relation with V_{DS}, and will increase slowly with increasing V_{DS}. It can be induced that f_{max} will continue to increase slightly above $V_{DS} = 1.0$ V.

5. Conclusions

88 nm gate-length InP-based $In_{0.53}Ga_{0.47}As/In_{0.52}Al_{0.48}As$ HEMTs have been fabricated and the L_{side} was optimized to obtain excellent DC and RF performances. In the experiment, the L_{side} was optimized to achieve a balance between the kink effect, breakdown voltage, f_T, and f_{max}. The extrinsic maximum transconductance, full channel current, threshold voltage, f_T and f_{max} of the HEMTs were 765 mS/mm, 591 mA/mm, −0.5 V, 150 GHz and 201 GHz, respectively. Consequently, the HEMTs are promising in millimeter-waveband integrated circuits.

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