Universal trench design method for a high-voltage SOI trench LDMOS*

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Abstract: The design method for a high-voltage SOI trench LDMOS for various trench permittivities, widths and depths is introduced. A universal method for efficient design is presented for the first time, taking the trade-off between breakdown voltage (BV) and specific on-resistance ($R_{s,on}$) into account. The high-k (relative permittivity) dielectric is suitable to fill a shallow and wide trench while the low-k dielectric is suitable to fill a deep and narrow trench. An SOI LDMOS with a vacuum trench in the drift region is also discussed. Simulation results show that the high FOM $BV^2/R_{s,on}$ can be achieved with a trench filled with the low-k dielectric due to its shortened cell-pitch.

Key words: SOI; trench; permittivity; RESURF; LDMOS; breakdown voltage

DOI: 10.1088/1674-4926/33/7/074006 **EEACC:** 2560; 2156

1. Introduction

The key issues in silicon-on-insulator (SOI) high-voltage integrated circuit (HVIC) design are to realize a high breakdown voltage (BV) and low specific on-resistance ($R_{s,on}$). RESURF technology has been successfully employed in improving the breakdown voltage and specific on-resistance tradeoffs in lateral power MOSFETs[1−7]. A 250 V LDMOS structure with an oxide-filled trench in the drift region was proposed exhibiting a 2.5X lower specific on-resistance than that of the conventional lateral DMOSFET[8]. Implementing lateral power MOSFETs in a trench-based technology has been shown to reduce the specific on-resistance, mainly because of the reduced cell pitch[9−11]. This technology has also been widely applied to SOI power lateral MOSFETs[12−15]. However, these researches focus on the TLDMOS (trench LDMOS) with a silicon dioxide trench in the drift region. SOI TLDMOS with different k value dielectric-filled trenches have not been reported and no universal rules for the trench design have so far been given.

The purpose of this paper is mainly to propose the universal trench design method for high-voltage SOI TLDMOS. The dependence of the trench parameters such as permittivity, width and depth on the breakdown voltage and the specific on-resistance is discussed in detail. The high-k (relative permittivity) dielectric is suitable to fill a shallow and wide trench while the low-k dielectric is suitable to fill a deep and narrow trench. However, it is better to choose a low-k dielectric constant filler material to obtain high FOM $BV^2/R_{s,on}$ due to its shortened cell-pitch.

2. Simulation results and discussion

The SOI TLDMOS structure is shown in Fig. 1. Firstly, the oxide trench can increase the electric field strength along the x direction like ENDIF technology[16−20]. Secondly, the drift region is folded in the y direction resulting in multiple-directional depletion[13]. The trench depth and width are D_T and W_T, respectively, and the width of the drift region is 2 μm. N_D is the doping concentration of the drift region. t_s and t_{ox}

Fig. 1. Schematic cross sections of the SOI trench LDMOS. (a) SOI TLDMOS with a high-k filling dielectric. (b) SOI TLDMOS with a low-k filling dielectric.

* Project supported by the National Natural Science Foundation of China (Nos. 61176069, 60976060) and the National Key Laboratory of Analogue Integrated Circuit, China (No. 9140C090304110C0905).

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Received 10 January 2012, revised manuscript received 22 February 2012

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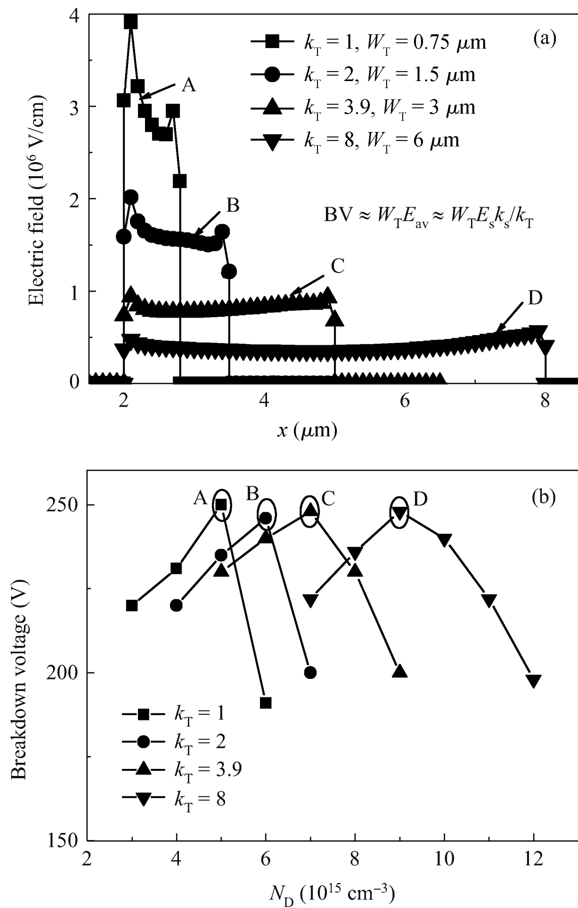

Fig. 2. Simulation curves for the minimum trench width design with the k_T value as a parameter for 240 V-class SOI TLDMOS. (a) Surface electric field distributions of SOI TLDMOS for optimal design ($D_T = 13.5$ μm for $k_T = 1$, $D_T = 9$ μm for $k_T = 2$, $D_T = 6$ μm for $k_T = 3.9$, $D_T = 3$ μm for $k_T = 8$). (b) Dependence of breakdown voltage on the drift doping N_D (the D_T and W_T values are the same as figure (a). Points A–D are optimal designs for the different k_T, respectively.

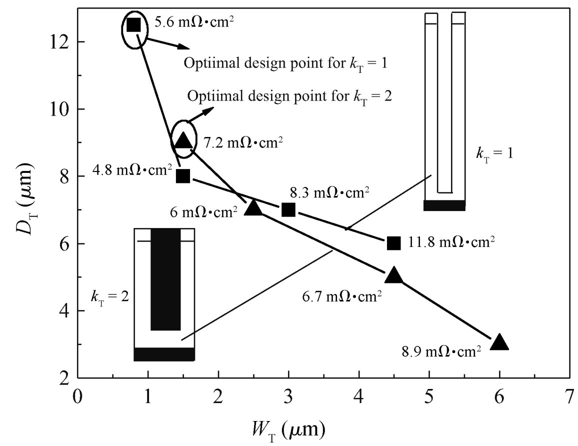

Fig. 3. Trade-off curves between trench depth and width with the dielectric constant of the trench materials as a parameter for 240 V-class SOI TLDMOS.

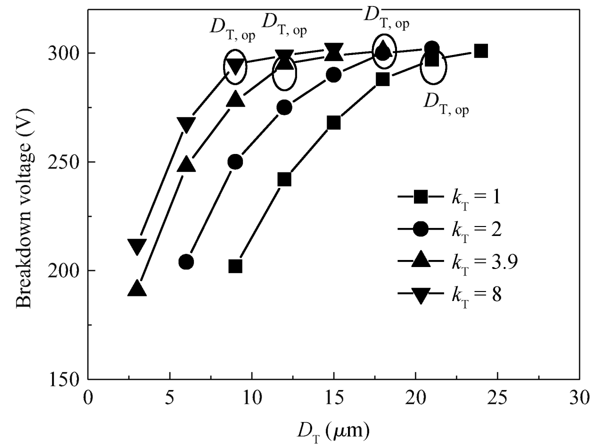

Fig. 4. Relationship between trench depth and breakdown voltage with trench permittivity as a parameter for a 300-V-class SOI TLDMOS.

is the thickness of SOI layer and BOX layer, respectively. The relative permittivity of the trench dielectric and Si drift region are k_T and k_s.

Figure 2 shows the simulation curves for the minimum trench width design with the dielectric constant of the trench materials as a parameter. Figure 2(a) shows the surface electric field distributions for the different k_T values. Simulation results show that the surface electric field can be approximately considered as a rectangular distribution. So, the breakdown voltage is BV $= E_{av} W_T$. E_{av} is the average electric field in the trench area, which can be expressed as $E_{av} = E_S k_s / k_T$ in terms of the Gaussian law if the interface charge between the Si drift region and the oxide trench is neglected. E_s is the critical electric field in the Si drift region. So, the maximum BV of the SOI TLDMOS is $\mathrm{BV}_{max} = W_T E_s k_s / k_T$. The surface electric field is decreased with an increased k_T. To obtain the same BV, the trench width must be increased, as seen in Fig. 2(a). Figure 2(b) shows the dependence of breakdown voltage on the drift doping N_D. The optimal drift doping is decreased with a decreased k_T due to the weakened assisted depletion effect. As discussed above, to obtain the minimum cell pitch, the low-k dielectric is a good choice.

Figure 3 illustrates the reason why the minimum trench width design is chosen. The optimal D_T and W_T values are given for 240 V-class SOI TLDMOS. The 240 V breakdown voltage can be achieved with different D_T and W_T values for the same k_T value. The minimum specific on-resistance is nevertheless obtained when the minimum trench width is chosen. It indicates that when the k_T value of the trench dielectric is chosen, the minimum trench width design is a necessity.

Figure 4 gives the dependence of BV on the D_T when the trench permittivity and width are fixed. The breakdown voltage increases with the increase in D_T due to the increase of the folded drift length. However, when the trench depth reaches its optimal value $D_{T,op}$, the BV is not increased because the maximum BV is restricted by the trench width and the k_T value as illustrated by the formula: $\mathrm{BV}_{max} = W_T E_s k_s / k_T$. So, the minimum trench depth is determined to ensure the lowest specific on-resistance. It can also be seen in Fig. 4 that the optimal trench depth is increased with a decreased k_T value. The drift doping is decreased as seen in Fig. 2(b) resulting in a decreased critical electric field, the drift length must be increased to obtain the same BV.

Universal design curves for the minimum D_T and W_T val-

Table 1. $R_{s,on}$ comparison for different trench permittivity.

k_T for different BV/L_{cell}, R_{on} and $R_{s,on}$ ($V_G = 30$ V)		R_{on} (10^4 mΩ·cm)	L_{cell} (μm)	$R_{s,on}$ (mΩ·cm²)
SOI trench LDMOS (480 V)	$k_T = 8$	1.75	18.5	33
	$k_T = 3.9$	2	12.5	25
	$k_T = 2$	2.32	9.5	22
	$k_T = 1$	3.2	8	26
SOI trench LDMOS (240 V)	$k_T = 8$	0.5	9.5	4.8
	$k_T = 3.9$	0.66	6.5	4.3
	$k_T = 2$	0.86	5	4.3
	$k_T = 1$	1.24	4.2	5.2

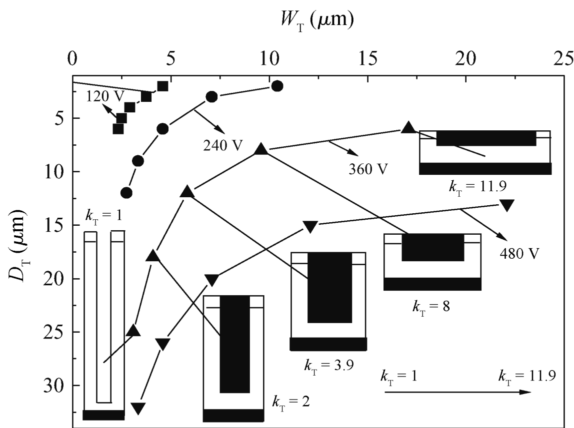

Fig. 5. Trade-off curves between trench depth and width with breakdown voltage as a parameter.

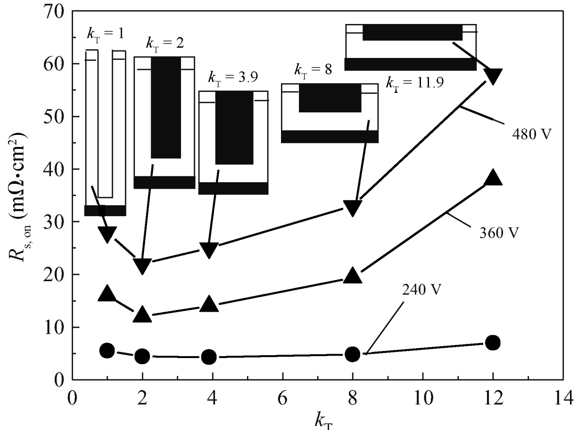

Fig. 6. Dependence of specific on-resistance on trench permittivity with breakdown voltage as a parameter.

ues for the different k_T value as a function of BV are shown in Fig. 5. It should be noted that the high-k dielectric is suitable to fill a shallow and wide trench while the low-k dielectric is suitable to fill a deep and narrow trench. The optimal D_T and W_T design method for different permittivities are illustrated in Figs. 2 and 4, respectively.

Figure 6 shows the influence of the k_T value on the $R_{s,on}$ with the optimal D_T and W_T. The on-resistance R_{on} and specific on-resistance $R_{s,on}$ comparison for different trench permittivity is shown in Table 1. The R_{on} increases with the decrease in k_T due to the lowered drift doping and increased drift length, as seen in Table 1. The optimal cell pitch decreases with the decrease in k_T. The specific on-resistance $R_{s,on} = R_{on}L_{cell}$ is determined by both factors. L_{cell} represents the length of the cell pitch. Simulation results show that the lowest specific on-resistance can be achieved with a low-k dielectric trench, especially for higher breakdown voltage classes. The SOI TLDMOS with vacuum trench ($k_T = 1$) has relatively high $R_{s,on}$ compared with that of low-k trench ($k_T = 2$) because the former has a greatly increased R_{on} but a slightly decreased L_{cell}.

3. Conclusion

The design method for a high voltage SOI trench LDMOS for various trench permittivities, width and depth is theoretically discussed in this paper. Universal curves for the efficient design through consideration of the trade-off between breakdown voltage and specific on-resistance are presented for the first time. The high-k (relative permittivity) dielectric is suitable for filling a shallow and wide trench, while the low-k dielectric is suitable for filling a deep and narrow trench. A low dielectric constant filler material will be a good choice to obtain a high breakdown voltage and low specific on-resistance due to its shortened cell-pitch.

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