An SEU-hardened latch with a triple-interlocked structure*

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Abstract: A single event upset (SEU) tolerant latch with a triple-interlocked structure is presented. Its self-recovery mechanism is implemented by using three pairs of guard-gates and inverters to construct feedback lines inside the structure. This latch effectively suppresses the effects of charge deposition at any single internal node caused by particle strikes. Three recently reported SEU-hardened latches are chosen and compared with this latch in terms of reliability. The potential problems that these three latches could still get flipped due to single event effects or single event effects plus crosstalk coupling are pointed out, which can be mitigated by this proposed latch. The SEU tolerance of each latch design is evaluated through circuit-level SEU injection simulation. Furthermore, discussions on the crosstalk robustness and some other characteristics of these latches are also presented.

Key words: single event upset; single event transient; latch; triple-interlocked; fault injection; crosstalk
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1. Introduction

As technology scales, the reliability problems caused by single event effects (SEEs) become more serious for digital systems developed for space applications. There are two main reasons for this evolution. First, advanced technology makes devices smaller, which reduces the capacitance loads of circuit nodes. Second, lower supply voltages are applied for the purpose of power control. Both of these factors decrease the critical charge, and make circuit nodes more likely to get flipped due to charge deposition caused by particle strikes[1−3].

In digital systems, SEEs affect both combinational logics and sequential cells, whereas lead to different fault modes[4]. For a complementary-metal–oxidation–semiconductor (CMOS) gate, SEEs produce a transient voltage pulse at its output node, which is referred to as single event transient (SET)[5]. This is because the output nodes of combinational logic gates are always driven either by the supply through pull-up networks (PUN), or by the ground through pull-down networks (PDN). Consequently, the deposited charge will finally be removed. For sequential cells, such as SRAMs, flip-flops, and latches, their states are often maintained through types of bi-stable structures, for example, an inverter-loop[6]. Once particles with high enough linear energy transfer (LET) hit these cells, the generated charge changes the states kept by these structures and alters their stored logic values. These structures then hold incorrect states that cannot be recovered. This fault mode is mentioned as single event upset (SEU), which is also the main concern of this paper.

Latches are among the most abundant and important basic units in digital systems, which are always used to sample and hold logic values, as well as to construct edge-triggered flip-flops in the master-slave mode. To achieve SEU tolerance for latches, as well as for other circuits, radiation-hardness-by-design (RHBD) approaches are considered to be more cost-effective and attractive because no radiation-hardening-specific technologies are needed. Redundancy has been the primary RHBD method used to achieve fault tolerance[7]. N modular redundancy (NMR) with majority voting replicates the original module N times and can correct c faults if $N \geqslant 2c+1$[7]. The most famous example of NMR may be triple modular redundancy (TMR)[8]. One significant advantage of TMR is that it can be realized using commercial libraries without any modifications. The dual-interlocked storage cell (DICE) is another well-known approach for SEU-tolerant latch design[9]. This method builds a dual-interlocked structure inside the latch, and can eliminate the level corruption at any single internal node. However, both TMR and DICE have their disadvantages and limitations. For TMR, the area overhead and power increase may be unacceptable. For DICE, the vulnerable internal nodes increase its sensitive area to SEEs[10]. Redundancy feedback is another kind of design approach used for avoiding SEU in latches. Recently, several latch designs based on different forms of redundancy feedback have been reported[10−12]. Although these designs claim that no vulnerable internal nodes are involved, there are still some potential problems in their applications, which will be discussed in detail in this paper.

2. Triple-interlocked latch

In this section, we detail the principles and implementation of the proposed RHBD latch. This latch obtains SEU tolerance by constructing an internal triple-interlocked structure using guard-gates (also mentioned as Muller C-elements)[13, 14]. The transistor-level schematic, symbol, and truth table of guard-gate are shown in Fig. 1. Normally, the guard-gate acts as an inverter if both inputs are identical. If one of its inputs gets disturbed or flipped due to SET or SEU, its PUN and PDN are both cut off, and the output node becomes floating. Hence, the guard-gate enters the filtering mode[10], and the correct logic

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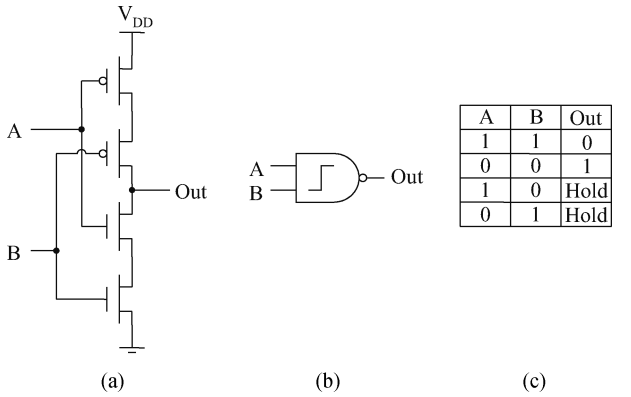

A	B	Out
1	1	0
0	0	1
1	0	Hold
0	1	Hold

Fig. 1. (a) Schematic, (b) symbol, and (c) truth table of guard-gate.

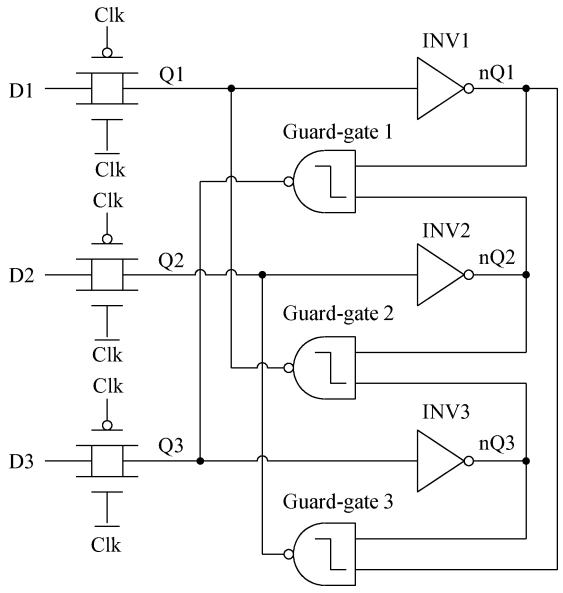

Fig. 2. Proposed latch with a triple-interlocked structure.

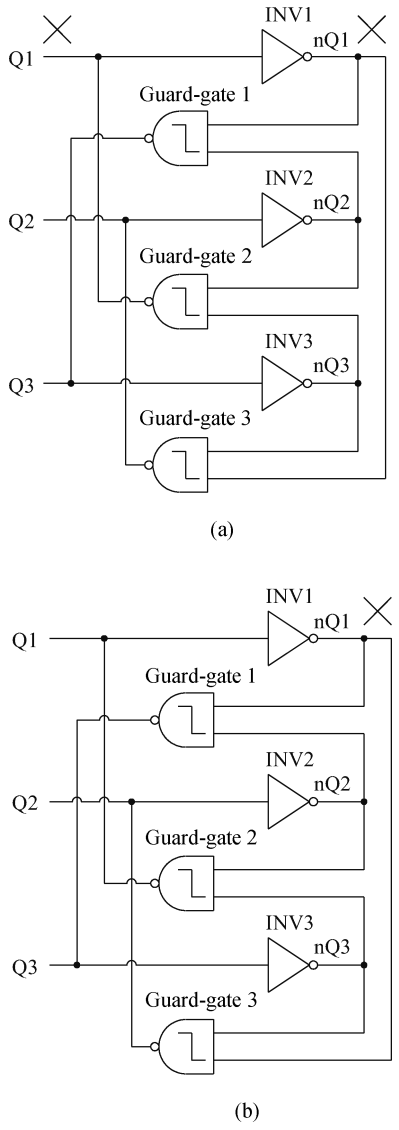

Fig. 3. SEU-hardening of the triple-interlocked structure.

level previously established at the output node will be held.

The structure of this proposed latch is shown in Fig. 2. The three inputs D1, D2, and D3 are identical. There are six internal nodes: Q1, Q2, Q3, nQ1, nQ2, and nQ3. The three guard-gates, Guard-gate 1, Guard-gate 2, Guard-gate 3, are driven by nQ1 and nQ2, nQ2 and nQ3, nQ1 and nQ3, respectively, and their outputs are fed back to Q3, Q1, and Q2. Hence, it is clear that three feedback lines with different start points and end points have been established inside this latch. During normal operation, these three feedback lines prevent each node of this latch from integrity problems caused by leakage and noise injections.

SEEs in this latch can be classified into two cases: {Q1, Q2, Q3} and {nQ1, nQ2, nQ3}. Hence, the analysis of SEEs occurred at Q1 and nQ1 can provide adequate and equivalent results for the two cases. First, assuming that node Q1 is affected by SEEs (marked by × in Fig. 3(a)), the level glitch of Q1 would pass through inverter INV1 and appear at nQ1. Since nQ2 and nQ3 retain the original values, the fault at nQ1 will be blocked by Guard-gate 1 and Guard-gate 3, so Q2, Q3, nQ2, and nQ3 will not be affected. Finally, the level of Q1 will be recovered by Guard-gate 2, and nQ1 will return to its original level. Second, assuming that node nQ1 is affected by SEEs (marked by × in Fig. 3(b)), this fault will be blocked by Guard-gate 1 and Guard-gate 3. Hence, the other nodes will not be affected. Finally, the level of nQ1 will be recovered by INV1. According to the analysis above, SEEs occurred at any single internal node of this latch can be recovered through this triple-interlocked structure.

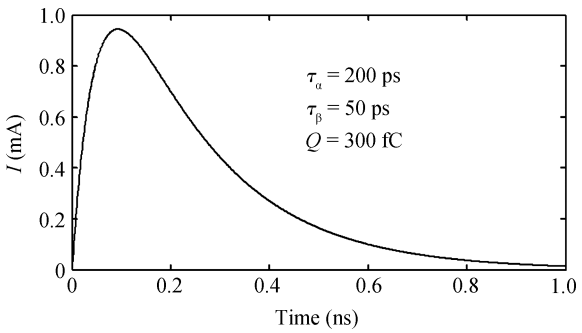

Fig. 4. Current pulse caused by a particle strike.

3. Comparative analysis

In this section, three recently reported latches[10−12], which also use guard-gates to construct internal feedbacks for SEU tolerance, are chosen and analyzed. All these latches are simulated and SEU injected in order to compare them with the proposed latch in terms of reliability.

3.1. SEU-injection method

Circuit-level structures of these latches are constructed using GSMC 130 nm 1.2 V technology. The current pulse that results from a particle strike is described as a double exponential function[15] (in Fig. 4). The expression for this pulse is

$$I(t) = \frac{Q}{\tau_\alpha - \tau_\beta}(e^{-t/\tau_\alpha} - e^{-t/\tau_\beta}). \quad (1)$$

Here Q is the amount of charge deposited as a result of the particle strike, while τ_α is the collection time constant for the junction and τ_β is the ion track establishment constant[15]. For the simulation results reported in this paper, $\tau_\alpha = 200$ ps, $\tau_\beta = 50$ ps, and $Q = 300$ fC[16] are used.

3.2. Reliability analysis of the previous work

Several previously reported latch structures for SEU tolerance have been proven to have vulnerable internal nodes in Ref. [10]. This work also presented its own idea of designing a totally SEU-tolerant latch with the structure shown in Fig. 5(a). This latch has four internal nodes N1, N2, N3, and N4. In hold mode (Clk = 0), SEEs occurred at N1 or N2 can be blocked by Guard-gate 1 and Guard-gate 2. Hence, the output Q will be maintained and the level of N1 or N2 can be finally recovered. Guard-gate 3 is responsible for preventing the propagation of SEEs at N3 or N4. Since SEEs at N3 or N4 can appear at N1 or N2, all guard-gates enter the filtering mode. This phenomenon can be observed from the simulation result shown in Fig. 5(b). At 1 ns, a positive pulse was injected to N3, making N1 drop to "0". This SEU cannot be recovered because the PUN and PDN of Guard-gate 1 were cut off. As shown in Fig. 5(b), although the output Q was not affected, the floating nodes N3, N4, and Q were now quite sensitive to coupled-noise injections. This problem becomes serious in cases where clock frequencies are relatively low, or the latch is used to hold a value for a long period without frequently refreshing operations.

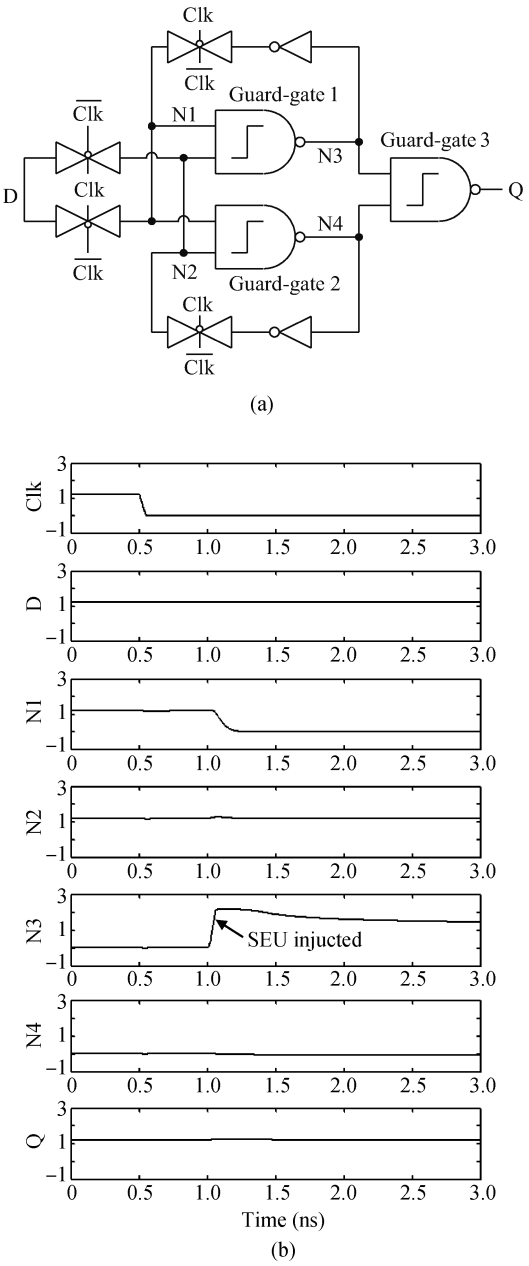

Fig. 5. (a) The latch proposed in Ref. [10] and (b) SEU injection to N3.

The problem of bit-flip induced by SEEs-plus-noise-injection also exists in the latch called the dual-interlocked latch for soft-error-tolerance (DL-SET) proposed in Ref. [11]. The structure of DL-SET is shown in Fig. 6(a). Suppose that in hold mode (Clk = 1), the original values of N1 and N2 are "1". Hence, N3 and N4 are driven to "0", which turns MP1, MP2, MP3, and MP4 on. If SEEs-induced negative charge is collected at N1, N3 jumps to "1", which turns off MP2 and MP4. Since N2's level is unchanged, all guard-gates enter the filtering mode, making N1, N2 and Q floating. This phenomenon can be observed in Fig. 6(b). Again, the floating nodes N1, N2 and Q are now sensitive to coupled-noise, which make the state of DL-SET unstable.

Another latch design with the similar structure to DL-SET was reported in Ref. [12] (in Fig.7). For this latch, two clocked CMOS (C^2MOS) gates and one guard-gate are applied. In Ref. [12], N1 and N2 are treated as equivalent nodes, as well as N3 and N4. However, they are actually not equivalent. This is because N3 and N4 are used for controlling different types of transistors: N3 controls p-channel transistors MP1 and MP3, whereas N4 controls n-channel transistors MN2 and MN4.

Firstly, suppose that in hold mode (Clk = 1), the original values of N1 and N2 are "1". The SEEs-induced negative charge collected at N1 makes N3 jump to "1". This turns off MP1 and MP3. Since N2 retains its level, nodes N1, N2, and Q become floating. This phenomenon can be observed in Fig. 8(a). As discussed above, noise injection will be a problem in this case.

Second, suppose that in hold mode, N2's original value "1" is damaged by SEEs-induced negative charge deposition. N4 jumps to "1", which turns MN2 and MN4 on. Hence, both the

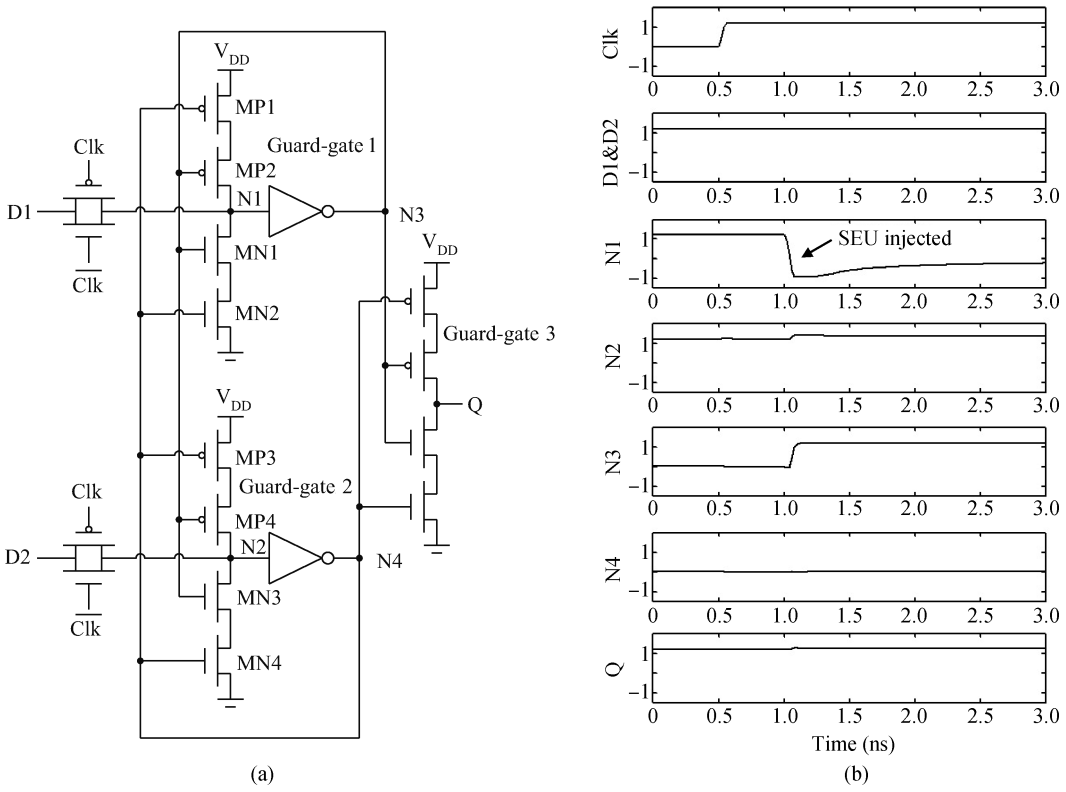

Fig. 6. (a) DL-SET latch proposed in Ref. [11] and (b) SEU injection to N1.

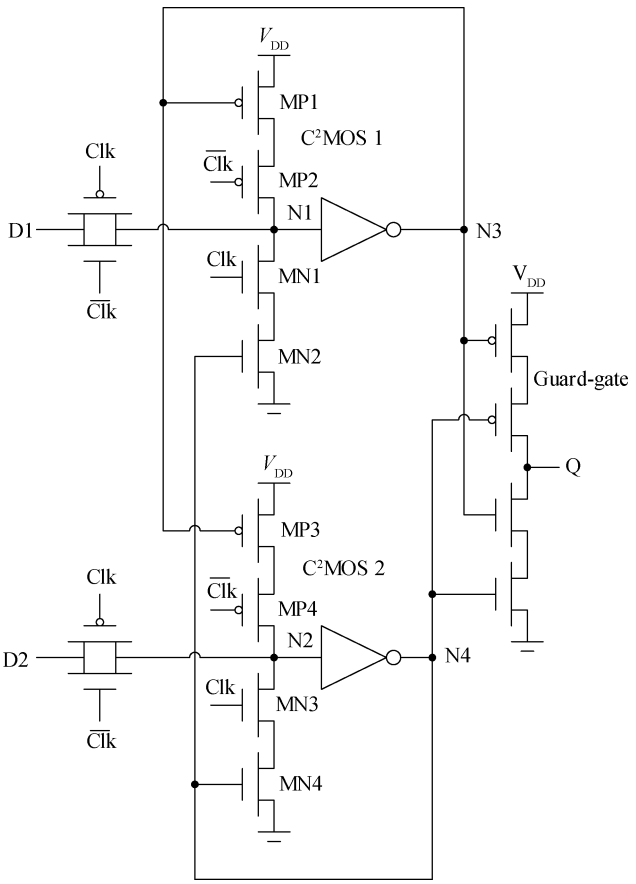

Fig. 7. The latch proposed in Ref. [12].

PUN and PDN of C²MOS 1 are working, making N1 drop to an uncertain level. Then the level of N3 is pulled up, so MP1 becomes weaker in the competition with MN2. This further lowers the level of N1. Finally, this positive feedback pulls N1 down to ground, and MP1 and MP3 are turned off. Then, the low level of N1 and N2 appear at Q, which means this latch has been flipped. This phenomenon can be observed in Fig. 8(b).

The simulation results shown in Fig. 8 give two conclusions: first, nodes N1 and N2 are not equivalent; second, this latch still has vulnerable internal nodes.

3.3. SEU injection simulations of the proposed latch

As analyzed in Section 2, for this proposed latch, only Q1 and nQ1 are needed to be fault injected to evaluate its SEU tolerance. Figures 9(a), 9(b), 10(a), and 10(b) depict the scenarios where Q1 and nQ1 were SEU injected when inputs D1, D2, and D3 were assigned "0" and "1", respectively. From these simulation results, it can be seen that if node nQ1 is affected by SEEs, the three outputs Q1, Q2, and Q3 can retain their original values; if Q1 gets disturbed, a transient voltage pulse appears at nQ1, but the other nodes will not be affected. Furthermore, the level of all nodes can be recovered through the triple-interlocked structure. Hence, the floating periods of Q1, Q2, and Q3 caused by particle strikes can be shortened to mitigate the effects of noise injections.

4. Discussion

In this section, critical characteristics of the latches proposed in Refs. [10, 11], and the latch proposed in this paper are

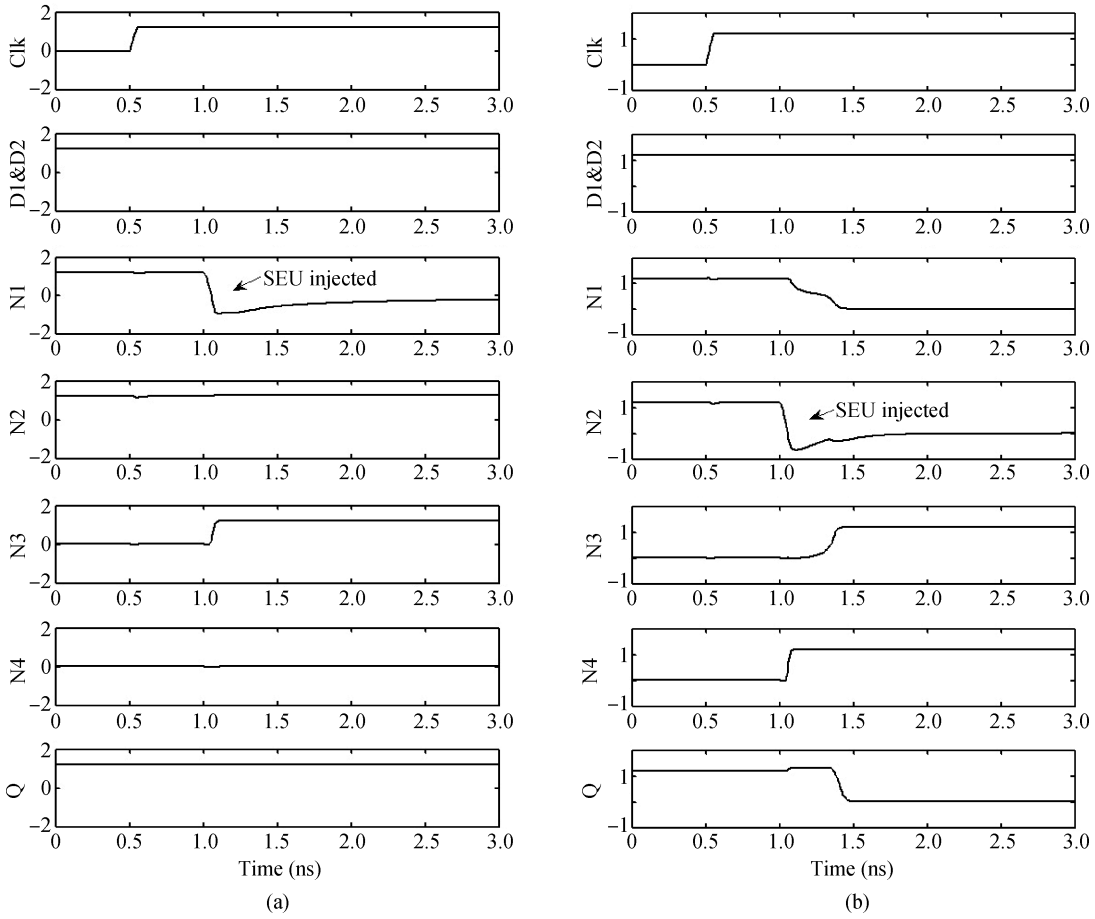

Fig. 8. SEU injection to (a) N1 and (b) N2 of the latch proposed in Ref. [12].

compared, whereas the latch proposed in Ref. [12] is excluded for its SEU intolerance.

4.1. Crosstalk

As discussed in Section 3.2, for the latches proposed in Refs. [10, 11], internal SEUs may make their output and some internal nodes floating, which results in the increased sensitivity to crosstalk noise for these nodes. In this paper, a classical model[17] based crosstalk injection platform is established for the evaluation of each latch's robustness (shown in Fig. 11), and capacitive coupling is taken as the major concern for the reason that it is the dominant effect at current switching speeds[18].

As shown in Fig. 11, the outputs of aggressor drivers (inverters) driven by random bit generators (bit-rate 333 Mbits/s) are coupled with internal and output nodes of the latch under test through cross-coupling capacitors C_Xs. Each random bit generator generates output asynchronously with the Clock (100 MHz, duty ratio 50%) and independently. A periodical SEEs current pulse generator is developed to inject SEEs to user-specified node in each holding phase of the latch. Two NAND2s are used as the external load. The input D of each latch is always driven to "1". Hence, the expected value of Q is known, and each level glitch with a magnitude over $V_{DD}/2$ of Q can be recognized and recorded by using an SEU counter. Xi ($i \in [1, n]$) are the main internal nodes of each latch as discussed in Section 3 (for the latch proposed in Ref. [10], these nodes are N1, N2, N3, and N4; for the latch proposed in Ref. [11], these nodes are N1, N2, N3, and N4; for the latch proposed in this paper, Q1 was used as the output, so these nodes are Q2, Q3, nQ1, nQ2, and nQ3). All the user-developed components (gray colored) are modeled using Verilog-A.

Larger C_X enables more serious crosstalk coupling[17]. In this platform, C_X is user-defined, and 5 fF, 8 fF, and 10 fF were applied. The simulation results of SEU injections plus crosstalk coupling of the three latches are listed in Table 1 (each simulation lasted for 2 μs, 200 cycles).

In Table 1, for the latch proposed in Ref. [10] (Fig. 5 (a)), more output upsets were observed when node N3 was SEU injected periodically, as compared with N1. The previous simulation result given in Fig. 5(b) shows that the three guard-gates of this latch enter the filtering-mode if N3 is flipped, making nodes N3, N4, and Q floating. The level of floating nodes could be more easily affected by noise injections. Hence, in this case, the crosstalk injected could introduce serious level corruption at nodes N3, N4, and Q. An SEU occurred at node N1 could also make nodes N3 and N4 floating. However, this disturbance is recoverable. Hence, the floating periods of N3 and N4 could be shortened, which also results in the fewer output upsets. The analysis above can also explain the results for the latch proposed in Ref. [11]: the SEU occurred at node N3 is recoverable, whereas the one occurred at N1 may not be.

As discussed before, for the latch proposed in this paper, its triple-interlocked structure offers self-recovery ability for

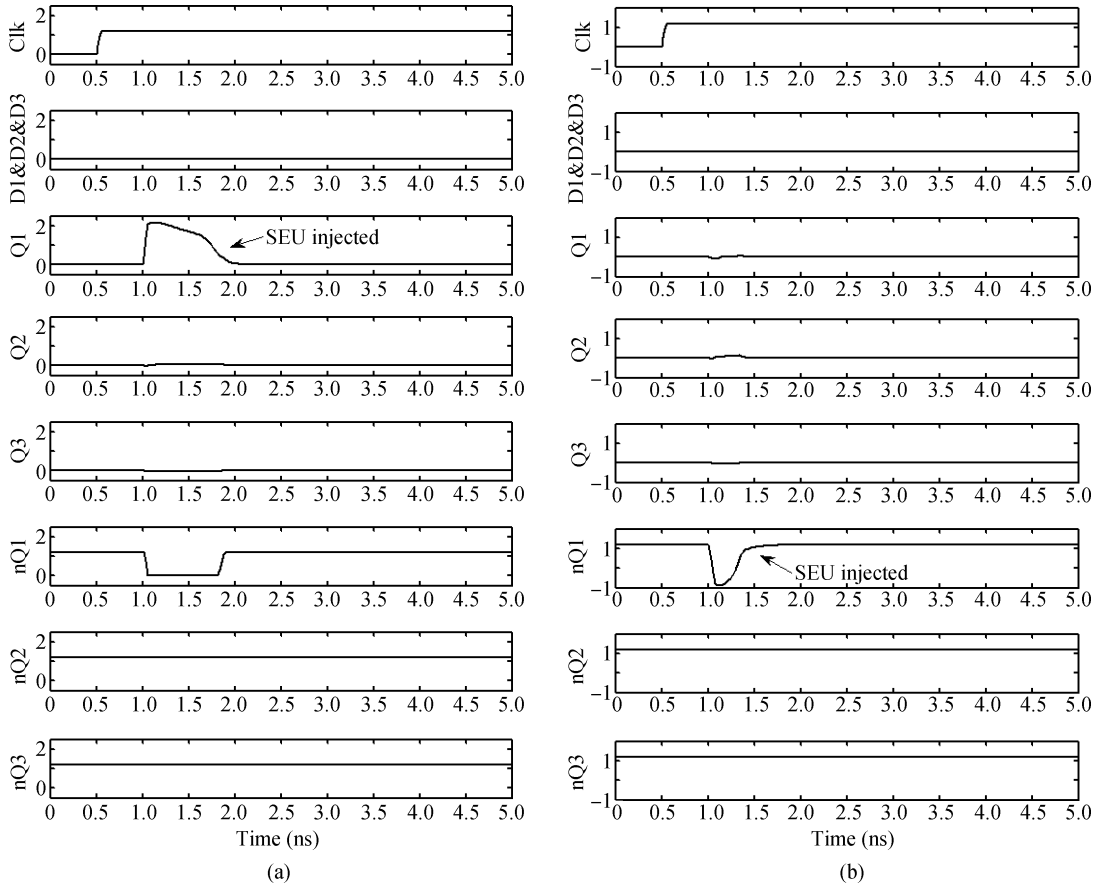

Fig. 9. SEU injection to (a) Q1 and (b) nQ1 when D1 = 0, D2 = 0, D3 = 0.

Table 1. Simulation results of SEU injections plus crosstalk coupling.

Latch under test	Target node of SEU injections	Amount of output's upsets		
		$C_X = 5$ fF	$C_X = 8$ fF	$C_X = 10$ fF
Proposed in Ref. [10]	N1	0	6	10
	N3	3	26	34
Proposed in Ref. [11]	N1	0	22	47
	N3	0	0	6
This work	Q2	0	0	0
	Q3	0	0	0
	nQ1	0	0	0
	nQ2	0	0	0
	nQ3	0	0	0

all the nodes. This enables the proposed latch to have the opportunity to return to the original stable state before being affected by possible crosstalk. As shown in Table 1, no upset was observed at the output node when Q2, Q3, nQ1, nQ2, or nQ3 was SEU injected periodically.

Table 2. Amount of transistors and clocked transistors needed for each latch design.

Latch	Ref. [10]	Ref. [11]	This work
Total transistors	24	20	24
Clocked transistors	8	4	6

4.2. Area, power, and performance

For the latches proposed in Refs. [10, 11], and the latch proposed in this paper, the numbers of transistors and clocked transistors needed are listed in Table 2.

As shown in Table 2, the latch structure proposed in Ref. [11] consumes the least amount of transistors, which makes it be the most area effective solution. However, the area evaluation for these three latches cannot just rely on the numbers of transistors needed. As shown in Figs. 5(a) and 6(a), both the latches proposed in Refs. [10, 11] apply the guard-gates as the output stages. A guard-gate uses two transistors in series to form PUN and PDN, respectively (Fig. 1(a)). To provide enough driving capability, the sizes of its transistors need to be made larger, which leads to an area overhead. This problem may be more serious for the latch proposed in Ref. [10], because its three guard-gates are all used to drive the back-end gates. On the other hand, making the transistors of a guard-gate

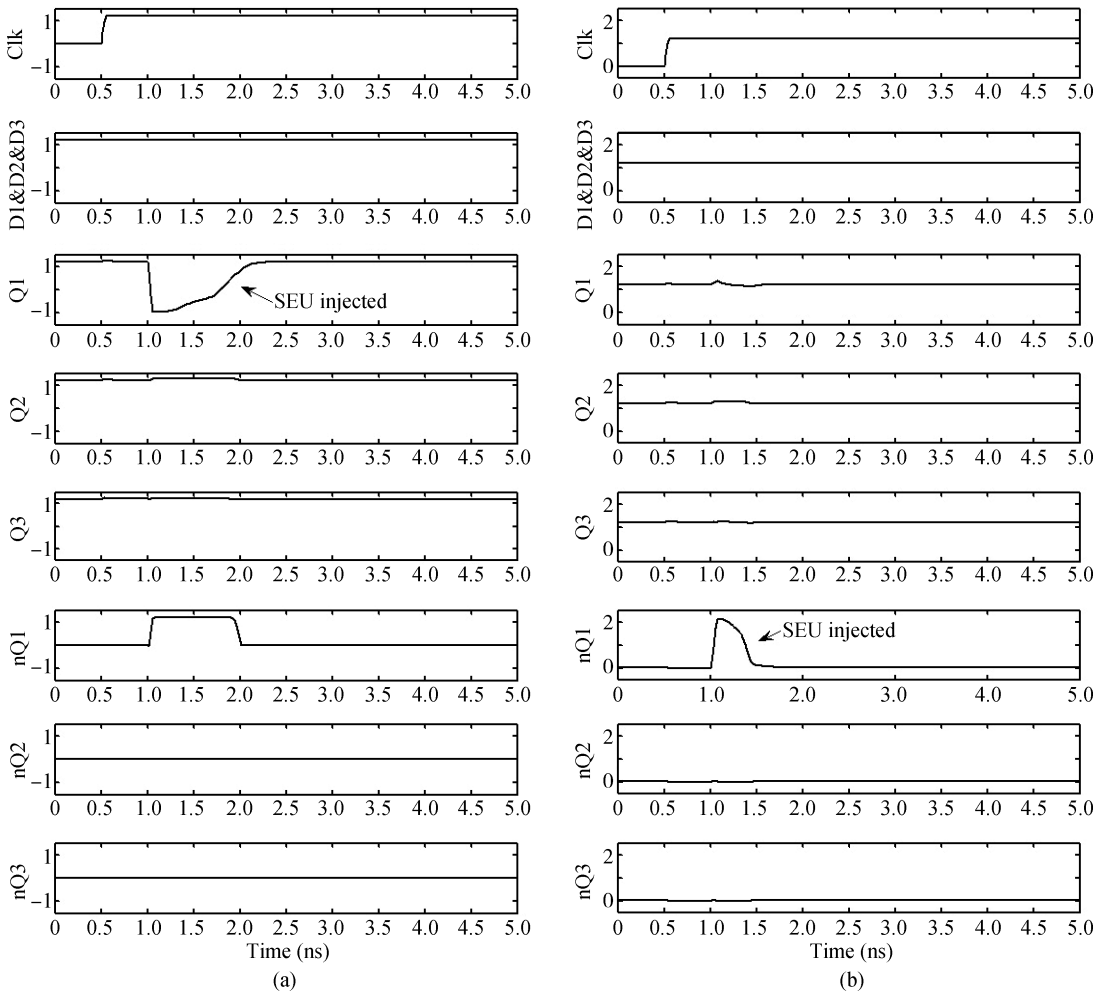

Fig. 10. SEU injection to (a) Q1 and (b) nQ1 when D1 = 1, D2 = 1, D3 = 1.

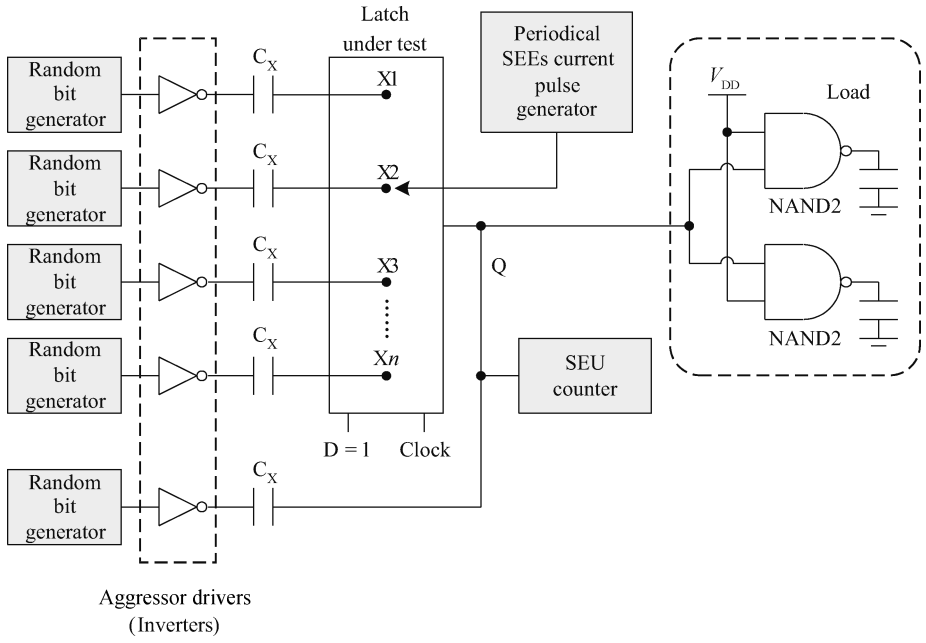

Fig. 11. Crosstalk injection platform.

larger will increase the load of its front-end gate. This may induce speed degradation and should be treated carefully.

For the latch proposed in this paper, the three guard-gates inside are not used to drive load, but applied to construct the internal feedbacks. Hence, these guard-gates can be realized using transistors with relatively small sizes to make it easier for the front-end circuit to write in the new value, and also to reduce area. However, this adjustment results in a longer time needed to recover the SEUs occurring at nodes Q1, Q2, and Q3 by these three guard-gates. For this problem, besides gate sizing, some layout techniques, such as guard rings and guard drains[19], can be introduced to reduce the amount of SEEs-induced charge collected by these nodes and shorten the recovery period.

The amount of total capacitance impacts the latch power significantly. Hence, reducing the total area also helps to reduce power. For latches, the amount of clocked transistors is another critical issue. As shown in Table 2, the latch proposed in Ref. [11] needs the least number of clocked transistors, which helps to reduce the total loads and power of clock network.

5. Conclusion

In this paper, an SEU tolerant latch with a triple-interlocked structure is proposed. This latch applies three pairs of guard-gates and inverters to construct three internal feedback lines with different start and end points. By using this structure, the effects of depositing charge at any single internal node by a particle strike can be suppressed. Three RHBD latches previously reported in Refs. [10–12] are chosen and compared with this latch. Circuit-level SEU injection simulations of the latches proposed in Refs. [10, 11] show that SEUs-occurred inside the latches may make some internal nodes and the output nodes of these two latches float. This increases the sensitivity to crosstalk coupling for these two latches, which could still lead to the bit-flips finally. This conclusion is further confirmed through crosstalk plus SEU injection simulations. The latch structure proposed in Ref. [12] is proven to be unreliable when certain internal nodes are affected by SEEs. The latches proposed in Refs. [10, 11] are also compared with this proposed latch in terms of area, power, and performance, and some quantitative and qualitative conclusions are given.

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