A low-power low-voltage slew-rate enhancement circuit for two-stage operational amplifiers*

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Abstract: A novel circuit is presented in order to enhance the slew rate of two-stage operational amplifiers. The enhancer utilizes the class-AB input stage to improve current efficiency, while it works on an open loop with regard to the enhanced amplifier so that it has no effect on the stability of the amplifier. During the slewing period, the enhancer detects input differential voltage of the amplifier, and produces external enhancement currents for the amplifier, driving load capacitors to charge/discharge faster. Simulation results show that, for a large input step, the enhancer reduces settling time by nearly 50%. When the circuit is employed in a sample-and-hold circuit, it greatly improves the spur-free dynamic range by 44.6 dB and the total harmonic distortion by 43.9 dB. The proposed circuit is very suitable to operate under a low voltage (1.2 V or below) with a standby current of 200 μA.

Key words: slew-rate enhancement; two-stage operational amplifier; low-voltage operation; low-power consumption

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1. Introduction

Recently, motivated by emerging modern wireless and portable consumer electronics in which the size and density of the chips continues to increase, the difficulty of dissipating the generated heat might add a cost to the system or limit the functionality that can be provided. Therefore, optimized power consumption has been highlighted in worldwide academic and industrial research[1,2]. Meanwhile, in order to reduce costs and improve the system performance, it is very common to integrate analog modules in a system-on-a-chip (SoC), so that analog circuits have to be implemented with standard digital CMOS processes which now enter the nanometer era and challenge the analog design with a lower supply voltage. However, in analog circuits, reduction of power dissipation while maintaining a high speed is not as straightforward as in the digital case[1].

In most wireless and portable products, operational transconductance amplifiers (OTAs) are adopted as active elements in analog circuits including data converters, switched-capacitor filters and driving buffers[1]. As the analog circuits have embarked on their implementation in nanometer CMOS processes, besides being a low-power and power-efficient operation, OTAs should have a fast transient behavior which necessitates a large slew rate (SR) to reduce the settling time occupied by the slewing phase[2]. However, reconciling these demands is difficult with traditional Class-A topologies, since the maximum driving current is limited by the fixed bias current. Thus, several slew-rate enhancement (SRE) methods have been presented to deal with the dilemma between high speed and low power dissipation[3−11]. In recent publications, Reference [6] uses an adaptive-biasing technique in its class-AB input stage, while Reference [7] adopts an auxiliary monitor circuit to adjust the driving current, and Reference [8] employs a dynamic current bias for a large output current. Unfortunately, some of these systems can hardly operate under a supply voltage below 1.2 V[3,7], or be thorny to achieve unconditional stability because of the positive current feedback[4,11], or only work well for one-stage OTAs[5,6,8−10].

In this paper, an efficient SRE technique for two-stage OTAs is proposed, which works under a low supply voltage and brings an external boost current to the OTA with a small standby current during the slewing of the OTA while it is off during the small-signal period of the OTA. The SRE circuit is applied to boost the performance of the OTA in a sample-and-hold circuit (SHC) in order to demonstrate its practicality.

2. The proposed SRE concept

A block diagram of the enhanced sample-and-hold circuit (SHC) which incorporates an OTA is shown in Fig. 1. This diagram shows a flip-around switched-capacitor SHC with non-overlapping clocks Φ_S and Φ_H and an added external enhancer which provides a dynamic current at the output of the OTA. This is accomplished by measuring the input differential voltage of the OTA and then injecting a proportionate amount of charge at the output of the OTA, i.e., the output of the SHC. The enhancer operates a completely open loop with respect to the OTA and does the bulk of the settling task. For instance, if the enhancer helps the OTA settle to 90% accuracy, then the OTA itself has only to be responsible for 10% of settling.

The enhancer contains three parts: a class-AB input stage,

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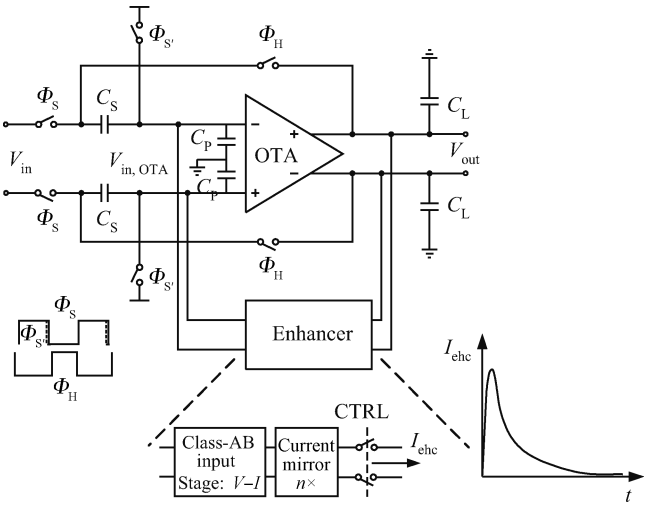

Fig. 1. The slew rate enhancer located externally to the SHC.

a current mirror, and a control switch. The input stage converts the input voltage of the OTA into a dynamic current which is then mirrored into the current mirror to generate the enhancement current I_{ehc} with n-time amplification, which is then conducted to the output of the OTA. The "CTRL" switch is closed to connect the enhancer with the OTA in the slewing period, and it is open if the OTA is in a quiescent state or small-signal settling period. The circuit implementation of the input stage and the "CTRL" switch will be explained in Section 3.

A brief summary of the operation of the enhancer in the SHC is as follows: during the Φ_S clock phase, the input signal, V_{in}, is sampled on the sample capacitor C_S. At the beginning of Φ_H, the "CTRL" switch is closed and two C_S's are flipped around to get their upper plates connected to the output of the OTA. Considering that the voltage across the capacitor is forbidden to undergo a sudden change, an instantaneous step appears at the input of the OTA, leading to the slewing of the OTA. Meanwhile, the step is sensed by the class-AB input stage of the enhancer immediately and a dynamic current is converted from the step. This current is amplified by the current mirror to produce the enhancement current I_{ehc} which is dumped directly on the output of the OTA. The current I_{ehc} will have an initial peak value, and will then continually decrease as the feedback of the SHC forces the input voltage of the OTA, $V_{in,OTA}$, to decrease. When $V_{in,OTA}$ reduces to a critical value, the enhancer disconnects itself from the OTA by opening the "CTRL" switch and thereby prevents itself from overcompensating, i.e., providing too much enhancement current. Note that the enhancer is fully differential, so the current I_{ehc} is a differential current and its direction depends on the polarity of V_{in}.

The time-domain solution for the enhancement current I_{ehc} can be found by assuming a large positive signal of V_{in} is sampled on the C_S. Thus, a negative step, $V_{in,OTA} = -V_{in}$, is presented at the input of the OTA at the very beginning of Φ_H, so that the class-AB input stage convert the voltage $V_{in,OTA}$ into the dynamic current of

$$I_{dyn} = \beta(-V_{in,OTA} - V_{TH})^2, \tag{1}$$

where I_{dyn} is the dynamic current, $\beta = \mu C_{ox}(W/L)$ is the geometry factor of the input device of the class-AB input stage, $V_{in,OTA}$ is the voltage at the input of the OTA which is a negative value, and V_{TH} is the threshold voltage of the input device. Since the enhancement current, $I_{ehc} = nI_{dyn}$, is directly charged to the output of the OTA, applying KCL at the output of the OTA gives

$$I_{ehc} = -C_L\frac{d}{dt}V_{out} - C_S\frac{d}{dt}(V_{out} + V_{in,OTA}), \tag{2}$$

assuming that the enhancement current is much larger than the current provided by the OTA, and therefore the slew is mainly contributed by the enhancement current. Note that

$$C_S\frac{d}{dt}(V_{out} + V_{in,OTA}) = -C_P\frac{d}{dt}V_{in,OTA}. \tag{3}$$

Substituting Eqs. (1) and (3) into Eq. (2) and solving the equation with an initial condition of $V_{in,OTA}(t = 0) = -V_{in}$ yields

$$I_{ehc}(t) = \frac{I_{ehc,peak}}{\left[1 + \dfrac{n\beta}{CC}(V_{in} - V_{TH})t\right]^2}, \tag{4}$$

$$V_{out}(t) = \frac{\dfrac{I_{ehc,peak}}{CC}t}{1 + \dfrac{n\beta}{CC}(V_{in} - V_{TH})t}, \tag{5}$$

where $I_{ehc,peak} = n\beta(V_{in} - V_{TH})^2$ and $CC = C_L(1 + C_P/C_S) + C_P$.

Equations (4) and (5) are the close solution of the enhancement current and output voltage, respectively. They are valid only when the OTA is slewing. For design purposes, the gain of the current mirror, n, must be chosen carefully. If n is large, the output voltage, V_{out}, settles fast according to Eq. (5). However, in realistic circuit implementation, a high-gain current mirror is accompanied by a heavy internal parasitic capacitance which slows down the conduction of the enhancement current, and hence deteriorates the effect of the enhancer. In reality, the value of n is selected by simulation for every process-voltage-temperature (PVT) corner.

As the slewing goes on, the input voltage of the OTA decreases gradually. When it drops to a small value, the enhancement is automatically terminated in order to avoid overcharging by opening the "CTRL" switch and the OTA continues to complete the charge transfer to a high accuracy, i.e., the OTA enters a small-signal settling phase. In addition, since the enhancer is separated from the output of the OTA by open switches when settling ends, it does not affect the stability and noise performance of the complete SHC.

3. Circuit implementation

To apply the introduced SRE concept into enhancing the two-stage OTAs, some improvements should be made, since the slewing of the two-stage OTAs is very different from that of the one-stage counterparts. Therefore, the slewing behavior should be explored at first.

Figure 2 depicts a typical fully-differential two-stage OTA widely used in switched-capacitor circuits[12−14]. Assuming that a large positive step is applied to the input, MA1 is turned

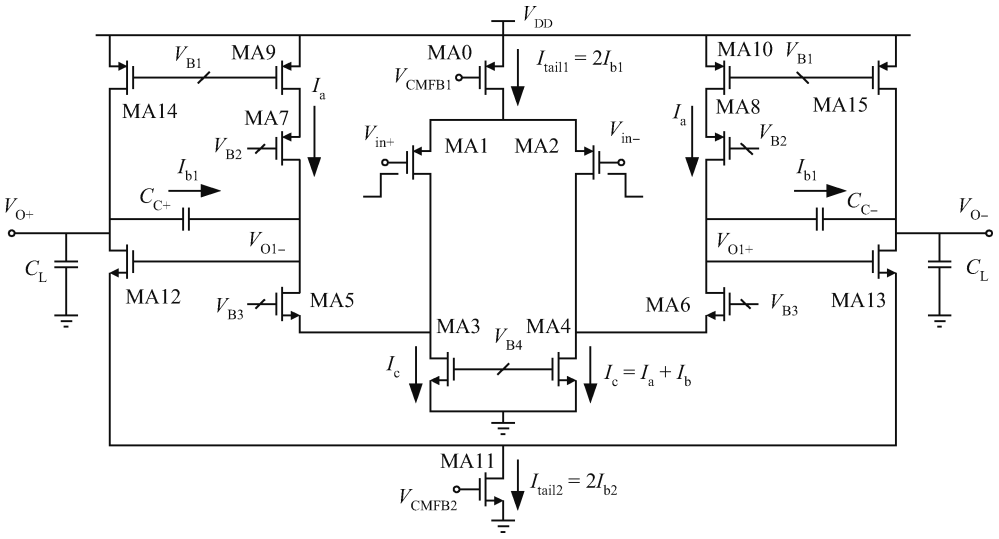

Fig. 2. The slewing of the two-stage OTA.

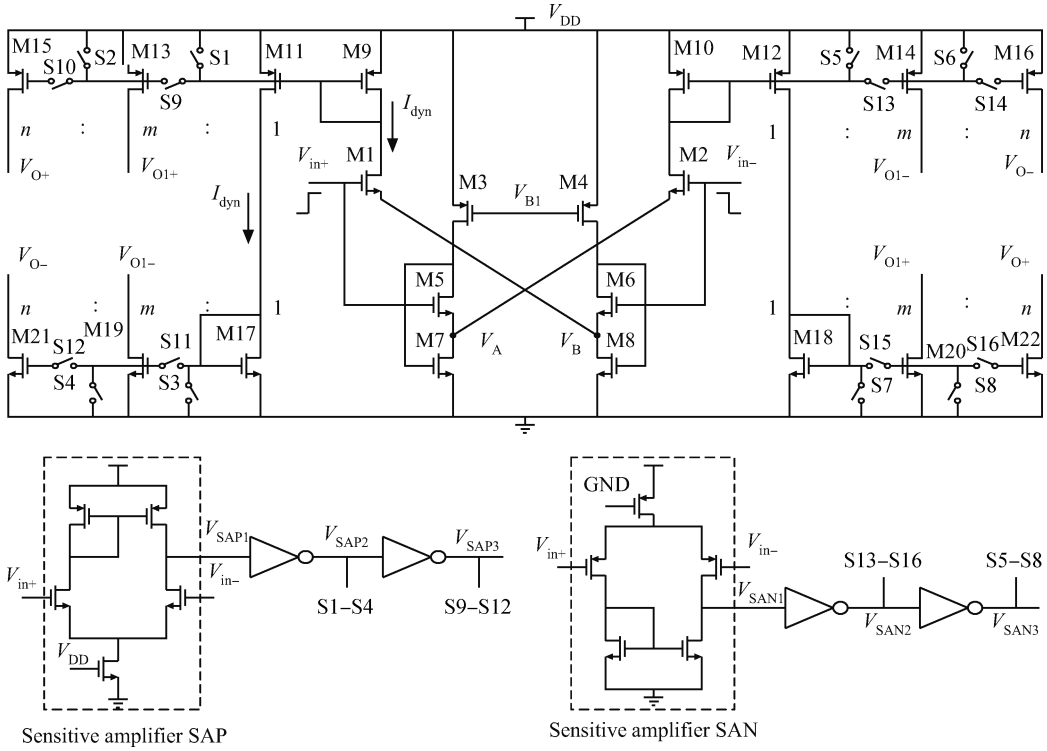

Fig. 3. The proposed slew-rate enhancer.

off and total tail current of the first stage, $I_{tail1} = 2I_{b1}$, flows through MA2. If the current provided by PMOS current sources MA7–MA10, I_a, is larger than I_{b1}, a current of I_{b1} will go through compensation capacitors C_{C+} and C_{C-}, leading to the first stage slew limit of $2I_{b1}/C_C$ [2]. For the second stage, due to rise of V_{O1+} and fall of V_{O1-} caused by the positive input voltage, MA13 is cut-off while MA12 pulls all the tail current of the second stage, $I_{tail2} = 2I_{b2}$. Recognizing that MA14 and MA15 sink a current of I_{b2}, two currents of I_{b2} charge the load and compensation capacitors, $C_L + C_C$, at node V_{O+} and discharges them at node V_{O-} respectively. The differential slew rate can be approximated to first order by a well-known equation[16]:

$$\mathrm{SR} = \min\left(\frac{2I_{b1}}{C_C}, \frac{2I_{b2}}{C_L + C_C}\right). \tag{6}$$

Equation (6) indicates that the slew rate of the two-stage OTA is limited by both the driving currents of C_C and C_L provided by the first and second stage. To enhance the slew rate, the driving current for both the first and second stage of the OTA must be boosted. Therefore, a current enhancer with the SRE concept discussed in Section 2 is proposed which applies external driving currents to nodes V_{O1+}, V_{O1-}, V_{O+} and V_{O-}, enriching the currents which drive C_C and C_L.

As shown in Fig. 3, the enhancer contains a class-AB input stage (M1–M8)[15], driving transistors (M13–M22), and con-

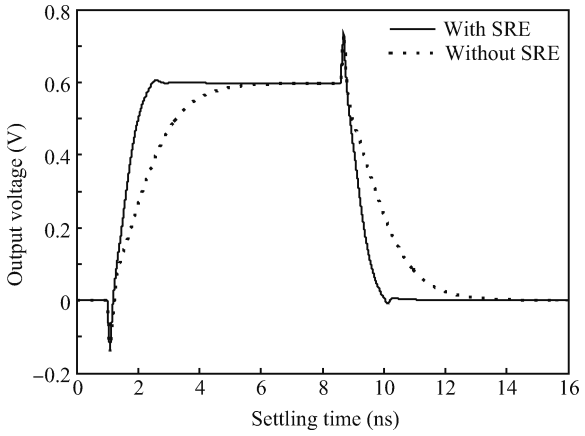

Fig. 4. Simulated OTA step response.

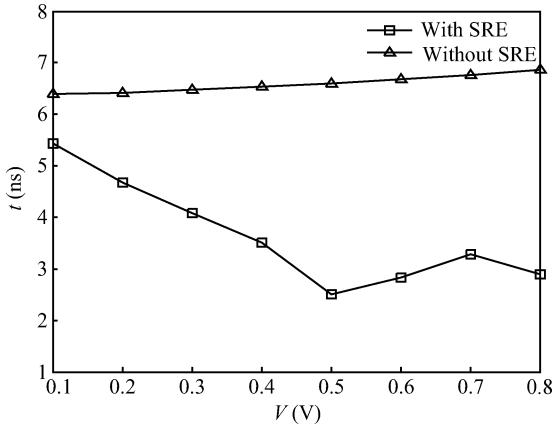

Fig. 5. Settling performance versus input amplitude.

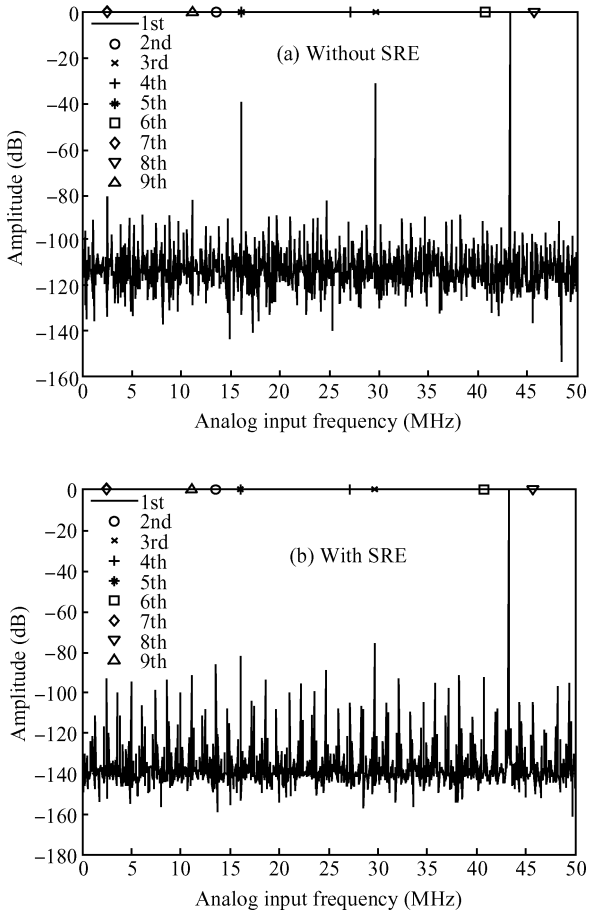

Fig. 6. FFT performance of the S/H circuit with an Nyquist-frequency full-swing input.

trol circuit (switches S1–S16, and sensitive amplifiers SAP and SAN),which adopts the previously introduced SRE concept. The enhancer is fully differential and complementary, i.e., the left half of the circuit works if the input voltage is positive, while the right half of the circuit works if the input voltage is negative. Depending on which half of the circuit is operating, the input stage senses the input voltage and generates a dynamic current through either M1 or M2 which is mirrored and amplified by four active driving transistors in either the left half (M13, M15, M19 and M21) or right half (M14, M16, M20 and M22), yielding four enhancement currents applied to V_{O+}, V_{O-}, V_{O1+} and V_{O1-} respectively. In the control circuit, the signals, V_{SAP2}, V_{SAP3}, V_{SAN2} and V_{SAN3}, drive S1–S16 to determine the connection between the enhancer and the OTA by enabling/disabling the driving devices.

Quiescently, V_{SAP1} and V_{SAN1} are biased at a voltage of $0.4V_{DD}$ and $0.6V_{DD}$ respectively, holding V_{SAP2}, V_{SAP3}, V_{SAN2} and V_{SAN3} at a voltage of V_{DD}, 0, 0 and V_{DD} respectively so that S1–S8 are closed and S9–S16 are opened, disabling all driving devices and hence disengaging the enhancer from the OTA. When a large positive voltage is applied to the input, it pulls V_A up and V_B down, forcing saturated M1 to produce a dynamic current of I_{dyn} and M2 to cut-off[15]. Meanwhile, the sensitive amplifier SAP raises V_{SAP1} dramatically, turning V_{SAP2} to 0 and V_{SAP3} to V_{DD} and subsequently opening S1–S4 and closing S9–S12 to start up driving devices M13, M15, M19 and M21 in the left half of the circuit. M13 injects anenhancement current of mI_{dyn} to V_{O1+} while M19 drains the same current as M13 from V_{O1-}, improving the current which drives C_C by mI_{dyn}. Additionally, M15 injects another enhancement current of nI_{dyn} to V_{O+} while M19 drains the same current as M15 from V_{O-}, improving the current which drives C_L plus C_C by nI_{dyn}. Thus, the enhanced differential SR can be written as

$$\mathrm{SR}_{\mathrm{enhanced}} = \min\left(\frac{2I_{b1} + 2mI_{dyn}}{C_C}, \frac{2I_{b2} + 2nI_{dyn}}{C_L + C_C}\right). \quad (7)$$

As the settling goes on, the negative feedback of the SHC reduces the input voltage of the OTA, so that V_{SAP1} drops and V_{SAP2} and V_{SAP3} turn back to their quiescent voltages gradually, reclosing S1–S4 and reopening S9–S12, which will disconnect the enhancer from the OTA. During the enhanced positive settling, V_{SAN1} fixes V_{SAN2} and V_{SAN3} unchanged, disablingM14, M16, M20 and M22 inthe right half of the circuit. Similar operations of the right half of the circuit can be easily analyzed if the input voltage is negative.

The implementation of the enhancer has several distinct advantages. First of all, the enhancer can work under a low supply voltage which should satisfy a very loose condition:

$$V_{DD} > V_{th,n} + V_{ov,p} + 2V_{ov,n}, \quad (8)$$

where $V_{th,p}$, $V_{ov,p}$ and $V_{ov,n}$ are the threshold voltage of the PMOS device, and the overdrive voltage of the PMOS and

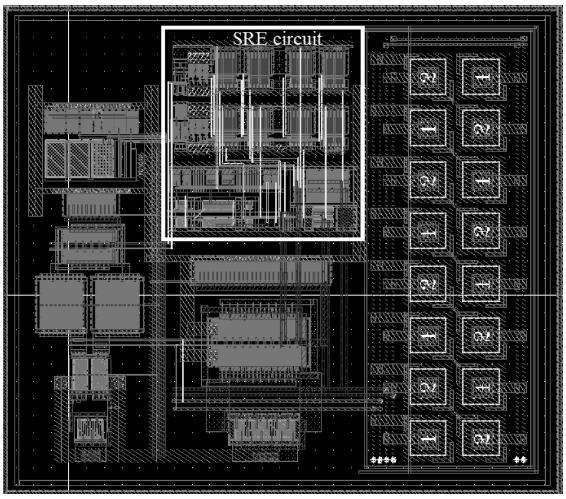

Fig. 7. The layout of the whole OTA with the SRE circuit.

NMOS devices respectively. Secondly, since the driving transistors sized to conduct large enhancement currents are off in a quiescent state, the enhancer saves considerable standby current. Thirdly, the enhancer is separated from the OTA by S1-S16 after enhancing is finished, therefore it does not affect the stability of the OTA.

4. Simulation results

To verify the performance of the proposed SRE circuit, two OTAs with the topology of Fig. 2 are designed to consume almost the same current and have similar frequency responses, one with and the other without the proposed enhancer. The OTAs work in the SHC shown in Fig. 1, with a C_S of 3 pF and a C_L of 2 pF. Under a TT of 27 ℃, the gain and phase margin of the OTAs are 62 dB and 70 degrees respectively. The enhancer totally consumes a current of 200 μA. The circuit is implemented in a 65-nm standard CMOS process with 1.2-V supply voltage and simulated by Spectre() after layout design and extraction. The transient step responses of both designs are shown in Fig. 4 for a 0.6-V input step. Figure 5 depicts the settling time comparison as the input swing varies, which shows that the proposed SRE circuit reduces the settling time by over 50% for a large input swing. The SHCs are simulated to sample and hold a Nyquist-frequency full-swing input at the clock rate of 50 MHz and 100 MHz respectively. For a 100-MHz sampling rate, the output spectra of the two SHCs without and with the enhancer areillustrated in Figs. 6(a) and 6(b) correspondingly. Figure 7 shows the layout of the OTA and SRE circuit, which occupies a chip area of 52 × 56 μm^2. Table 1 gives the FFT performance of the two SHCs, revealing a 44.6-dB SFDR and 43.9-dB THD improvement contributed by the enhancer. Table 2 compares the performance of this work and the SRE circuits presented in Refs. [6, 7]. The proposed SRE circuit consumes 100 times of the standby current of Ref. [6], but its slew rate is 200 times that of Ref. [6], improving the settling time from microsecond order to nanosecond order, which is an extreme optimization. Meanwhile, it consumes almost the same standby current as Ref. [7], whereas its slew rate is 40 times larger than Ref. [7].

Table 1. Performance summary of SHC with/without SRE.

Parameter	SHC without SRE	SHC with SRE
12-bit settling time (ns)	6.5	2.8
SFDR @ 50 MHz (dB)	78.6	81.8
THD @ 50 MHz (dB)	–78.5	–79.7
SFDR @ 100 MHz (dB)	31.7	76.3
THD @ 100 MHz (dB)	–31.0	–74.9
Input swing (V)	1.2	1.2
Supply voltage (V)	1.2	1.2
Technology	SMIC 65-nm 1P7M standard digital CMOS process	

Table 2. Performance comparison.

Parameter	This work	Ref. [6]	Ref. [7]
Slew rate + (V/μs)	1186	4.92	26.7
Slew rate – (V/μs)	1167	5.04	26.6
Settling time (ns)	2.8 (0.025%)	2100 (1%)	None
Standby current (μA)	201	1.09	200
Supply voltage (V)	1.2	1.8	1.8
Technology	65 nm	0.18 μm	0.18 μm

5. Conclusions

A new circuit has been introduced to enhance the slew rate of two-stage OTAs. It works in open-loop mode without any voltage or current feedback to the OTA, thereby avoiding the instability and redesign of the OTA. Simulations show that the circuit reduces the settling time by 50% and improves the SFDR and THD for over 40 dB with a small cost to the standby current. The circuit is particularly useful in low-voltage and power-efficient applications.

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