Optimization of a Cu CMP process modeling parameters of nanometer integrated circuits*

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Abstract: A copper chemical mechanical polishing (Cu CMP) process is reviewed and analyzed from the view of chemical physics. Three steps Cu CMP process modeling is set up based on the actual process of manufacturing and pattern-density-step-height (PDSH) modeling from MIT. To catch the pattern dependency, a 65 nm testing chip is designed and processed in the foundry. Following the model parameter extraction procedure, the model parameters are extracted and verified by testing data from the 65 nm testing chip. A comparison of results between the model predictions and test data show that the former has the same trend as the latter and the largest deviation is less than 5 nm. Third party testing data gives further evidence to support the great performance of model parameter optimization. Since precise CMP process modeling is used for the design of manufacturability (DFM) checks, critical hotspots are displayed and eliminated, which will assure good yield and production capacity of IC.

Key words: chemical mechanical polishing; process modeling; parameter extraction; modeling verification; hotspot

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1. Introduction

Cu chemical mechanical polishing (Cu CMP) is very effective at reducing feature level or local step height and achieves global planarization[1]. However, Cu CMP planarization is influenced by geometric characteristics such as line width, line spacing and pattern density. It is known that various degrees of copper dishing and dielectric erosion occur at different densities and metal line widths[2, 3]. Dishing is defined as the difference between the height of the copper in the trench and that of the dielectric in the spaces surrounding the copper trench in question. Erosion on the other hand, is defined as the difference between the dielectric thickness before Cu CMP and that after Cu CMP.

With the development of Moore's law & more, thickness variation has remained constant at $\pm$10 nm from a 65 to 32 nm node, but the percentage of the total thickness variability has increased from 9% to 20%[4]. To reduce interconnected thickness variation, dishing and erosion must be minimized, which requires an understanding of the layout and process dependencies involved in Cu CMP, and Cu CMP process modeling to predict the dishing and erosion accurately. Although there are many published papers about Cu CMP modeling, the fundamental mechanisms of the micro-wear of the Cu CMP process are not well understood. In addition, most research pays great attention to the chemical and physical understanding of Cu CMP, such as the slurry chemistries, polishing pads, pressure, velocity and abrasion[5, 6]. Some research does take layout pattern into account. The Massachusetts Institute of Technology (MIT)[7−11] brings forward PDSH modeling, but the model considers mainly the great line width and spacing (more than 5 μm), and process experiments and testing are not implemented in the IC mass production process, which is not very good for nanometer integrated circuits. Moreover, for the different slurry chemistries, pad types, polishing pressures and rotational speeds used in different foundries, the Cu CMP process modeling parameters are different. In this paper, based on the Cu process modeling of MIT and Cu CMP process of production process, we extract the Cu CMP modeling parameters to cover the fine size (about 0.09 μm), abiding by the nanometer IC design rule and verified by testing data from the volume production process.

2. Review of the Cu CMP process

A typical Cu CMP tool consists of a rotating platen, which is covered by a pad as shown in Fig. 1. The wafer is mounted upside down in a carrier on a backing film. The retaining ring keeps the wafer in the correct horizontal position. Although both the platen and the carrier are rotating in the same direction, good speed control is important. During chemical mechanical polishing, pressure is applied by a down force on the carrier, transferred to the carrier through the carrier axis and a gimbal mechanism. Also, gas pressure or back pressure is loaded on the wafer. Because high points on the wafer are subjected to higher pressures than lower points, hence, the removal rates are enhanced and planarization is achieved.

The removal rate of Cu can be determined by the competitive reaction between the chemical dissolution of Cu and the mechanical removal of the passivation layer. Cu CMP slurry is

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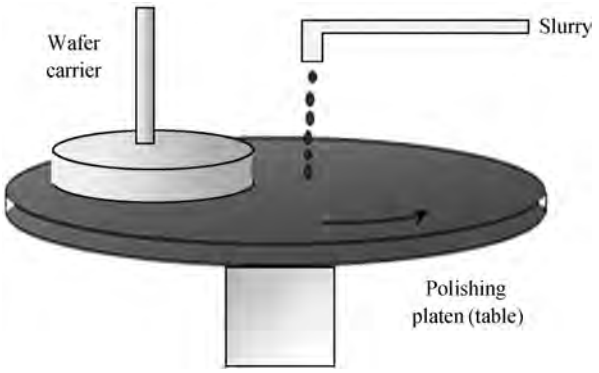

Fig. 1. Polishing mechanisms of the Cu CMP tool.

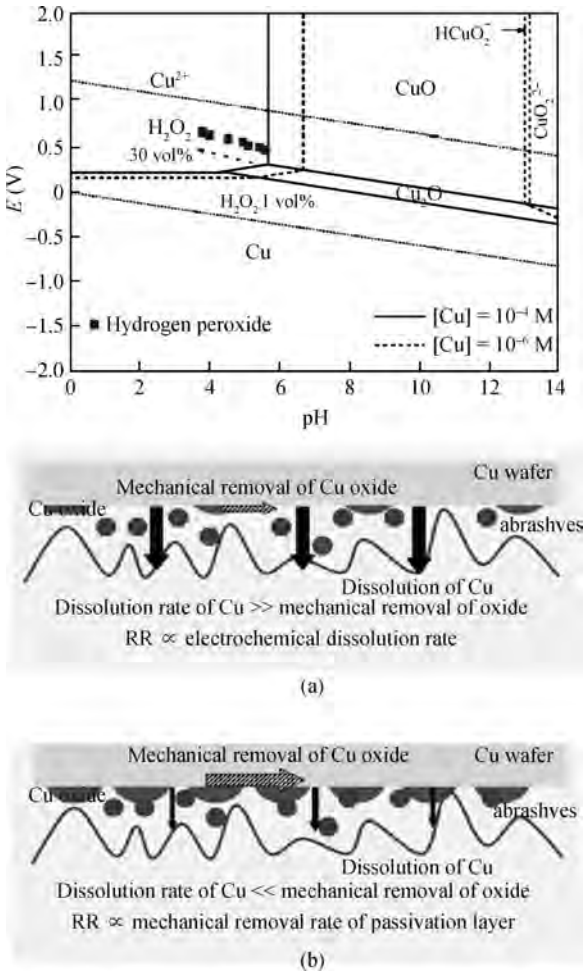

Fig. 2. (a) Chemical and (b) physical mechanisms of CMP polishing[12].

an aqueous solution with the complexing agent, oxidant, and abrasive particles. Generally, the oxidant reacts with the Cu surface in the slurry and Cu ions and Cu oxide are formed. Then, anions of the complexing agent react with the Cu^{2+} or Cu oxide and form a soluble species or insoluble salt as passivation films. The passivation layer is very weak and is removed by chemical dissolution or mechanical abrasion. As Figure 2 shows, the Cu CMP slurry must contain an oxidizing agent to achieve a desirable removal rate of Cu which is decided by the electrochemical dissolution rate and mechanical remove rate of

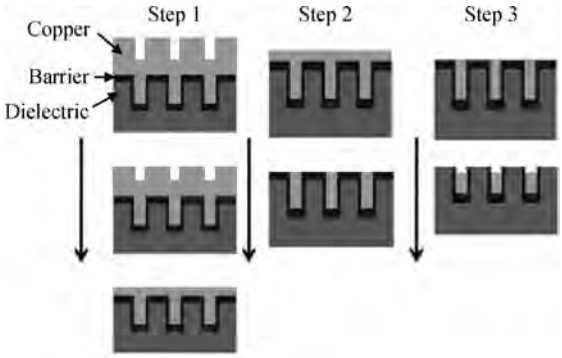

Fig. 3. The three steps of the copper CMP process.

the passivation layer. Hydrogen peroxide (H_2O_2) is the most common oxidizer due to its high oxidizing power in commercial Cu slurries. Slurry pH is also a key factor in determining the removal rate of Cu. Acidic, neutral or alkaline slurries have been investigated for Cu CMP processes.

The Cu CMP process involves the simultaneous polishing of multiple materials: copper, dielectric and barrier. It is necessary to clear the overburdened copper and remove the barrier on top of the dielectric spaces separating the copper interconnecting lines[9, 13]. Now three step polishing processes are used, as shown in Fig. 3. The first step uses a high copper removal rate (typically about 6000 Å/min) to remove a large amount of the overburdened copper without completely clearing it. For this step, a high down force is used, the copper remaining above the barrier film is about 150 nm and the end-point detection is by an eddy current sensor. This second step is intended to clear all the overburdened copper residue across the wafer, while achieving low dishing and erosion. A low removal rate (typically about 1500 Å/min) copper process (compared to the step one process) is used. The pressure is about 1.0 psi, the end-point detection is by optical system, and the ideal result is that zero copper remains, besides the low dishing and erosion. In step 3, a different polishing process setting, a different type of slurry, and possibly a different type of pad are used. The process involves low removal rates for the copper, barrier and dielectric. Compared to the first and second steps, the polishing pad is soft and the process control is by fixed time not by endpoint. The process pressure is about 1.5 psi and the removal rates of the different materials are about 30–40 nm.

3. Extraction and verification of Cu CMP process modeling parameters

3.1. Formulaic expression of Cu CMP modeling

According to Preston's model[15], the polish rate at any position on the wafer is given by Eq. (1), where RR is the material removal rate, K the Preston coefficient, P the polish pressure, and V the relative speed between the platen and the carrier. The chemical contributions are lumped in Preston's coefficient.

$$\mathrm{RR} = KPV. \tag{1}$$

Based on Preston's modeling, MIT developed PDSH modeling for the Cu CMP process[9, 15, 16]. For the first step, the pad

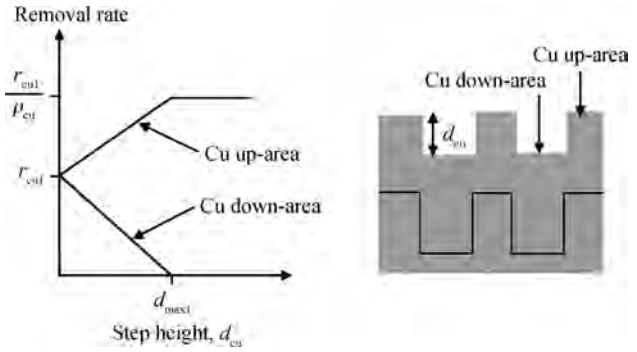

Fig. 4. The first step removal rate diagram.

firstly touches the up-area of the wafer surface, and the pressure of the up-area is thus P/ρ_{cu}, where ρ_{cu} is the effective copper pattern-density. The up-area removal rate is $r_{\mathrm{cu1}}/\rho_{\mathrm{cu}}$ and the down-area is zero, where r_{cu1} is the blanket copper removal rate. As the polishing progresses, the step height d_{cu} decreases as illustrated in Fig. 4. When the step height becomes less than the critical step height d_{max1}, the pad touch, the down-area surface and the pressure exerted on the down-area becomes non-zero. By Hooke's law, this non-zero down-area pressure increases linearly as the step-height decreases, while the up-area pressure decreases linearly as the step-height decreases. Step height reduction continues until the step height is eliminated and the copper surface is flat. The up-area copper removal rate decreases from $r_{\mathrm{cu1}}/\rho_{\mathrm{cu}}$ to r_{cu1} and the down-area removal rate increases from zero to r_{cu1}.

The up-area and down-area removal rates are expressed mathematically in Eqs. (2)–(4), where $\mathrm{RR_{up}}$ is the up-area removal rate, $\mathrm{RR_{dn}}$ is the down-area removal rate, Z_{dn} is the down-area thickness based on some plane, Z_{up} the up-area thickness based on some plane and d_{cu} the step height (in step 1) or the dishing (in steps 2 and 3). Given the appropriate boundary conditions, $\mathrm{RR_{up}}$, $\mathrm{RR_{dn}}$, Z_{up} and Z_{dn} can be obtained, so one can get the step height, the surface thickness and the time to clean some material at any spatial position of interest. Equations (3)–(5) show the time dependency of Z_{up} and Z_{dn}, in which Z_{up0}, Z_{dn0} and d_0 are initial data of Z_{up}, Z_{dn} and d_{cu}, and t is process time. In other words, the wafer topography will achieved using this semi-experiential modeling. The second and third steps are handled the same way, only different materials are eliminated and there are different boundary conditions. The following equations are no longer a description about the second and third steps formula.

$$\begin{cases} \mathrm{RR_{up}} = \dfrac{r_{\mathrm{cu1}}}{\rho_{\mathrm{cu}}}, \\ \mathrm{RR_{dn}} = 0, \end{cases} \qquad d_0 > d_{\mathrm{max1}}, \tag{2}$$

$$\begin{cases} \mathrm{RR_{up}} = r_{\mathrm{cu1}} + r_{\mathrm{cu1}} \dfrac{1-\rho_{\mathrm{cu}}}{\rho_{\mathrm{cu}}} \dfrac{d_{\mathrm{cu}}}{d_{\mathrm{max1}}}, \\ \mathrm{RR_{dn}} = r_{\mathrm{cu1}} \left(1 - \dfrac{d_{\mathrm{cu}}}{d_{\mathrm{max1}}}\right), \end{cases} \qquad 0 < d_0 \leqslant d_{\mathrm{max1}}, \tag{3}$$

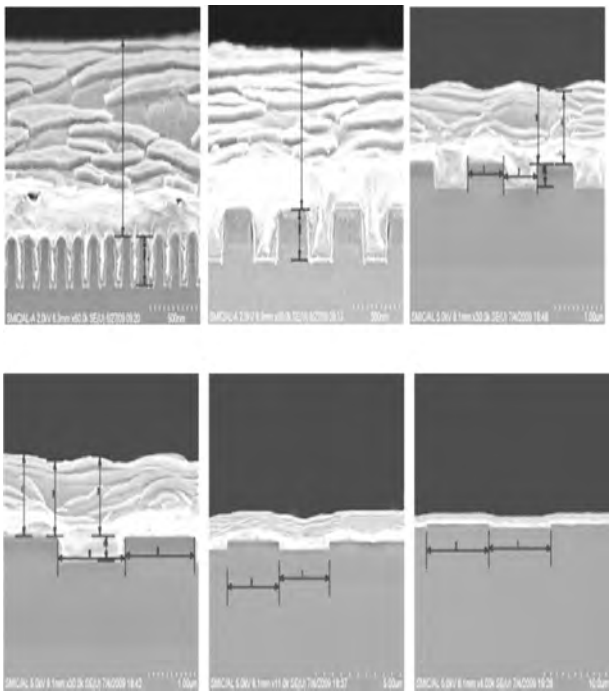

Fig. 5. SEM images with line width: 0.09 μm, 0.3 μm, 0.75 μm, 1.5 μm, 3 μm and 10 μm.

$$\begin{cases} \dfrac{\mathrm{d}z_{\mathrm{up}}}{\mathrm{d}t} = -\mathrm{RR_{up}}, \\ \dfrac{\mathrm{d}z_{\mathrm{dn}}}{\mathrm{d}t} = -\mathrm{RR_{dn}}, \end{cases} \tag{4}$$

$$\begin{cases} z_{\mathrm{up}} = z_{\mathrm{up0}} - r_{\mathrm{cu1}} t + d_0(1-\rho_{\mathrm{cu}})(\mathrm{e}^{\frac{-t}{\tau_{11}}} - 1), \\ z_{\mathrm{dn}} = z_{\mathrm{dn0}} - r_{\mathrm{cu1}} t - d_0 \rho_{\mathrm{cu}}(\mathrm{e}^{\frac{-t}{\tau_{11}}} - 1), \\ \tau_{11} = \dfrac{d_{\mathrm{max1}} \rho_{\mathrm{cu}}}{r_{\mathrm{cu1}}}. \end{cases} \tag{5}$$

The post-electroplating (ECP) topography strongly depends on layout patterns. From the SEM pictures of the wafer cross section, such as Fig. 5[17, 18], we can get the conclusion that fine lines have the largest copper height. When the density is 50% and the line widths are 0.09, 0.3, 0.75, 1.5, 3 and 10 μm, the copper heights are 9910, 8080, 7723, 8038, 7123 and 7213 Å respectively. However, the PDSH modeling fails to take into account die scales variation caused by the electroplating process. Contact mechanics[19–21] can accommodate the long range initial thickness variation caused by copper electroplating, and also accounts for the evolution of surface topography as polishing progresses. If the pad is treated as a massive elastic body, and the wafer a rigid body, then the pad displacement W and the contact pressure P are related as given in Eq. (6), where v is Poisson's ratio and E the elasticity of the pad. If the initial displacement w_0 of wafer and pad is known, the contact pressure P can be computed and vice-versa. Once the pressure is computed, it can be substituted to compute the material removal rate used in Eqs. (2)–(5).

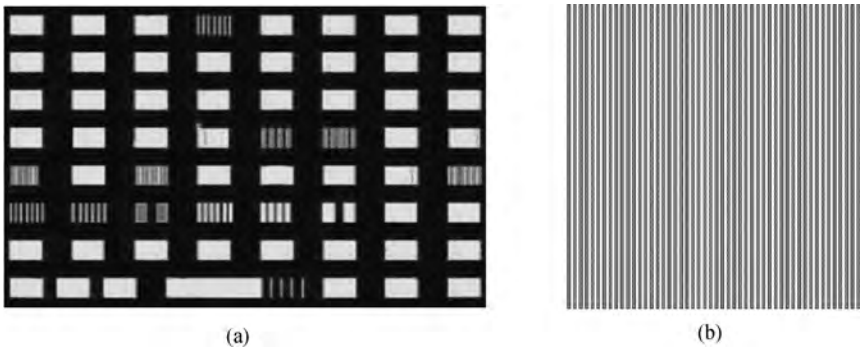

Fig. 6. (a) Single-level copper testing mask. (b) Physical test structure.

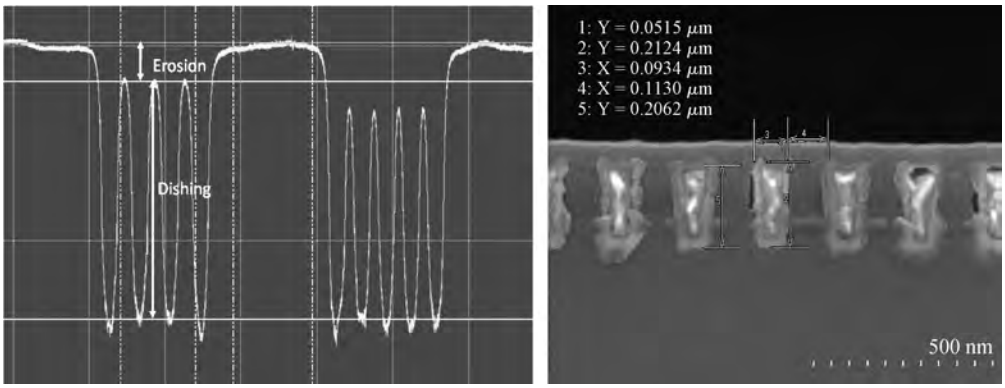

Fig. 7. AFM line scan curve and SEM photo from SMIC.

$$W(x,y)=\frac{1-v^2}{\pi E}\iint_A \frac{P(\xi,\eta)}{\sqrt{(x-\xi)^2+(y-\eta)^2}}\mathrm{d}\xi\mathrm{d}\eta+w_0. \tag{6}$$

3.2. Testing chip design and process implementation

To capture characterization of Cu CMP process pattern dependencies, a mask has been designed as shows in Fig. 6(a). It is a single level mask with dimensions of about 5 mm by 5 mm, which contains 64 array structures. The size of each array is about 300 μm by 300 μm; the space between neighboring arrays is also 300 μm, which is designed to decouple interactions among structures and also serve as measured surface profile reference points. To mimic interconnection, arrays of lines and spaces form the fundamental test structure for the study of pattern dependencies. Figure 6(b) is an array structure that incorporates two regions or elements. The "array" region gives information about array erosion and local dishing within array lines in the Cu CMP process. As a whole, the range of feature size is about 0.09 μm to 40 μm and the metal density scope is from 10% to 91%. The feature size is small enough to display characterization of 65 nm processes, so the conclusions obtained from this paper will be more accurate and useful.

The mask experiment is carried out in the 65/45 nm process of volume production, which has four steps: the first is the ECP process, the second is the P_1 step of the Cu CMP process, the third is the P_2 step of the Cu CMP process and the fourth is the P_3 step of the Cu CMP process. To measure dishing and erosion, a surface profile measurement is taken with an atomic force microscope (AFM), which is a two dimensional measurement that gives the relative height of the different regions of the surface in question. To investigate the evolution of copper thickness, a copper thickness measurement is necessary. For the great high aspect ratio, it is very difficult to use a common tool, such as the Metapulse 300 from Rudolph, to measure thickness directly. Therefore, we cut the test structures, obtained cross-section images, and then measured them using the SEM photo. Figure 7 shows the AFM scan curve and SEM photo, from which dishing, erosion and thickness can be measured.

3.3. Extraction and verification of process modeling parameters

Extraction of modeling parameters involves fitting the model equations to the measured experimental data with low RMS error. The constraints of low root mean square (RMS) error are intended to force the parameters to take values in a given range in accordance with the physical interpretation of these parameters. The extraction of the model parameters related to each of the Cu CMP three steps is done independently. The methodologies for extracting the model parameters in each step are described in Fig. 8. The overall extraction criteria are the minimization of the RMS error between the filtered measured data and the simulation data from modeling.

To check the accuracy of the extraction procedure, at least two things must be done. Firstly the extraction in each step of the Cu CMP process must be checked for accuracy, and then a full simulation of the entire process should be done. The ex-

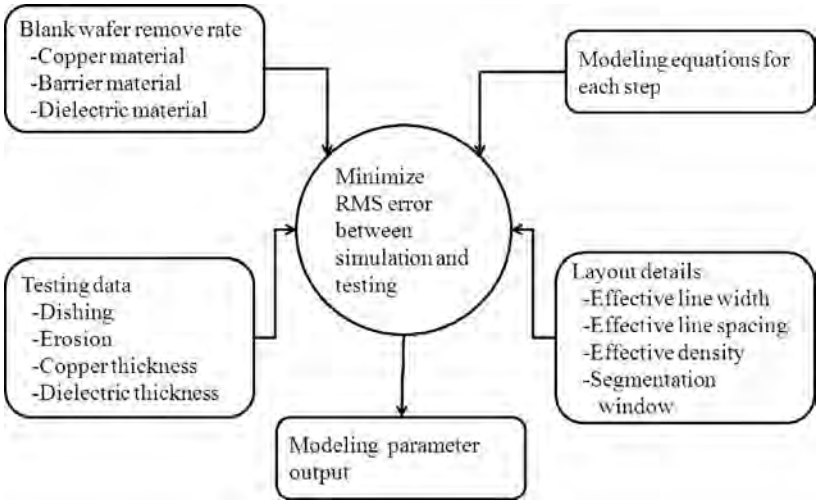

Fig. 8. Modeling parameter extraction procedure.

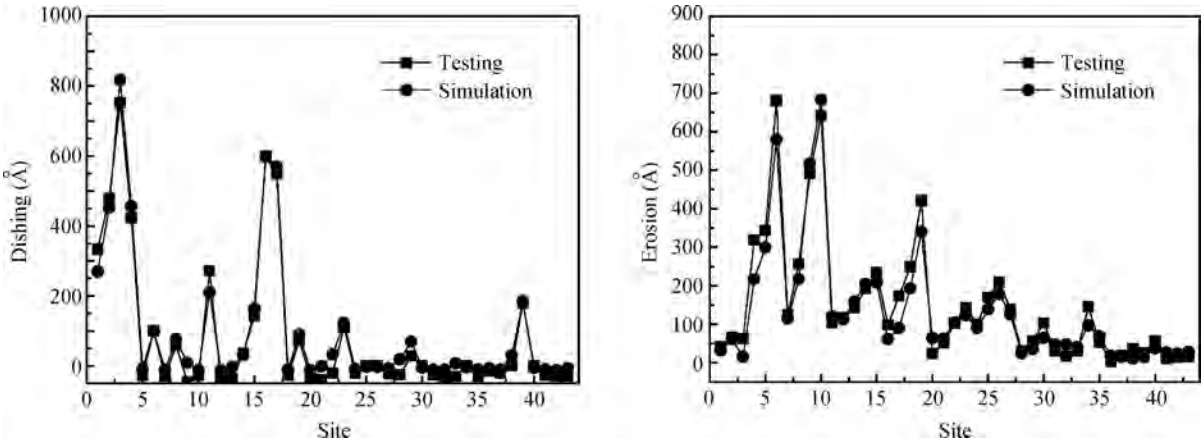

Fig. 9. Model prediction versus test data.

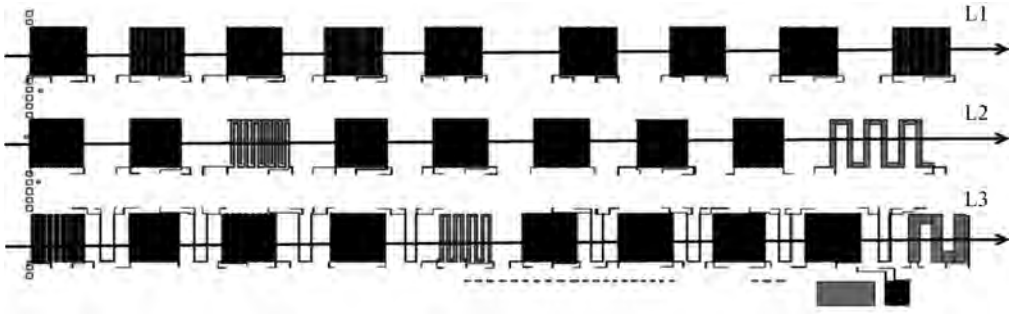

Fig. 10. 65 nm test chip layout from SMIC.

tracted modeling parameters in all three steps are used to simulate the copper thickness, dishing and erosion at several sites on the die. The dishing and erosion simulation results should be compared to the measured dishing and erosion. Figure 9 shows the model simulation data versus testing data, which demonstrates the same trend and the largest deviation less than 5 nm. The CMP model has great accuracy, meets the requirements of industry (RMS error < 15 nm) and can be used for volume production prediction.

In order to test the modeling accuracy further, we got some test data from production process. Figure 10 is the 65 nm test chip supplied by SMIC, which is polished and then tested. In Fig. 10, the line L1, L2 and L3 include 9, 9 and 10 modules from left to right respectively. Figure 11 shows testing pictures by the AFM, from which we can get dishing and erosion data. After using our modeling software to simulate the test chip layout, we can get some prediction data of dishing and erosion. Figure 12 is the dishing and erosion data, comparing between test and prediction. The RMS errors of dishing and erosion are 3.5 nm and 4.5 nm respectively, which also show great accu-

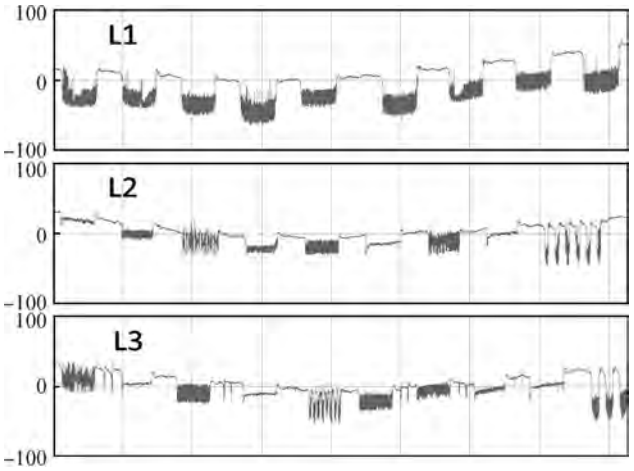

Fig. 11. AFM testing picture.

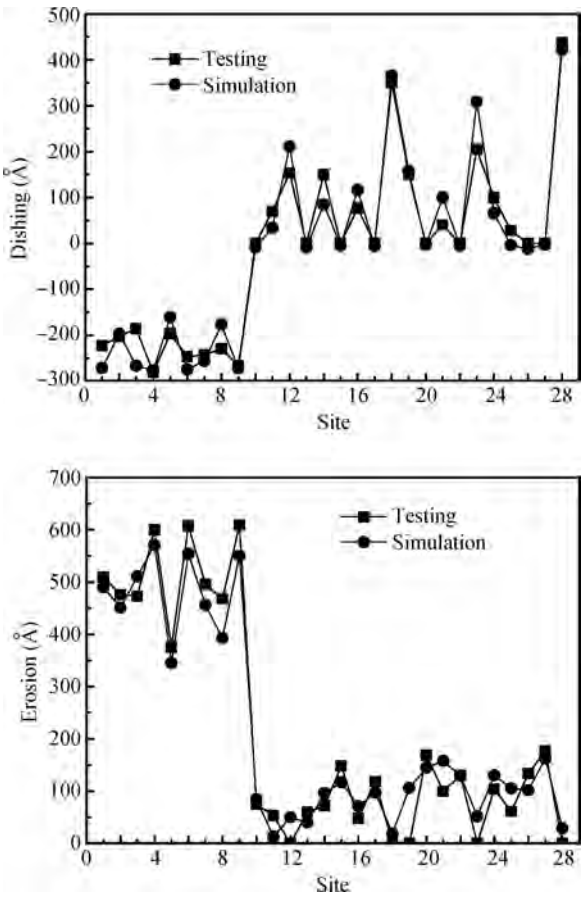

Fig. 12. Cu CMP modeling test.

racy.

3.4. Cu CMP process modeling application

The Cu CMP process model can be used to predict the performance of Cu CMP such as dishing and erosion which is highly dependent upon the pattern characteristics. For a fixed pattern density as illustrated in Fig. 13, an increasing line width reflects increasing dishing and decreasing copper thickness. As the line width increases, the pad asperity easily touches the copper in the trench and so the wide line dishing increases and

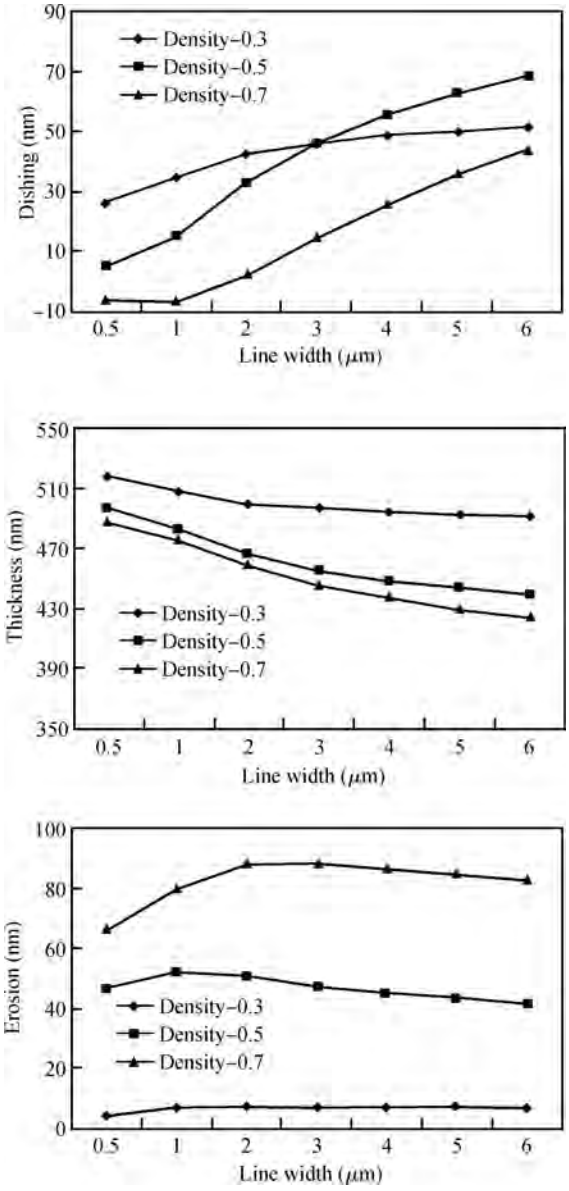

Fig. 13. Cu CMP modeling predictions.

thickness decreases. Given the same line width, it is evident from Fig. 13 that erosion increases with increasing pattern density. The effective pressure in the dielectric location (for high pattern density) will be high, which enhances the aggressiveness of the slurry towards the dielectric, and assists in mechanical abrasion. These effects account for the dramatic increase in erosion with increasing patter density.

Cu pooling or Cu residual is a common issue related to the CMP process. It is a pool of Cu residuals between metal lines, can cause potential catastrophic shorting and will have an impact on functional yield. Since the CMP process model has good accuracy, it can be used as a DFM checking tool to predict the potential catastrophic shorting or opening. The application process is shown in Fig. 14. There are various hotpot rules in the CMP simulation tool including excess metal thickness variation, surface topography variation and excess density variation. Figure 15 shows the hotspot display and analyses, by which designers can eliminate some critical hotspots before process application.

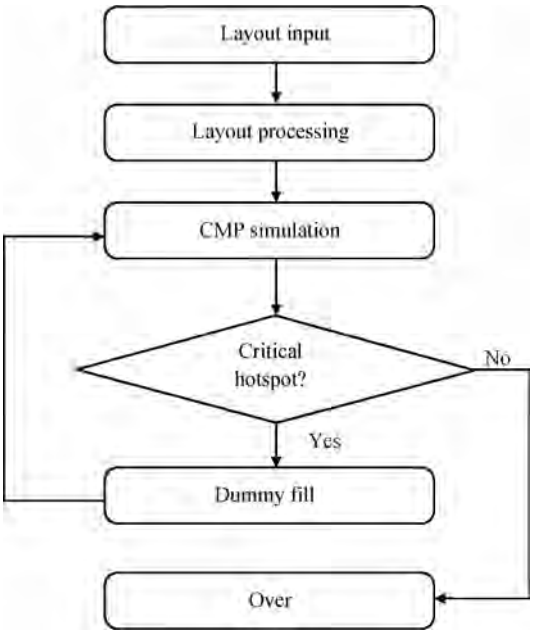

Fig. 14. Application process of CMP modeling.

4. Conclusion

In this paper, we introduce the copper CMP process and CMP modeling parameter extraction and verification. The compared results between the model predictions and test data show the Cu CMP process models have good accuracy and the maximum error is less than 5 nm. The verified Cu CMP modeling is used to forecast nanometer IC design hotspots to avoid Cu residue or line opening. By checking and eliminating critical hotspots, it will assure a good functional yield and production capacity of IC.

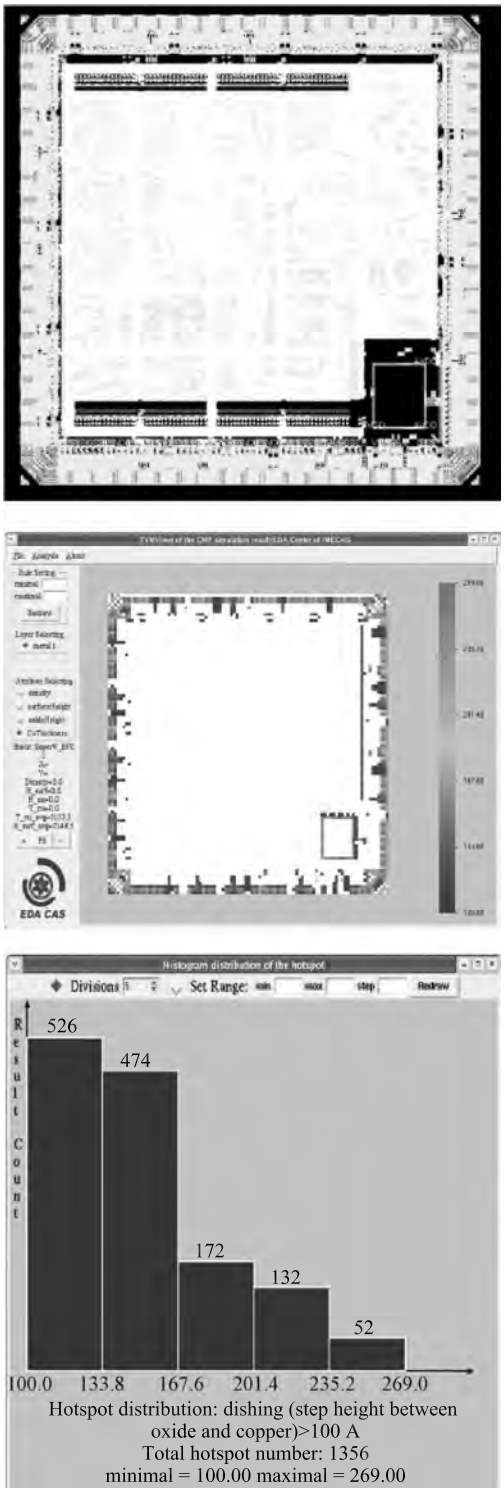

Fig. 15. Hotspot check and analyses.

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