A high-efficiency, low-noise power solution for a dual-channel GNSS RF receiver

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Abstract: A high-efficiency low-noise power solution for a dual-channel GNSS RF receiver is presented. The power solution involves a DC–DC buck converter and a followed low-dropout regulator (LDO). The pulse-width-modulation (PWM) control method is adopted for better noise performance. An improved low-power high-frequency PWM control circuit is proposed, which halves the average quiescent current of the buck converter to 80 μA by periodically shutting down the OTA. The size of the output stage has also been optimized to achieve high efficiency under a light load condition. In addition, a novel soft-start circuit based on a current limiter has been implemented to avoid inrush current. Fabricated with commercial 180-nm CMOS technology, the DC–DC converter achieves a peak efficiency of 93.1% under a 2 MHz working frequency. The whole receiver consumes only 20.2 mA from a 3.3 V power supply and has a noise figure of 2.5 dB.

Key words: GNSS; power solution; DC–DC converter; pulse-width-modulation; low-dropout regulator
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1. Introduction

Global navigation satellite system (GNSS) RF receivers have become a standard feature in portable electronic products like mobile phones, tablets, notebooks and personal navigation devices. During recent years several successful RF receivers have been reported[1−4]. Although currently the United States global positioning system (GPS) is the only completed GNSS system, other systems like the Russian GLONASS, the Europe Union's Galileo and the Chinese Compass all have specific schedules[5−7].

With several GNSS systems available, using multiple constellations could improve the accuracy of the resulting position significantly, especially in environments where the satellite visibility is impaired[8]. However, a multi-GNSS RF receiver means the power consumption is multiplied which is the bottleneck in portable electronic devices. Hence, high efficiency is demanded for the power supply converter. Considering the current consumption of a regular multi-channel GNSS receiver is less than 100 mA, this light load increases the difficulty of achieving high efficiency. Additionally, the performance of a RF receiver is sensitive to power supply noise and interference. Thus, low electromagnetic interference (EMI) and a high power supply rejection ratio (PSRR) is another crucial requirement for the power supply[9, 10].

Considering the above mentioned, this work presents a high efficiency, low noise and high PSRR power supply solution for a dual-channel GNSS RF receiver, which involves a PWM DC–DC buck converter and a high PSRR LDO, as shown in Fig. 1.

The specific architecture of the power supply solution is shown in Fig. 2. The DC–DC converter transforms the battery voltage to around 2 V with a 93.1% peak efficiency. For the purpose of achieving a fixed voltage, which is equivalent to a fixed duty cycle, two fundamental control methods, pulse-width-modulation (PWM) and pulse-frequency-modulation (PFM) have been widely used. As PFM converters have an unpredictable operating frequency to retain a constant-on-time, they suffer from very poor EMI performance. On the other hand, PWM has a fixed operating frequency which makes the induced noise and interference easier to be filtered. Consequently, in this design, the PWM control method is selected to achieve a better noise performance. The major drawback of PWM is low efficiency under light-load conditions because the circuit still works at a relatively high frequency and the quiescent current does not decrease[11]. To overcome this problem a novel PWM control strategy is proposed, which not only halves the average quiescent current but also enables the DC–DC converter to retain high efficiency even at tens of MHz working frequency to reduce the PCB board area and avoid interference influence on the IF in-band signal. The size of the output stage has also been optimized to improve efficiency. The followed LDO is used to regulate the switching noise and to provide a clean voltage source for the noise-sensitive GNSS RF receiver.

In order to protect the circuit during the start-up phase, a novel soft-start circuit is proposed. The soft-start circuit eliminates the inrush current by using a comparator and an approximate current sample circuit. Avoiding the use of a DAC or large off-chip capacitor, the design complexity is reduced.

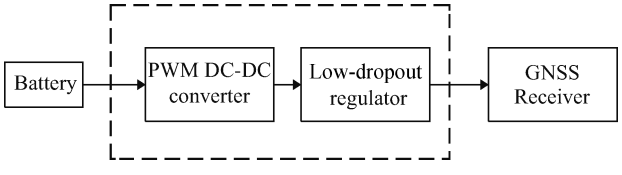

Fig. 1. Block diagram of the power supply solution.

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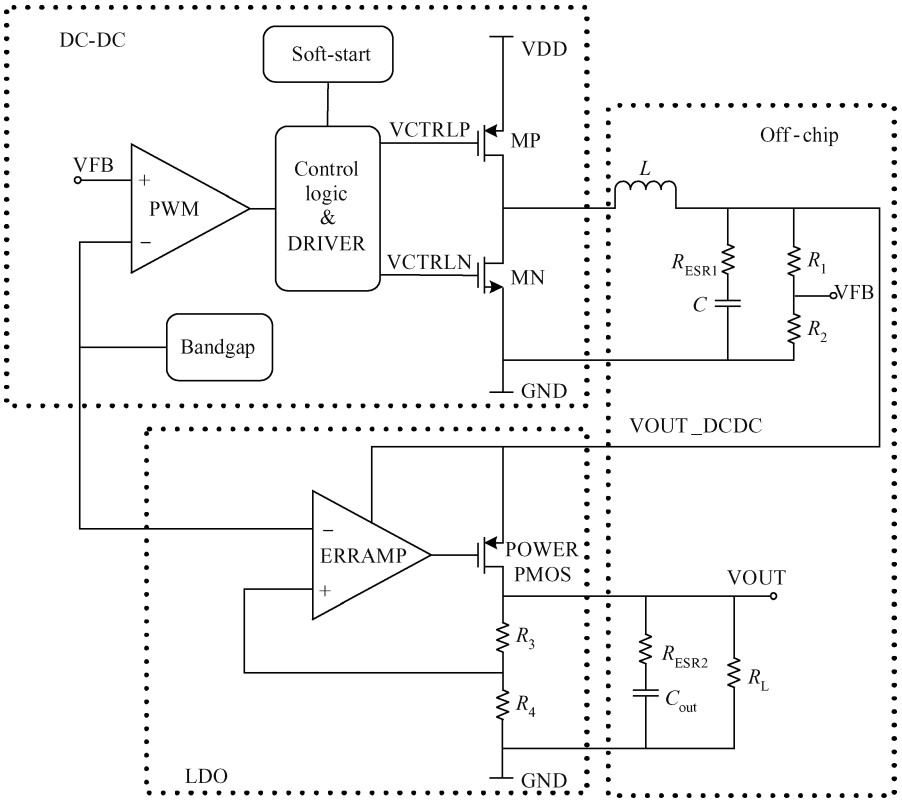

Fig. 2. Specific architecture of the power supply solution.

With this power solution the dual-channel GNSS receiver consumes only 20.2 mA from a 3.3 V power supply and has a noise figure of 2.5 dB.

2. Circuit design

2.1. An improved high frequency PWM control scheme

Generally, a conventional current-mode PWM control circuit involves an error amplifier to compare the feedback output voltage with the reference. Together with the sensed inductor current and ramp signal, the comparator and control logic generate the PWM signal[12]. Unfortunately, the adoption of an error amplifier and comparator will result in a decline of efficiency as the operating frequency increases because a broader bandwidth requires more current of the control circuit.

A high frequency PWM control circuit is proposed in Ref. [13], a voltage-to-current scheme replaced the error amplifier and comparator and the bandwidth is significantly expanded. However, the mirrored error current is bypassed to V_{DD} every half of the clock cycle and the power of the OTA is certainly wasted. This drawback increased the average quiescent and decreased the efficiency. Another problem is the stacked four transistors of the OTA limited the range of the battery voltage range.

In this design, a revised low power high frequency PWM control circuit is proposed, as shown in Fig. 3. The PMOS transistors MP0–MP2 and NMOS transistors M1–M4 form an operational transconductance amplifier (OTA) which compares the feedback output voltage with reference voltage and transforms the error voltage to error current. The g_m of the differential pair MP1 and MP2 determines the gain of the control circuit. M1–M4 are implemented as a low voltage cascode current mirror to earn more voltage margin. With $V_{err} = V_{FB} - V_{REF}$, we can get the error current to be expressed as:

$$I_{err} = 0.5(I_{bias} + g_m V_{err}). \tag{1}$$

The error current is then mirrored to modulate the duty cycle of the PWM control signal via switch transistors M5 and MP3–MP6. CLKP and CLKN are the opposite clock signal provided by the external circuit. When CLKN is high, transistor MP4 is shut down and the error current is bypassed to VDD via MP3. To avoid the waste of the OTA quiescent current, a PMOS transistor MP7 is added to shut down the OTA periodically. This technique saves 50% of power consumption and the whole average quiescent current of the buck converter is 80 μA. At this time the B end of the capacitor C_0 is charged to the V_{DD} as transistor MP5 is turned on and the output control signal is high; When CLKP is high, transistor MP4 is turned on and MP5 is shut down. The capacitor C_0 is discharged by the mirrored error current, in other words, the gate voltage of MP6 decreases with a slope of NI_{err}. The output control signal remains high until the decreased voltage of V_X exceeds the threshold of the PMOS transistor V_{THP}. R_1, R_2, C_1 and C_2 form an RC filter network to avoid the interference to OTA from the clock signal. Figure 4 shows the waveforms of CLKP, V_x and Control. From the charge conservation, we can get the relationship:

$$V_{THP}C_0 = NI_{err}(M - D)T_{clk}. \tag{2}$$

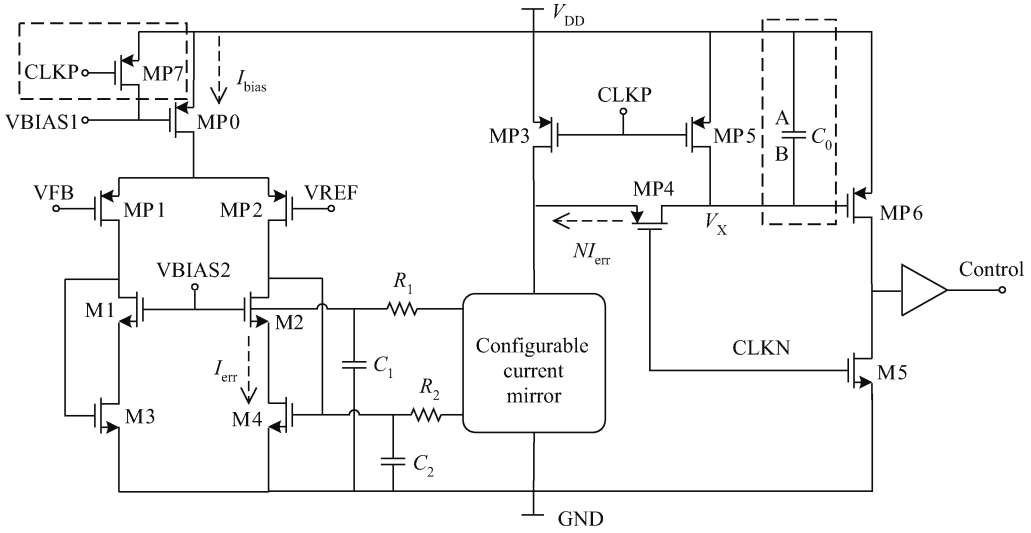

Fig. 3. Proposed PWM control circuit.

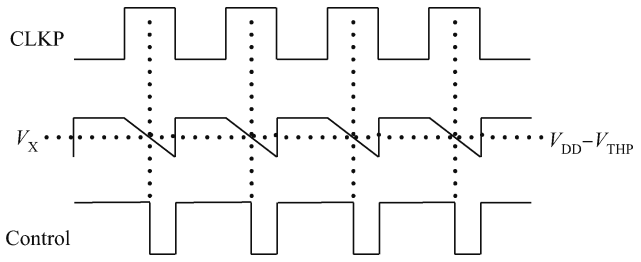

Fig. 4. Waveforms of CLKP, Vx and Control.

The expression of the duty cycle M of Control can be further derived:

$$M = D + \frac{V_{THP}C_0}{NI_{err}T_{clk}} = D + \frac{V_{THP}C_0}{0.5N(I_{bias} + g_m V_{err})T_{clk}}, \quad (3)$$

where D is the duty cycle of the clock (in this illustration D is 0.5), and N is the ratio of the current mirror digitally controlled by SPI to satisfy varied operating frequency. From Eq. (3) we would know that if V_{FB} exceeds V_{REF}, V_{err} will increase and induce a narrower M. The duty cycle M operates on the power stage and results in a decreased output voltage eventually. So a negative feedback system is established.

2.2. Efficiency optimization

Maintaining high efficiency at light-load conditions is the biggest challenge for PWM buck converters. As the load is decreased, traditional PWM buck converters commonly exhibit a rapid drop-off in efficiency.

In this design, the receiver consumes about 32 mA from the 1.8 V power supply and the operating frequency could be several tens of MHz. Considering the sources of power loss analyzed in Ref. [14], besides the conduction loss, the impact of MOSFETS switching and gate-drive losses become significant.

The power MOSFETS conduction loss is given by

$$P_{cond} = \frac{I_{rms}^2(a+1)R_{ds0}}{aW_p}, \quad (4)$$

where R_{ds0} is the resistance per unit width, I_{rms} is the RMS load current, a is the width ratio of NMOS-to-PMOS transistor, and W_p is the width of power PMOS transistor.

The power MOSFETS switching loss is given by

$$P_{sw} = f_s C_{out} V_{DD}^2 = f_s(C_{gs0} + 2C_{gd0} + C_{db0})(1+a)W_p V_{DD}^2, \quad (5)$$

where C_{gs0}, C_{gd0} and C_{db0} are capacitances per unit width, and f_s is the operating frequency.

The gate-drive loss is given by

$$P_{gate} = f_s\left[\frac{f^n - 1}{f - 1}(C_i + C_o) + C_{g0}W_p\right](1+a)V_{DD}^2, \quad (6)$$

where f and n is the tapering factor and series number of the driver chain, respectively.

From Eqs. (4)–(6) we notice that the total loss $P_{total} = P_{cond} + P_{sw} + P_{gate}$ could be optimized by the adjustment of W_p with fixed load and operating frequency. In this work the optimized W_p is chosen to be 8000 μm as $\partial P_{total}/\partial W_p = 0$.

2.3. A novel soft-start circuit

During the start-up phase, the reference voltage is established but the feedback voltage is increased slowly. This unbalanced state would induce an inrush current and damage the electronic device. To avoid this phenomenon, a soft-start circuit is required. Traditional soft-start circuits usually need a large off-chip capacitor or a DAC converter. As a result they suffer from either extra PIN and PCB board area or increased design complexity.

A novel soft-start circuit based on a current limiter is implemented, as shown in Fig. 5, the use of a DAC or large off-chip capacitor is avoided.

A PMOS transistor M15 is parallel with the power PMOS transistor M16 to approximately sample the current in the proportion of 1:1000. The control signal from the PWM module would not act on the power transistor directly. If the sample current exceeds the limited value, the soft-start circuit will restrain the control signal and shut the power transistor down.

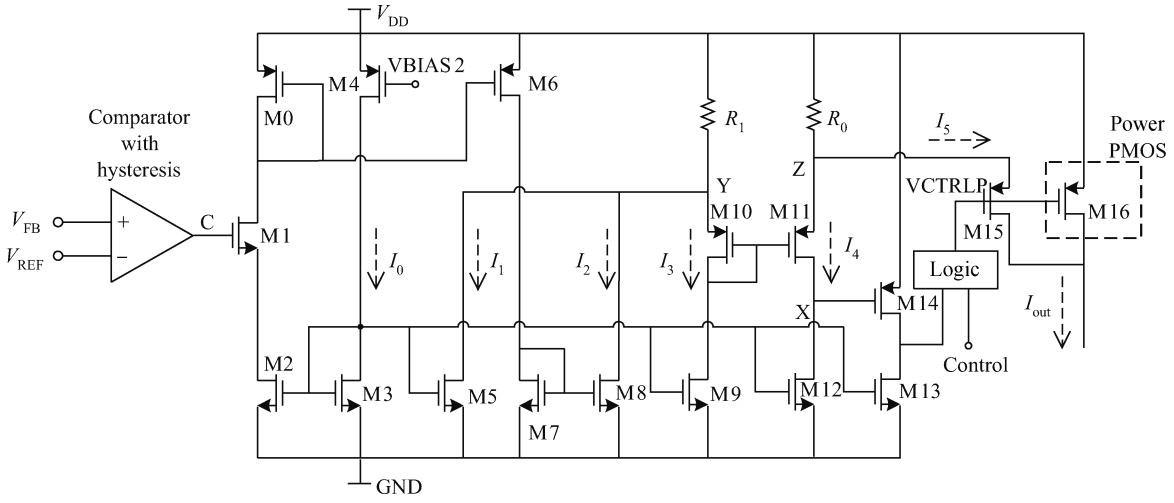

Fig. 5. Current limiter based on soft-start circuit.

During the start-up phase, the output of the hysteresis comparator is low and M1 is shut down. As the proportion of the current mirror is always 1:1, the floating current of R_1 is $2I_0$. I_3 is equal to I_4 under the condition

$$2I_0R_1 = (I_0 + I_5)R_0. \tag{7}$$

I_5 is equal to $9I_0$ when R_1 is $5R_0$. If I_5 exceeds this, the voltage of node Z would be lower than Y. As a result, the additional current of I_4 would discharge node X and transistor M14 would be turned on. The switch signal processed by digital logic will then shut the power transistor down to avoid the inrush current. The limited current is 90 mA when I_0 is 10 μA.

There is a problem with the fixed limited current. As the limited current is required higher than the maxim load current, an overshoot voltage would be induced during the start-up phase. As a result a comparator with hysteresis is adopted to change the limited current in different states. When the feedback voltage is close to the reference, the output of the comparator is high. I_3 is equal to I_4 when

$$3I_0R_1 = (I_0 + I_5)R_0. \tag{8}$$

I_5 is equal to $14I_0$ when R_1 is $5R_0$. Consequently the limited current is increased to 140 mA during the normal working phase.

2.4. LDO

The switching noise brought by the DC–DC converter leads to the need for high power supply rejection (PSR) for the followed LDO. For a conventional LDO, the PSR is mainly limited by the gain of the error amplifier and the PSR of the bandgap circuit[15].

A conventional structure composed by an error amplifier, a unit-gain buffer, a power transistor and a feedback network is adopted in this work, as shown in Fig. 6. The folded cascode structure provides a high gain and wide range of input voltage. As the high output impedance of the error amplifier and the large parasitic capacitance at the gate of the power transistor form a pole which is at a rather low frequency, the unit-gain buffer is required for isolation. Also, a pole-zero tracking compensation replaces the conventional Miller compensation[16]. Transistor M10 and capacitor C_Z contribute a zero changing with the regulator output pole. This compensation scheme boosts the open loop DC gain and makes the frequency response load independent.

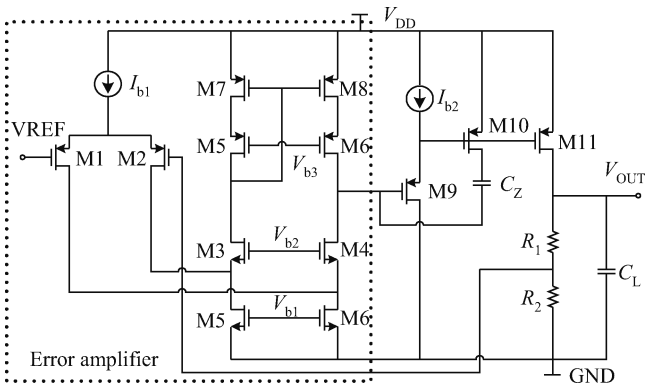

Fig. 6. Structure of the LDO.

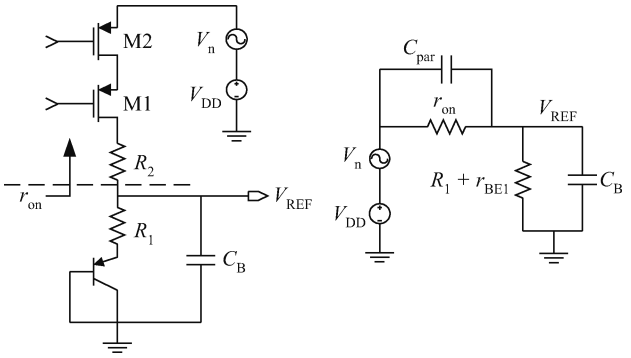

Fig. 7. Output stage of the bandgap and equivalent small signal model.

Figure 7 shows the output stage of the bandgap circuit and its equivalent small signal model. From the small signal model

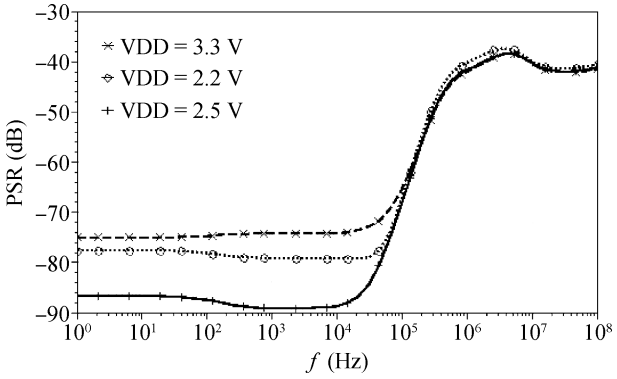

Fig. 8. Simulated PSR of the LDO.

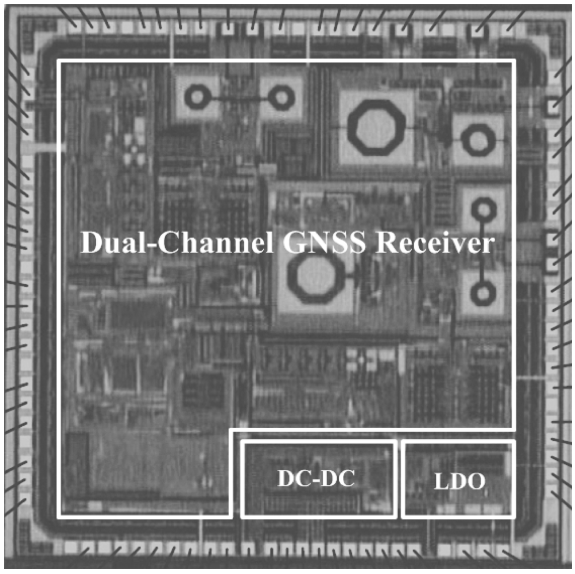

Fig. 9. Chip microphotograph.

we can get the power supply rejection:

$$\mathrm{PSR} = \left|20\lg\frac{\mathrm{Ripple_{VREF}}}{\mathrm{Ripple_{VDD}}}\right| = \left|20\lg\left(1+\frac{r_{\mathrm{on}}}{R_1+r_{\mathrm{BE1}}}\right)\right|. \quad (9)$$

From Eq. (8) we notice that a larger r_{on} could improve the PSR of the bandgap circuit. As a result the cascode current mirror is used. The simulated PSR of the LDO is shown in Fig. 8. With a supply voltage of 2.5 V, the LDO achieves a PSR better than −86 dB up to 10 kHz. The PSR is still around −40 dB up to 100 MHz.

3. Experimental results

The power solution has been implemented with commercial 0.18-μm CMOS technology and the chip microphotograph is shown in Fig. 9. The whole active area of the power solution is 1.2 mm × 0.3 mm = 0.36 mm^2. Figure 10 shows the measured DC–DC and LDO output voltage.

The peak efficiency of the DC–DC converter is 93.1% under the light load conditions, as shown in Fig. 11(a). The dual-channel GNSS receiver consumes 31.8 mA from the output voltage of the LDO which meets our design specifications. As the load increases, the conduction loss becomes dominant and

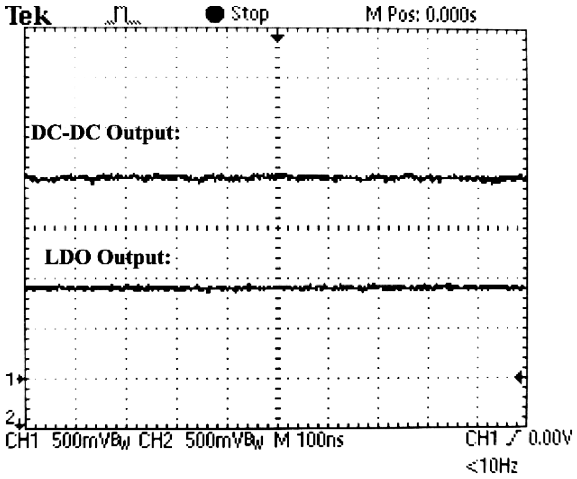

Fig. 10. Measured output voltage of the DC–DC and LDO.

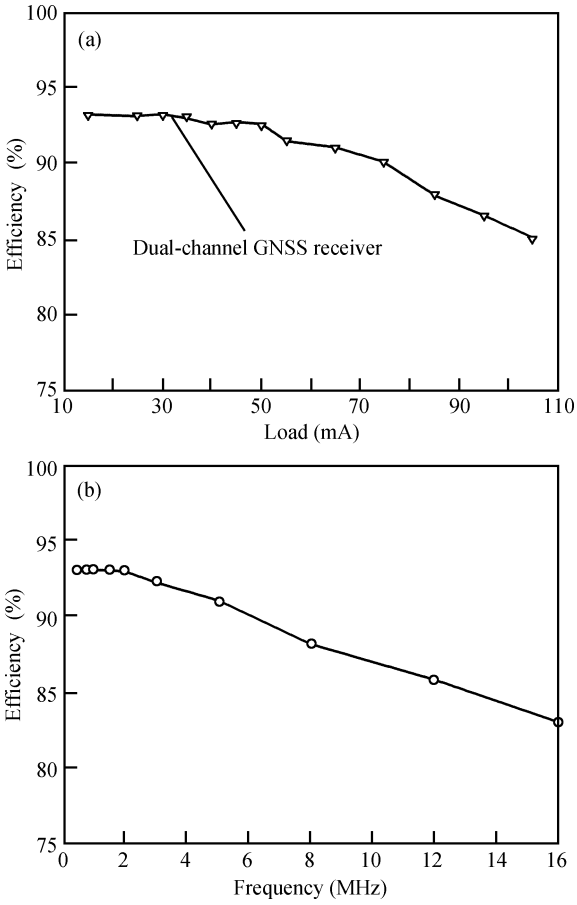

Fig. 11. Measured efficiency of the DC–DC versus (a) output load and (b) frequency.

reduces the efficiency. We are glad to see the efficiency still remains above 85% when the load current exceeds 100 mA, which means this power solution is also suitable for multi-channel GNSS receivers. Table 1 summarizes the main performances of the DC–DC converter. Table 2 shows the comparison of the efficiency when the load current is 30 mA. The efficiency of this work is even higher than the product with PFM control. This result proves the quiescent current of the control circuit is rather low and the optimization of the output stage is

Table 1. Summary of the DC–DC converter performances.

Index	Control method
Technology	CMOS 180 nm
Area	0.21 mm^2
Peak efficiency	93.1%
Quiescent current	80 μA
Maxim working frequency	16.368 MHz

Table 2. Comparison of efficiency when the load current is 30 mA.

Parameter	Efficiency (%)	Control method
This work	93.1	PWM (2 MHz)
Ref. [17]	87.2	PWM (2 MHz)
Ref. [18]	85	PWM (3 MHz)
Ref. [19]	84	PWM (600 kHz)
Ref. [20]	91	PFM

Table 3. Power comparison of published GNSS receivers.

Parameter	Technology	Power (mA)	Comments
This work	CMOS 180 nm	20.2	Dual-channel
Ref. [1]	CMOS 180 nm	23	Single-channel
Ref. [2]	CMOS 65 nm	25.8	Single-channel low power mode
Ref. [3]	CMOS 180 nm	25	Single-channel
Ref. [4]	CMOS 180 nm	31.3	Dual-channel

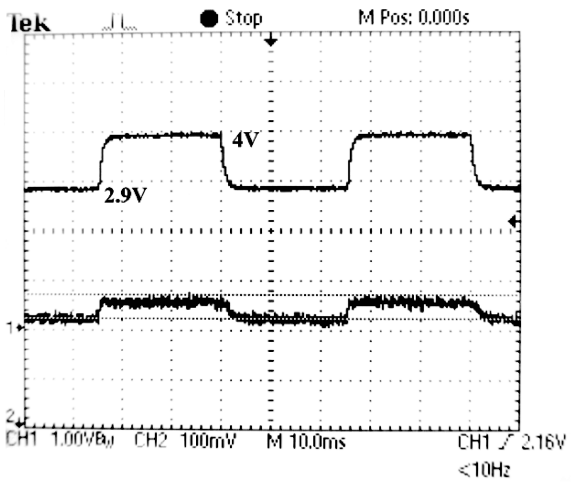

Fig. 12. Measured line regulation of the power solution.

effective. Table 3 summarizes the power comparison of published GNSS dual-channel receivers. Figure 11(b) shows the efficiency with different working frequencies. When the working frequency reaches 16 MHz, we can still get an efficiency of 83%. As a result smaller off-chip devices can be used.

Figure 12 shows the line regulation of the power solution with a variation of the supply voltage from 2.9 to 4 V. It is noted that the output voltage drop is about 4 mV. Eventually, the experiment results show the dual-channel GNSS receiver has a same noise figure of 2.5 dB with or without the DC–DC converter which means the power solution is harmless to the performance of the sensitive RF receivers.

4. Conclusion

This paper presents a high efficiency low EMI power solution for multi-channel GNSS RF receivers. The power solution is composed of a PWM DC–DC converter and a LDO. A PWM control method is chosen for the DC–DC for a better EMI performance. An improved high frequency control circuit is proposed to replace the conventional error amplifier and comparator. By periodically shutting down the OTA, the average quiescent current is halved. In order to achieve high efficiency under light load conditions, the size of the output stage has been optimized. The DC–DC converter has a peak efficiency of 93.1% under a 2 MHz working frequency and the dual-channel GNSS RF receiver consumes only 20.2 mA from a 3.3 V power supply. In addition, a current limiter based soft-start circuit has been implemented in this work. A high PSRR LDO is adopted in this work to prevent the noise of the DC–DC output voltage from sensitive RF modules. By adopting the designed power solution, the receiver achieves a noise figure of only 2.5 dB.

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