A CMOS frequency generation module for 60-GHz applications*

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Abstract: A frequency generation module for 60-GHz transceivers and phased array systems is presented in this paper. It is composed of a divide-by-2 current mode logic divider (CML) and a doubler in push-push configuration. Benefiting from the CML structure and push–push configuration, the proposed frequency generation module has a wide operating frequency range to cover process, voltage, and temperature variation. It is implemented in a 90-nm CMOS process, and occupies a chip area of 0.64×0.65 mm^2 including pads. The measurement results show that the designed frequency generation module functions properly with input frequency over 15 GHz to 25 GHz. The whole chip dissipates 12.1 mW from a 1.2-V supply excluding the output buffers.

Key words: frequency generation; divider; doubler; CMOS

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1. Introduction

Recently, 60-GHz wireless systems with a high transmission data rate of multi gigabits per second has attracted the attention of both academic and industrial researchers[1−5]. However, systems of this kind suffer from huge power consumption, especially in the local frequency generation parts of the systems.

A voltage controlled oscillator (VCO) working at high frequency dissipates a lot of power and always has a narrow tuning range[6−8]. Moreover, the dividers for frequency down-conversion in phase-locked loops also have a high power consumption. Therefore, a frequency plan using a low frequency VCO, followed by dividers and multipliers, is more suitable for 60-GHz transceivers and phased array systems.

Current mode logic (CML) frequency dividers are widely used in the frequency generators[9−11], as they achieve a larger division bandwidth than injection-locking frequency dividers[12, 13]. Moreover, power consumption can be optimized and dramatically reduced by using the injection-locked model proposed in Ref. [11].

Most of the doublers used in frequency generators are single-ended[14−19]. Although doublers with Gilbert cells can realize differential outputs, the power consumption is huge in the mm-wave frequency bands due to the large capacitance incurred at the common sources of the switching pairs[20]. Recently, another kind of differential doubler, evolved from the injection-locked concept, was proposed by Monaco[21−23]. Benefiting from the use of an inductor-tuning tank, the circuit only draws a small current from the supply even above 100-GHz, however the operation frequency range is inevitably narrow due to the limited injection efficiency, which unsatisfactory for many applications.

This paper presents a millimeter-wave frequency generation module composed of a CML divider and a doubler with differential outputs. It is implemented in a 90-nm CMOS process and has realized a working frequency range over 15 GHz to 25 GHz.

2. Circuit design

The frequency generation module is shown in Fig. 1, which is composed of a divide-by-2 divider and a differential doubler. The circuit design will be depicted in the following sections.

2.1. CML divider

Figure 2(a) shows the schematic of CML divide-by-2 divider. It is based on edge-triggered flip-flops in a negative feedback form, which is composed of master and slave CML latches, driven by anti-phase input clocks. M_L, and M_D are the latching pair and the driven pair, respectively. M_B is the tail transistor for constant current bias. Both CML latches are loaded with resistances for a wide-band operating scheme.

The two latches, part I and part Q, are identical, only part I is analyzed here. Obviously, the latching and driven pairs be-

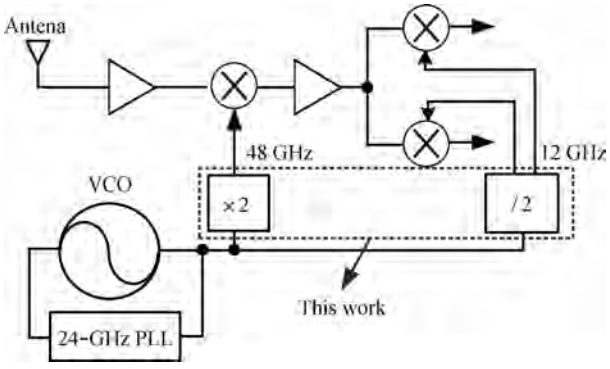

Fig. 1. Block diagram of frequency generation for a 60-GHz system.

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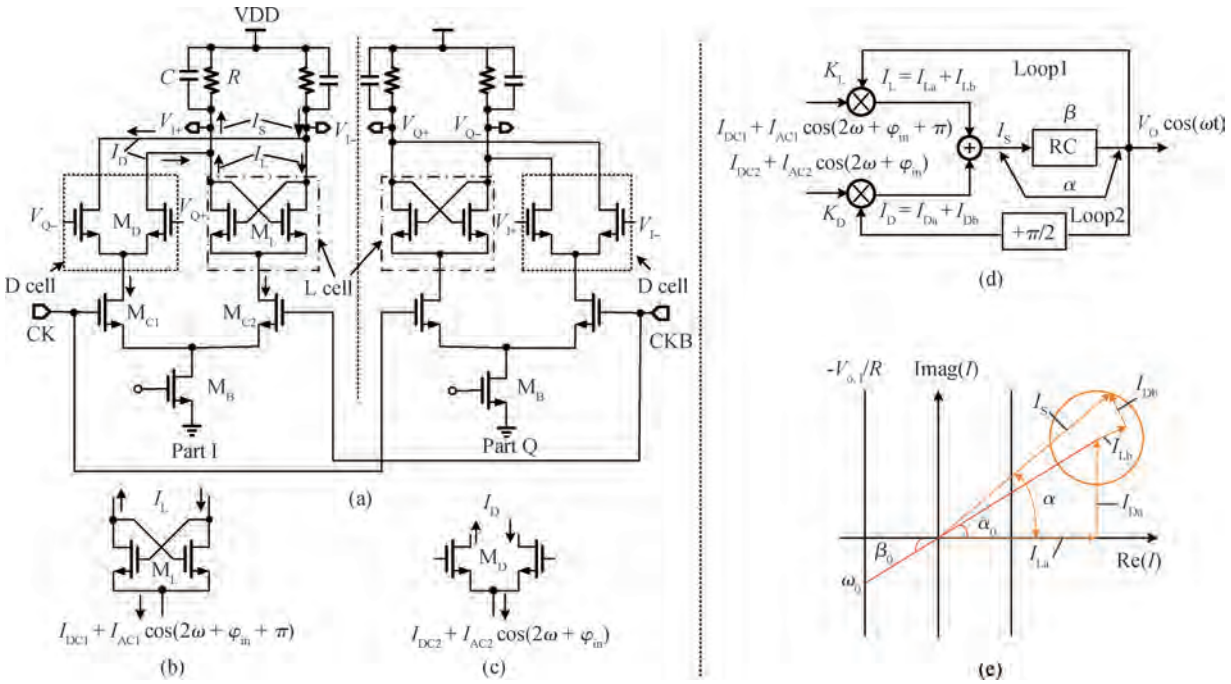

Fig. 2. (a) CML divider. (b) D-cell mixer. (c) L-cell mixer. (d) behavior model. (e) phasor diagram.

haves as mixers. An L-cell mixer mixes the output voltage with the combination of I_{DC1} and $I_{AC1}\cos(2\omega t + \varphi_{in} + \pi)$, while the D-cell mixer mixes the feedback signals with both DC current I_{DC2} and AC current $I_{AC2}\cos(2\omega t + \varphi_{in})$ at a frequency of 2ω, as shown in Figs. 2(b) and 2(c). Therefore, the divider performs as two-loop systems, as shown in Fig. 2(d). Based on the Barkhausen criterion, the divider needs to satisfy two necessary conditions: (1) the loop phase at operation frequency ω is equal to 0; (2) loop gain at the same frequency is larger than one. Since a negative phase β is introduced by the RC load, the mixers should generate a positive phase to compensate it. Therefore, the Q output must lag its Q counterpart by $\pi/2$.

According to the behavioral model of the CML divider, the total current at frequency ω is calculated as

$$\begin{cases} I_S(\omega) = I_L + I_D = I_{La} + I_{Da} + I_{Lb} + I_{Db}, \\ I_{Da} = K_D I_{DC2}\cos(\omega t + \pi/2), \\ I_{La} = K_L I_{DC1}\cos(\omega t), \\ I_{Db} = K_D I_{AC2}\cos(\omega t + \varphi_{in} - \pi/2), \\ I_{Lb} = K_L I_{AC1}\cos(\omega t + \varphi_{in} + \pi). \end{cases} \quad (1)$$

Here K_L and K_D denote the current conversion gain of the L-cell and D-cell mixers. The phasor diagram of the output current is shown in Fig. 2(e). According to the Barkhausen criterion and the phasor diagram, it is easily to find that a small current I_{DC1} enables a large positive phase to compensate the negative phase introduced by the RC load, which helps to improve the division frequency band of the CML divider. Optimized with the two-loop behavior model, the CML divider achieves an operating frequency range from 17-GHz to 27-GHz at an incident input signal power of 0-dBm based on the simulations, as shown in Fig. 3.

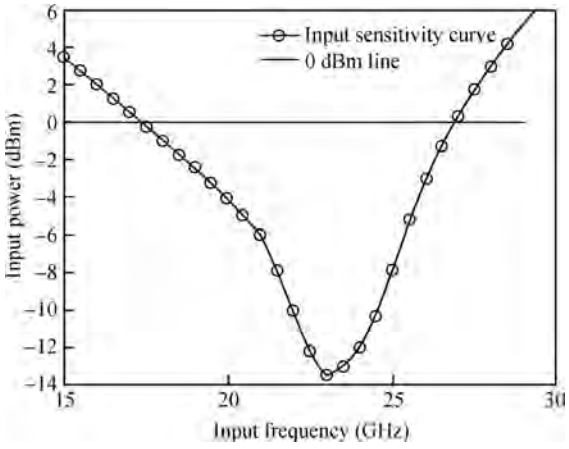

Fig. 3. Simulated input sensitivity curve.

2.2. Doubler in push-push configuration

The schematic of the doubler is shown in Fig. 4. M_3 and M_4 are the input push-push pair. M_1 and M_2 are the cascoded transistors. M_5 and M_6 consist of the output buffer. L_1 is the inductor used to choose the second harmonic of the input signals, and T_1 is the output balun for differential output generation.

The operating frequency range is wide because the second harmonic input is generated by the nonlinearity of the push-push pair. Moreover, benefiting from the differential input and the output tuning tank, the fundamental suppression of the doubler is larger than 43 dB from 21 GHz to 27 GHz of input frequency, as shown in Fig. 5. In order to acquire a large conversion gain, a strong input is needed and the push-push pair should be biased in the class AB condition. Figure 6 shows the simulated conversion gain of the doubler with 0-dBm input power.

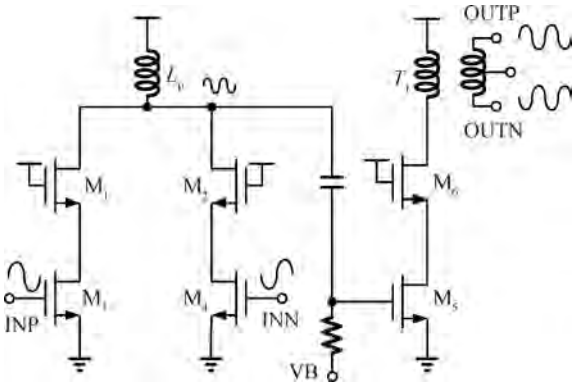

Fig. 4. Schematic of the doubler.

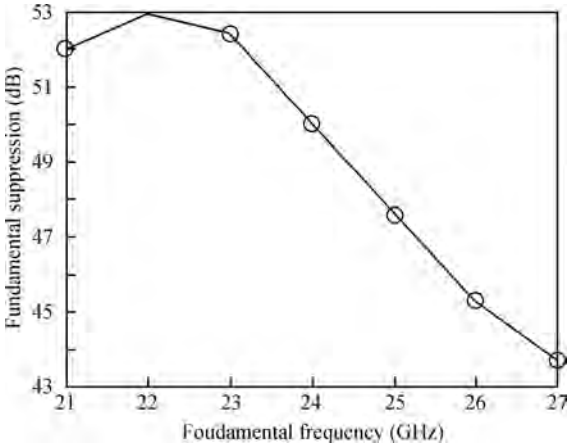

Fig. 5. Simulated fundamental suppression of the doubler.

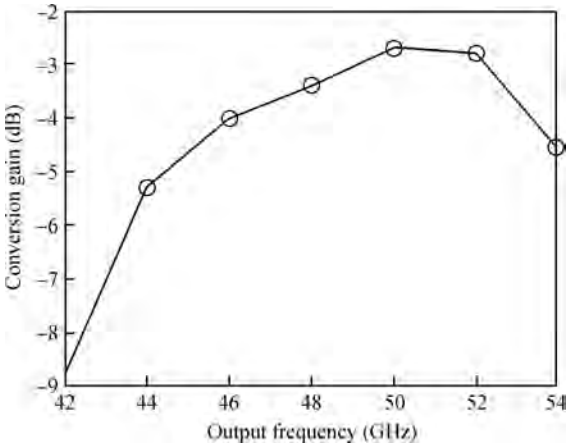

Fig. 6. Simulated conversion gain of the doubler.

A stacked balun is introduced to obtain a differential outputs for phased array systems, which is simulated and optimized in a high frequency structure simulator (HFSS). The optimized balun with a width of 5 μm and a inner radius of 25 μm has an insertion loss of -3.5 dB at 48 GHz when used in the doubler.

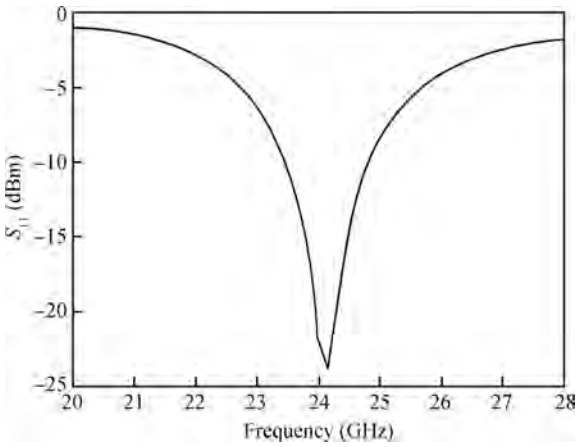

Fig. 7. Simulated input return loss of the frequency generation module.

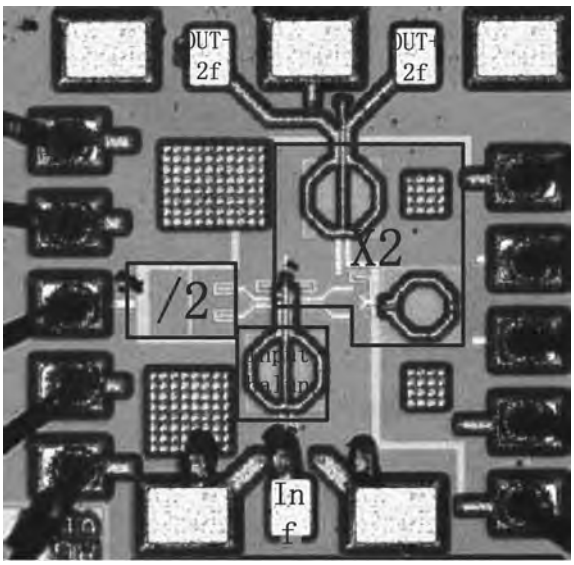

Fig. 8. Chip micrograph of frequency generation.

2.3. Design of the Input Balun

The differential input of the CML divider and the doubler is provided by a stacked balun with the top two thick metals in a 90-nm CMOS process. The dimensions of the input balun is optimized using the HFSS. The trace width and inner radius of the input balun in the design are 5 μm and 30 μm, respectively. The simulated input return loss is shown in Fig. 7.

3. Measurement results

The proposed frequency generation module consisting of a CML divide-by-2 divider and a doubler of push-push configuration is designed and implemented in a 90-nm CMOS process. The die micrograph is shown in Fig. 8. The core chip size is 0.4×0.44 mm^2 excluding pads.

The DC supplies and outputs of the divider are wire-bonded to a printed circuit board (PCB), while the input of the frequency generation module and the outputs of doubler are probed. The measured power spectrum density of the divider and doubler outputs with a 24-GHz input frequency are shown in Figs. 9, and 10, respectively. The input achieves good

Table 1. Performance comparison with state-of-the-art frequency generation modules.

Parameter	Technology	Input frequency (GHz)	Power consumption: Divider/Doubler (mW/mW)	FOM_{Pdc}: Divider/Doubler (dB/dB)
Ref. [9]	0.13-μm CMOS	12–18	12/–	15/–
Ref. [10]	90-nm CMOS	2–35.5	28.8/–	17.9/–
Ref. [11]	0.18-μm CMOS	7.5–20	4.3/–	23.3/–
Ref. [20]	0.18-μm SiGe BiCMOS	18–40	–/137.28	–/7.42
Ref. [23]	65-nm CMOS	53–64	–/6	–/14.96
This work	90-nm CMOS	15–25	4.7/7.4	20.3/18.3

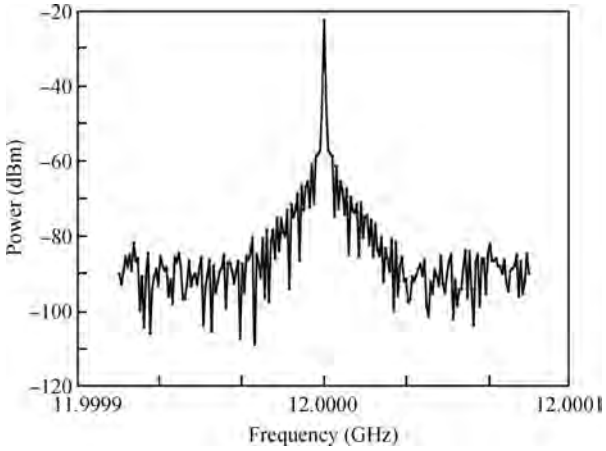

Fig. 9. Measured power spectrum of the divider output with 24 GHz input.

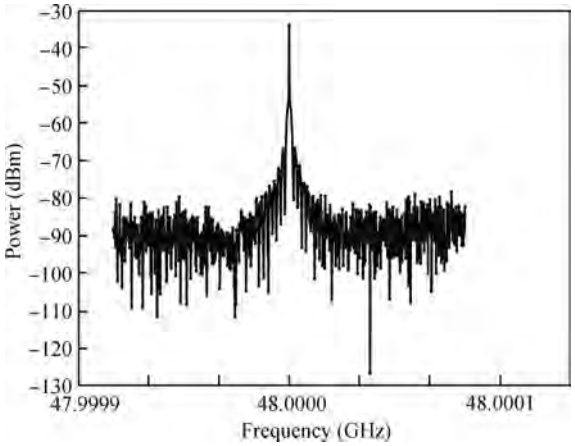

Fig. 10. Measured power spectrum of the doubler output with 24 GHz input.

matching, as shown in Fig. 11.

In order to compare the overall performance of the dividers and doublers, a widely used figure of merit (FOM_{Pdc}) is applied, which is defined as

$$\mathrm{FOM_{Pdc}} = 10\lg\left(\frac{f_{\mathrm{lock}}}{f_{\mathrm{center}}}\frac{1\,\mathrm{W}}{P_{\mathrm{dc}}}\right), \tag{2}$$

where f_{lock} is the input locking range, f_{center} is the center input working frequency, and P_{dc} is the DC power consumption. Table 1 shows comparisons with reported dividers and doublers. Obviously, this proposed CML divider and doubler implemented in 90-nm CMOS technology achieve a good FOM_{Pdc}.

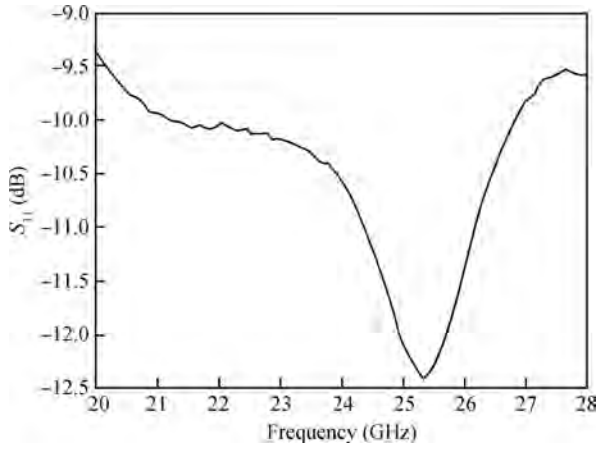

Fig. 11. Measured input return loss of the frequency generation module.

4. Conclusion

A 24-GHz frequency generation module consisting of a divider and a doubler for 60-GHz phased array transceiver application is presented in this paper and implemented in a 90-nm CMOS process. The measurement results show that the designed frequency generation system achieves a working frequency range from 15 GHz to 25 GHz with 0-dBm input power. The whole chip dissipates only 12.1 mA from 1.2-V supply excluding output driven buffers and occupies a chip area of 0.64×0.65 mm^2 including pads.

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