A strained Si-channel NMOSFET with low field mobility enhancement of about 140% using a SiGe virtual substrate*

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Abstract: A fully standard CMOS integrated strained Si-channel NMOSFET has been demonstrated. By adjusting the thickness of graded SiGe, modifying the channel doping concentration, changing the Ge fraction of the relaxed SiGe layer and forming a p-well by multiple implantation technology, a surface strained Si-channel NMOSFET was fabricated, of which the low field mobility was enhanced by 140%, compared with the bulk-Si control device. Strained NMOSFET and PMOSFET were used to fabricate a strained CMOS inverter based on a SiGe virtual substrate. Test results indicated that the strained CMOS converter had a drain leakage current much lower than the Si devices, and the device exhibited wonderful on/off-state voltage transmission characteristics.

Key words: CMOS inverter; strained Si; mobility enhancement; SiGe virtual substrate; relaxed layer
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1. Introduction

During the past few years, carrier mobility enhancement technology has been intensively investigated for its diverse applications[1,2]. Strained Si technology, including both material and process innovation considerations, is the usual method to increase the mobility of electrons and holes. The strained NMOSFET device has great potential in the application for high-speed CMOS ICs, thanks to its mobility enhancement. A $Si_{1-x}Ge_x$ virtual substrate is used as a useful and key technology to obtain a high performance strained NMOSFET[2]. The conventional technical scheme is to grow a strained Si layer on a relaxed $Si_{1-x}Ge_x$ buffer layer with a smooth surface and a low threading dislocation density, which has been well investigated[2–8].

In this paper, the samples were fabricated on a nominal n-type substrate. Prior to growth of a 20 nm thick strained Si cap layer, an approximately 2 μm thick Si buffer , a 1 μm linearly graded $Si_{1-x}Ge_x$ (with a nominal final Ge mole fraction of 0.25) layer and an approximately 0.5 μm thick $Si_{0.75}Ge_{0.25}$ relaxed layer were deposited layer by layer.

During the CMOS process, NMOSFET should be fabricated in a p-well. So, the p-well process is the key issue. In general, a high temperature drive-in following ion implantation was used to form the p-well. It should be noted that the thermal budget must be well controlled, considering the strain characteristics of the channel. Therefore, a low temperature drive-in after implantation with four-time varied energy becomes the best method to form a p-well. Figure 1 shows a cross section of a CMOS inverter. NMOSFET and PMOSFET devices using a 20 nm strained Si layer on a relaxed $Si_{0.75}Ge_{0.25}$ layer are fabricated and measured.

2. Structure and process design

2.1. Structure design

The epitaxial layer structure of the strained Si on the virtual SiGe substrate is shown schematically in Fig. 2. The strained $Si/Si_{0.75}Ge_{0.25}$ channel layers are grown on a relaxed linearly graded $Si_{1-x}Ge_x$. The smaller lattice constant of Si dictates that the subsequent Si layer is in tension, allowing the electron mobility enhancement suitable for the n-channel of strained Si NMOSFET.

The proposed concentrations and structural parameters are as follows:

Concentration of the substrate: 4×10^{15} cm^{-3}.
Concentration of the buffer layer: $\sim 1 \times 10^{17}$ cm^{-3}.
Concentration of the relaxed SiGe layer: $\sim 1 \times 10^{17}$ cm^{-3}.
Depth of the p-well: about 0.58 μm.
Depth of the source/drain: about 0.13 μm.

2.2. Process design

The main process steps to fabricate a strained NMOSFET and PMOSFET based on a $Si_{0.75}Ge_{0.25}$ virtual substrate are described as follows. The gate oxide is thermally grown by low temperature wet oxidation. The gate polysilicon is implanted with source and drain implantation.

N(100) wafer → buffer Si layer deposition → relaxed $Si_{0.75}Ge_{0.25}$ layer growth → strained Si layer deposition →

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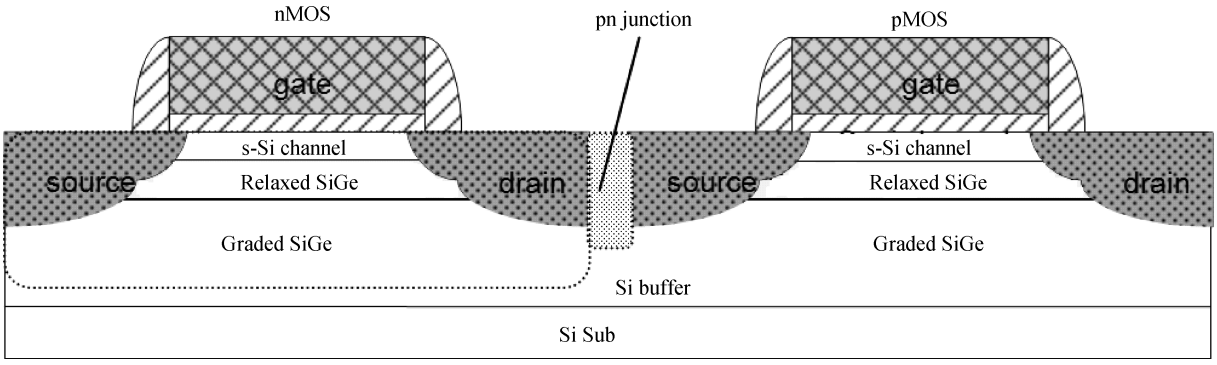

Fig. 1. Cross-section of the strained CMOS structure based on relaxed SiGe virtual substrate.

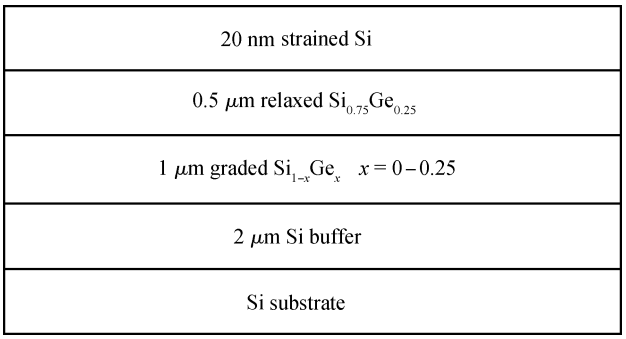

Fig. 2. Structure of the SiGe virtual substrate.

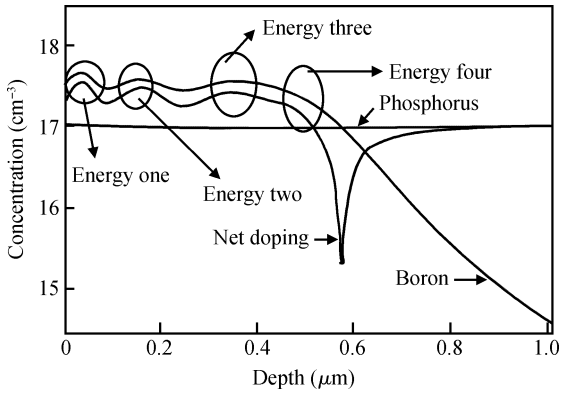

Fig. 3. Simulated distribution curves of the net doping and boron doping (boron is implanted with varied energy).

LPCVD deposition of dielectrics → N^+ ring lithography/etch → N^+ ring implantation → P^+ ring lithography/etch → P^+ ring implantation → active lithography/etch → gate oxide → p-well lithography → p-well implantation → LPCVD deposition of poly-silicon → poly-silicon oxide → poly-silicon lithography/etch → LPCVD deposition of SiO_2 → spacer etch → NMOSFET source/drain lithography → arsenic implantation → PMOSFET source/drain lithography → BF_2 implantation → LPCVD deposition of SiO_2 → contact lithography/etch → metallization → testing → alloying → parameter testing.

In the complete process, the p-well is one of the main issues. Four-time varied energy boron implantation is adopted to form the p-well. As shown in Fig. 3, there are four peaks on the simulated curves.

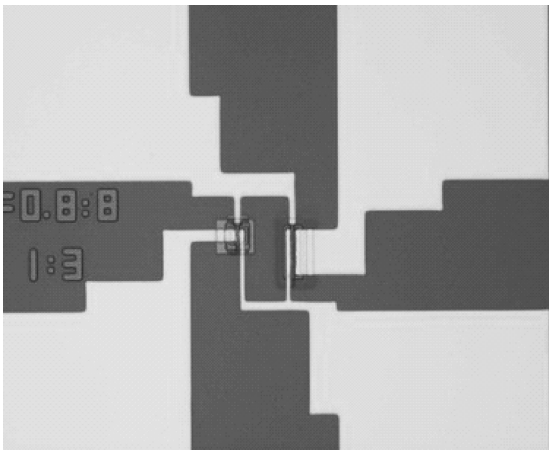

Fig. 4. Photograph of the strained CMOS inverter based on a $Si_{1-x}Ge_x$ virtual substrate.

3. Results and discussion

3.1. Results

Using the above-mentioned process flow, a stained CMOS inverter based on a $Si_{1-x}Ge_x$ virtual substrate is fabricated. Figure 4 shows the photograph of the strained CMOS inverter. Finally, characteristics of the separate MOSFET and the inverter are measured at five locations on the wafer. Figure 5 shows I_D–V_G transfer characteristics of the strained NMOSFET and bulk-Si control device at $V_{ds} = 0.5$ V. Output characteristics of the strained NMOSFET and bulk Si as the gate voltage V_{gs} changes from 1 to 10 V at 1 V intervals are compared in Fig. 6. In the experiment, two normal Si wafers and one strained wafer are measured, and the field-effect mobility ratio of the s-Si NMOSFET and the bulk-Si NMOSFET versus the effective field measured at $V_d = 0.5$ V can be seen in Fig. 7. The carrier mobility is calculated from these curves (Section 3.2). Figure 8 shows the characteristics of the fabricated inverter.

3.2. Discussion

At the low field of $V_{ds} = 0.5$ V and $V_{gs} = 3.5$ V, current density and maximal mobility of the proposed strained NMOSFET are improved by 140%, which is 2.4 times that of the bulk-Si control device. The characteristics of the strained PMOS-

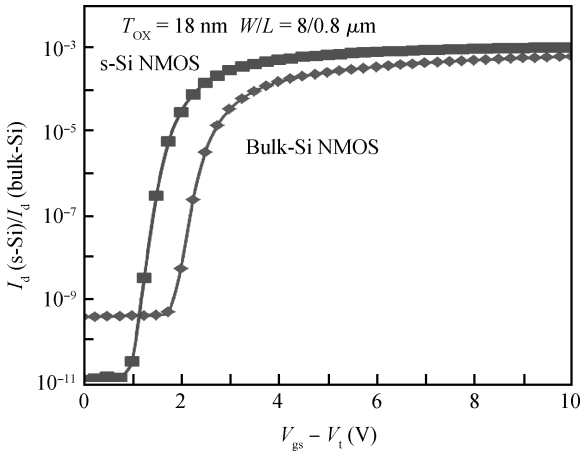

Fig. 5. Typical I_d versus V_{gs}–V_t characteristics for a 0.8 × 8 μm^2 strained Si device and bulk-Si at $V_{ds} = 0.5$ V.

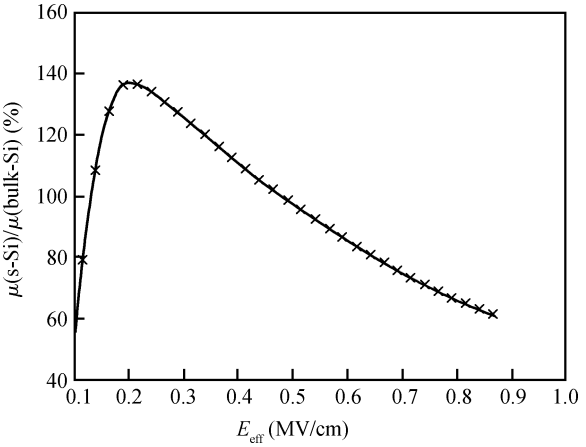

Fig. 7. Field-effect mobility ratio of the s-Si NMOSFET and the bulk-Si NMOSFET versus the effective field E_{eff} measured at $V_d = 0.5$ V.

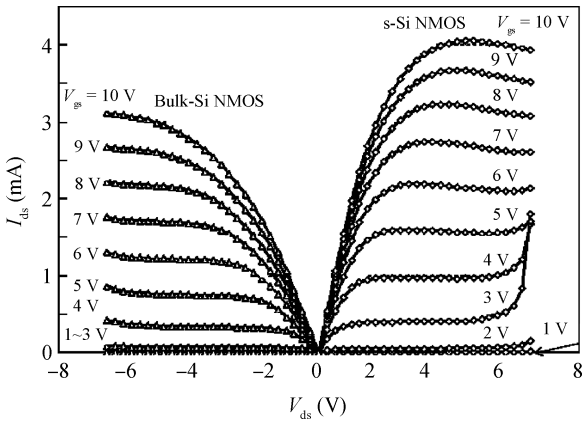

Fig. 6. Output characteristics of the strained NMOSFET and bulk Si NMOSFET at $V_{gs} = 1$–10 V.

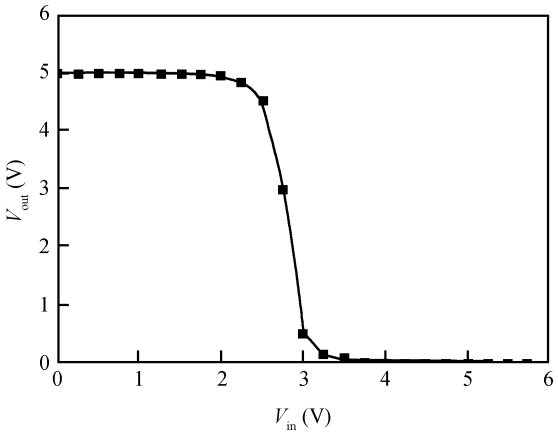

Fig. 8. Characteristics of the proposed inverter.

FET are almost the same as the bulk-Si PMOSFET.

In designing the layout of the proposed NMOSFET, channel length is 0.8 μm, channel width is 8 μm, and the depth of source and drain is 0.13 μm. Taking the source/drain resistance and the contact resistance into consideration, the following equation can be used:

$$I_{DS} = \frac{W}{L}\mu C_{ox}[V_{GS} - V_T - I_{DS}(R_s + R_c)] \times [V_{DS} - I_{DS}(R_S + R_D + 2R_c)], \quad (1)$$

where C_{ox} is the capacitance of poly-silicon gate to the epitaxial layer, μ is the mobility of the electron or hole, W is the channel width, L is the channel length, V_t is the threshold voltage of the gate–source, R_S is the source series resistance, R_D is the drain series resistance, R_C is the contact resistance, and V_{GS}–V_t is the effective gate voltage.

Although gate voltages of the strained NMOSFET and Si NMOSFET are not equal, their effective gate voltages are the same. This is accurate from a physical sense. For the convenience of the calculation, the value of C_{ox1} is the same as C_{ox2}. The mobility of the proposed strained NMOSFET is enhanced by about 140% at a gate–source voltage of 3.5 V, as can be seen from Fig. 7.

From Fig. 5 to Fig. 7, it can be seen that the drain–source current (I_{ds}) of the strained NMOSFET is higher than that of the bulk-Si control device at $V_{ds} = 0.5$ V, and the I_{ds} value of the strained NMOSFET is 2.9 times the value of the bulk-Si control device, which is higher than the enhancement of 170% reported in Ref. [1]. Furthermore, the mobility of the strained NMOSFET is enhanced by about 140% at $V_{gs} = 3.5$ V and $V_{ds} = 0.5$ V. As shown in Fig. 8, characteristics of the strained CMOS inverter are perfect. Its drain leakage current is very low. Moreover, the high/low output voltage of the device is almost rail to rail.

4. Conclusion

A high performance strained NMOSFET and a strained CMOS inverter based on a SiGe virtual substrate were presented. Test results showed that the drain-source current of the strained silicon NMOSFET is enhanced by 190% and the mobility is enhanced by a maximum of 140% at $V_{gs} = 3.5$ V and $V_{ds} = 0.5$ V, compared with the bulk Si NMOSFET using a similar process. The strained CMOS converter based on the SiGe virtual substrate has perfect on/off-state voltage transmission characteristics, such as a low drain leakage current. The

proposed device structure and process is applicable for high-performance CMOS analog IC's.

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