A 400-MS/s 12-bit current-steering D/A converter

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Abstract: This paper presents a 400-MS/s 12-bit CMOS current-steering digital-to-analog converter (DAC). The proposed DAC adapts 6+2+4 segmented architecture and a modified switching scheme to improve dynamic and static performance. The measured spurious-free dynamic range is up to 77.18 dB at 400 MS/s with a 10 MHz input signal. The full-scale output current is 20 mA with a 1.8 V single power supply. The core area occupies 0.6 mm^2 in a standard 1P-6M 0.18-μm CMOS process.

Key words: current-steering; digital-to-analog converter; spurious-free dynamic range; high-speed
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1. Introduction

The recent research trends of SOC systems and wireless communication systems have led to a high demand for front-end and back-end mixed-signal circuits. High-speed, high-accuracy digital-to-analog converters (DACs), typically with 12-bit or higher resolution and sampling rates of up to hundreds of MHz, are the key building blocks that usually dominate the performance of these systems. CMOS current-steering DACs are ideal candidates for use in these applications. Since no internal nodes with large capacitances need to be charged or discharged, they are inherently fast and can offer a large spurious-free dynamic range (SFDR) up to high frequencies[1]. Furthermore, they can drive an output resistive load directly without requiring the extra use of buffers.

Current steering DACs are based on an array of matched current sources, which are steered to the output depending on the decoded digital codes. According to the organization of the current sources with different weights, DACs are divided into three classes, namely binary, unary and segmented architecture[2]. Binary architecture has advantages in its simplicity and small silicon area, but a large glitch and a large DNL error are intrinsically linked with this architecture. However, unary architecture has a low glitch and guarantees good monotonicity. Its major disadvantage is its complex thermometer decoder, which not only occupies a large silicon area, but also consumes a lot of power. In order to obtain a tradeoff between the two types, most current steering DACs are implemented in a segmented architecture. In this architecture, unary current sources are used for the most significant bits while the least significant bits are composed by small binary current sources. Thus a balance between small glitch energy, DNL error on one side and a reasonable area, decoder power and complexity on the other side can be made.

In the next section, an overview of the DAC architecture is described first. Then the main design issues including current mismatches, decoding logic implementation and the current switch control signals are discussed. The measurement results and then conclusions are presented.

2. DAC design

Current sources are the fundamental cells of current-steering DACs. Both PMOS and NMOS transistors are potential candidates. PMOS transistors are implemented in an N-well so that they have better matching properties, while NMOS transistors have the advantage of a large bandwidth. As a high working frequency is one of the main aims of our design, NMOS transistors are selected while improved layout techniques are used to compensate the matching errors.

To achieve good performance, it is very important to choose an appropriate segmentation[2]. The number of binary-weighted bits has to be kept small in order to avoid large glitch energy and DNL errors. Meanwhile, every extra bit in MSBs will considerably increase the routing complexity and digital logic delay, thus degrading DAC performance at high frequency. The proposed 12-bit DAC employs three-segmented architecture. Four least significant bits (LSB) are implemented in a binary configuration and six most significant bits (MSB) in a unary configuration. The remaining two intermediately significant bits (ISB) are also unary-weighted, while the unit current is a quarter that of the MSBs. The DAC's structure can be functionally divided into two sub-circuit entities, the digital part and the analog part. Figure 1 shows the block diagram of the realized DAC.

The analog part includes current cells and switches. It provides well-matched reference currents and switches them to the output. Static errors and linearity behavior are mainly determined by this part.

The digital part consists of the decoding logic and the latch. The decoders process the applied code and generate the control signals for the switches. High-speed latches are inserted between the current cell and the decoding logic to support timing synchronization. The digital part is also designed manually at transistor level.

In the next sections, a closed design plan of these two sub parts are discussed in detail.

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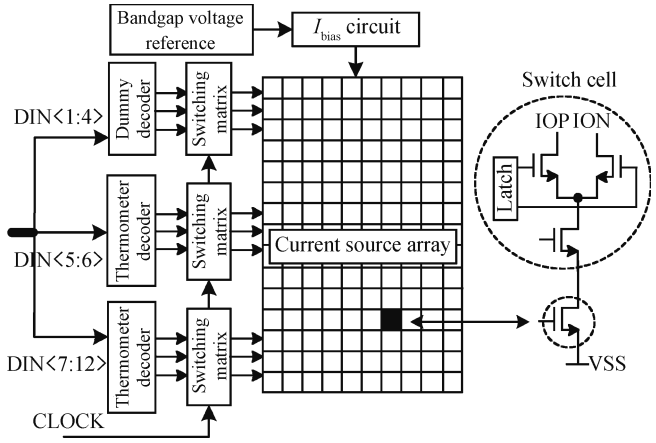


Fig. 1. Block diagram of the realized DAC.

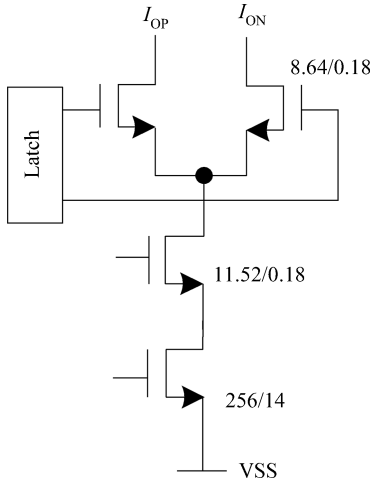


Fig. 2. Dimensions of the proposed current cell.

2.1. Analog part

Static nonlinearity mainly comes from three sources: (1) finite and code-dependent output impedance; (2) random errors caused by current cell mismatch; and (3) systematic and graded errors due to layout and process problems.

To achieve good statistic performance, all the problems mentioned above have to be tackled carefully.

2.1.1. Finite impedance

The finite output impedance is one of the major sources of static nonlinearity because the total impedance at the output node varies with the number of the current sources switched to the output. The relation between integral nonlinearity (INL) and output impedance is expressed by

$$\mathrm{INL} = \frac{I_{\mathrm{LSB}} R_{\mathrm{L}}^2 2^{2N}}{4Z_{\mathrm{imp}}}, \tag{1}$$

with R_{L} the load resistor, I_{LSB} the LSB current, Z_{imp} the impedance seen from the drain of the switch transistors, and N the resolution of the DAC. To reduce the influence on INL, a large Z_{imp} is desired. As shown in the right-hand side of Fig. 1, a cascode transistor is placed on top of the current source to enable sufficiently high impedance.

On the other hand, output impedance will degrade at a high operating frequency due to the parasitic capacitive load. Therefore, the cascode and switch transistors should be as small as possible. The cascode transistor is also useful in lowering glitch errors caused by drain voltage variation of the current source.

2.1.2. Random errors

For a current-steering DAC, the random variation of current sources is another dominant source of DNL and INL[2]. The adequate area of the current source transistors can be determined by using a statistical model related to the mismatch properties[3]. The minimum area is given by

$$WL = \frac{1}{2[\sigma(I)/I]^2}\left[A_\beta^2 + \frac{4A_{\mathrm{VT}}^2}{(V_{\mathrm{GS}} - V_{\mathrm{T}})^2}\right], \tag{2}$$

where $\sigma(I)/I$ is the relative standard deviation of an LSB current source; A_β and A_{VT} are process mismatch parameters. The other parameters W, L, V_{GS} and V_{T} are the width, length, gate-to-source voltage, and threshold voltage of the current source transistor, respectively. The gate overdrive voltage ($V_{\mathrm{GS}} - V_{\mathrm{T}}$) is limited by the fact that both the cascode and the switch transistors have to operate in the saturation region.

The INL specification leads to the first constraint for the dimensions, W and L, of the current source. The full-scale current leads to another.

$$I_{\mathrm{full}} = 2^N \frac{\mu_{\mathrm{p}} C_{\mathrm{ox}}}{2} \frac{W}{L} (V_{\mathrm{GS}} - V_{\mathrm{T}})^2 . \tag{3}$$

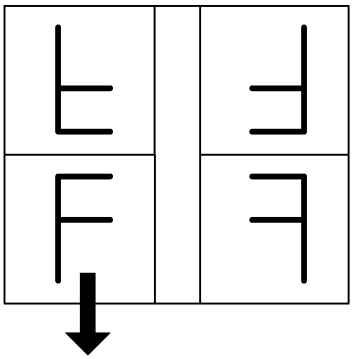
The dimensions of the current cell transistors are obtained from Eqs. (1)–(3). The MSB cell is shown in Fig. 2. These dimensions are designed for a 20 mA full-scale output current.

2.1.3. Systematic and graded errors

For a DAC with a resolution of 12-bits or even higher, the dimensions of the current source array become so large that process, temperature, and electrical gradients have to be taken into consideration. The nonlinearity errors introduced by these systematic gradients can be partially compensated by employing a carefully designed layout. Until now, the most linearity efficient switching scheme reported was the Q^2 random walk switching scheme[4]. It is suggested that the current source transistors should not only be arranged in a specific sequence in a matrix, but also each of them split into several units in different locations to average the systematic error spatially.

A switching sequence designed to reduce linear errors was introduced by Huang[5]. We apply the Q^2 random walk method to this scheme to develop an improved switching scheme. Thus not only linear errors but also quadratic errors can be efficiently compensated.

The 6 MSB inputs are converted into 63-bit thermometer code. Each thermometer-coded current source is split into four identical units in parallel and located in the four quadrants of the array respectively. 4 LSB binary-coded current sources and 2 ISB unary-coded current sources occupy the vertical symmetry axis. Then the original switching sequence is utilized to compensate for the residual errors in each quadrant. The switching sequence of the current sources in the third quadrant is shown in detail in Fig. 3, while other quadrants are assigned



M0	60	56	52	51	55	59	63	29	25	21	17	18	22	26	30
48	44	40	36	35	39	43	47	13	9	5	1	2	6	10	14
16	12	8	4	3	7	11	15	45	41	37	33	34	38	42	46
32	28	24	20	19	23	27	31	61	57	53	49	50	54	58	62

Fig. 3. Improved switching scheme.

using different symmetrical methods, indicated by the direction of "F".

The simulation results of the original and improved schemes are shown in Fig. 4. We have assumed that the gradients of both linear and quadratic errors are 0.1% per unit length, which is the distance between two horizontally adjacent current sources. The improved switching scheme can totally cancel the linear errors and reduce the quadratic errors to half that of the original scheme.

2.2. Digital part

The digital part's task is to decode the input code into appropriate switching signals and to keep them synchronous.

The 6-64 thermometer decoder is combined by two 3-8 decoders. The 6 MSBs are further divided into two groups, each containing 3 bits. First, two conventional 3-8 decoders convert each 3 bits into row and column signals, respectively. Then the controlling signals and the inverse signal for the unit current cells in the matrix are generated by combining the output of the row and column decoders. The switching signal (COL+1)+(ROW×COL) is equivalent to an AND-OR gate function. To achieve an increased operation speed, the decoder has been manually designed and has been laid out at transistor level.

The dynamic performance of a current-steering DAC may be limited by several factors[2]. Some important issues that have been identified to cause dynamic degradation are:

(1) voltage fluctuation at the common node of the differential switches;

(2) feed-through of switch control signals to the analog outputs; and

(3) imperfect synchronization of switch control signals.

To minimize these negative effects, latches are generally placed in front of the differential switches. Figure 5 shows the schematic of the latch used in this design. Since NMOS current switch transistors are used, the differential output control signals of the latch must have a high crossing point to keep

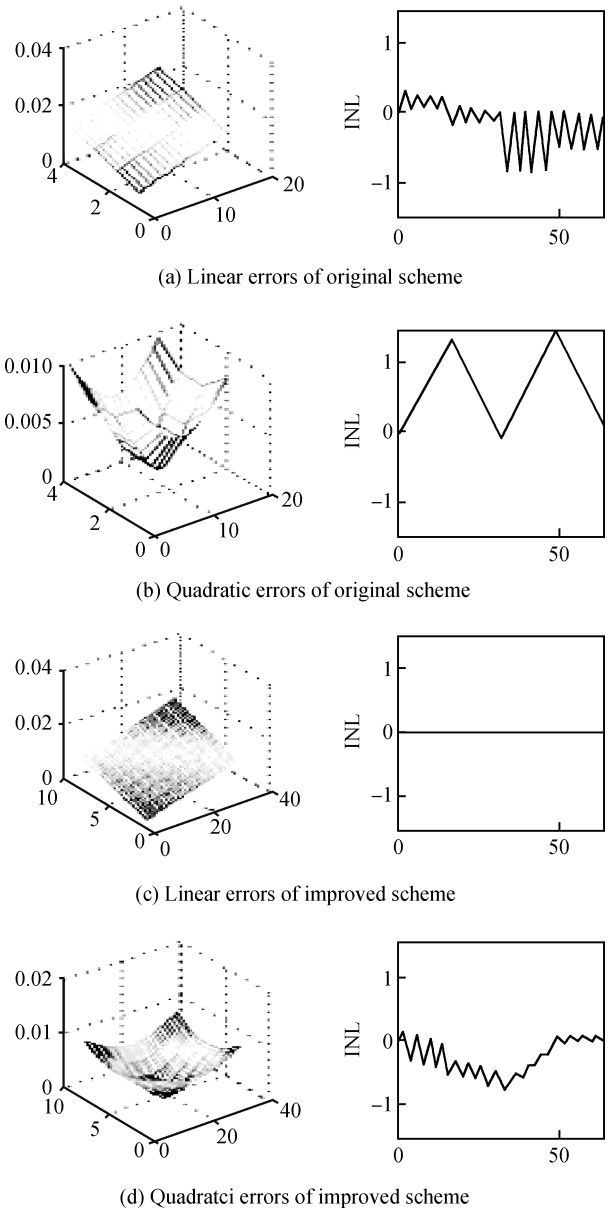


Fig. 4. INL depending on current gradient.

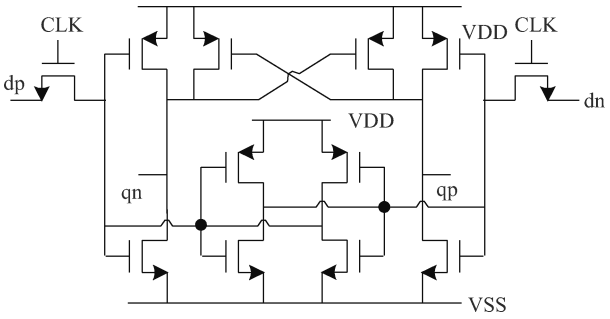


Fig. 5. Latch schematic.

the switches from being simultaneously in the off state, thus reducing voltage fluctuation at the common node. The latches are controlled by the clock signal to ensure synchronization of the switching signals. In this case, the sampling rate of the DAC is limited by the speed of the decoder.

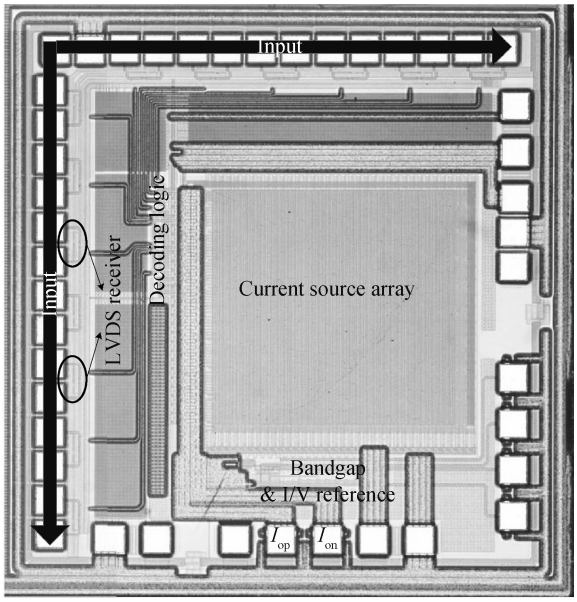


Fig. 6. Photo of the current-steering DAC.

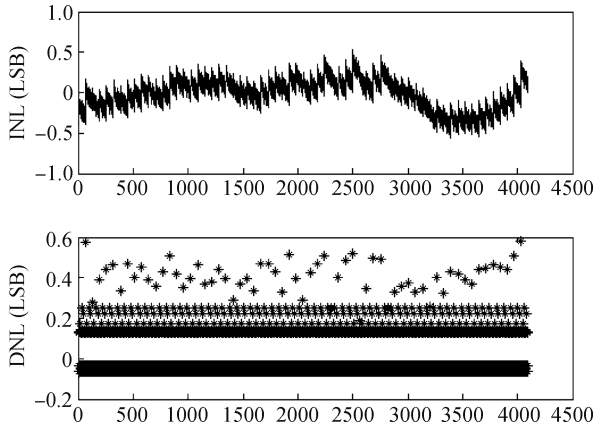


Fig. 7. Measured DNL and INL of the DAC.

3. Measurement results

The chip was fabricated in a 1P-6M 0.18 μm CMOS process with 1.8 V power supply. An LVDS interface is used to achieve a high board-to-chip data rate. The output load resistor is 50 Ω differentially terminated. A photo is shown in Fig. 6, with the active area 0.7 × 0.8 mm^2. The full-scale current is 20 mA, resulting in a 1 V output voltage swing.

The DNL and INL characteristics of the proposed 12-bit DAC with 20 mA output current are shown in Fig. 7. This plot illustrates DNL errors less than 0.58 LSB and INL errors less than 0.56 LSB.

The dynamic test is based on a single-end output of 20 mA. Figure 8 shows the spectrum of the converted signal with a 10 MHz input signal at a 400 MS/s sampling rate. The measured SFDR is 77.18 dB.

Figure 9 shows the SFDR versus input signal frequency at a 400 MS/s sampling rate.

The measured performance of the proposed 12-bit 400MS/s DAC is summarized in Table 1.

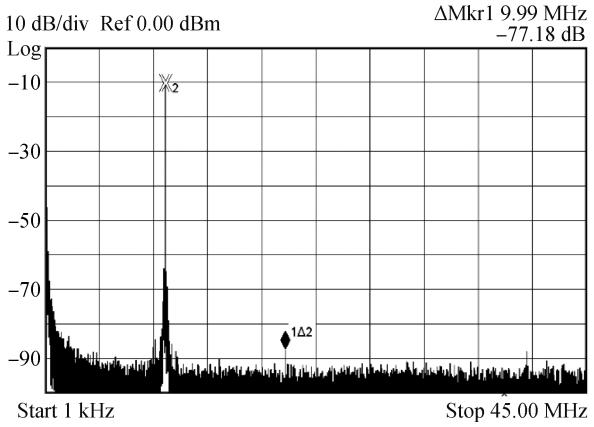


Fig. 8. SFDR @ f_{in} = 10 MHz, f_s = 400 MS/s.

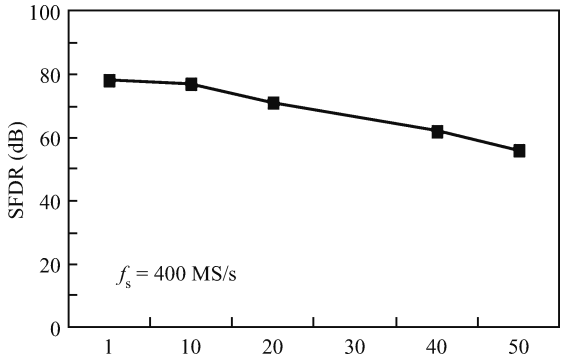


Fig. 9. Measured SFDR at 400 MS/s versus input signal frequency.

Table 1. Measured performance of 12-bit DAC.

Parameter	Value
Resolution	12 bits
Sampling rate	400 MS/s
INL/DNL	±0.56 LSB/±0.58 LSB
SFDR (10 MHz @ 400 MS/s)	77.18 dB
Power supply	1.8 V
Power consumption	65 mW
Full-scale output current	20 mA
Core area	0.7 × 0.8 mm^2
Process	1P-6M 0.18 μm CMOS

4. Conclusion

In this paper, a 12-bit 400 Ms/s DAC is presented. To minimize systematic influence on the current source, an improved switching scheme is developed and evaluated. According to the measurement results, an SFDR of up to 77.18 dB can be achieved from a full-scale output of 20 mA and the update rate is 400 MS/s with a 10 MHz input signal. The active area is 0.6 mm^2 in a 0.18 μm CMOS process.

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