A low-phase-noise ring oscillator with coarse and fine tuning in a standard CMOS process*

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Abstract: A low-phase-noise wideband ring oscillator with coarse and fine tuning techniques implemented in a standard 65 nm CMOS process is presented. Direct frequency modulation in the ring oscillator is analyzed and a switched capacitor array is introduced to produce the lower VCO gain required to suppress this effect. A two-dimensional high-density stacked MOM-capacitor was adopted as the switched capacitor to make the proposed ring VCO compatible with standard CMOS processes. The designed ring VCO exhibits an output frequency from 480 to 1100 MHz, resulting in a tuning range of 78%, and the measured phase noise is –120 dBc/Hz @ 1 MHz at 495 MHz output. The VCO core consumes 3.84 mW under a 1.2 V supply voltage and the corresponding FOM is –169 dBc/Hz.

Key words: ring oscillator; switched capacitor array; phase noise; MOM-capacitor; standard CMOS
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1. Introduction

Phase-locked loops (PLLs) are widely used for clock generation in high-speed digital systems and local oscillation signals in wireless communication systems. The voltage-controlled oscillator (VCO) is a key component of PLLs. The most essential requirements for VCOs are low phase noise and a wide tuning range. Other important considerations are low implementation costs and ease of integration. There are two basic types of VCO structure: the ring VCO and the LC-VCO. The ring VCO exhibits a wide tuning range, ease of integration and low cost, but poor phase noise due to a low Q and a large VCO-gain ($K_{\rm vco}$)[1].

To improve the phase noise of the ring VCO, a dual-loop ring-VCO structure was proposed by Park[2]. This circuit technique provides fast rail-to-rail switching, thus improving the Q of the ring VCO and lowering phase noise. Another ring-VCO with a digitally switchable FET load was proposed by Gerosa[3] to lower the $K_{\rm vco}$ and keep the tuning range unaffected. A lower $K_{\rm vco}$ means less sensitivity to noise at tuning node and the phase noise was improved

In this paper, a dual-loop wideband ring VCO with coarse and fine tuning techniques are presented. It not only has the advantages of the dual-loop ring-VCO, but also shows a relatively small $K_{\rm vco}$. Direct frequency modulation (FM) in the ring oscillator is analyzed and then a switched capacitor array is introduced to conventional ring-VCO to lower the $K_{\rm vco}$. A lower $K_{\rm vco}$ means weaker direct FM modulation at the tuning node for the ring oscillator, as explained in Section 2. Furthermore, a two-dimensional MOM-capacitor with large capacitance density is adopted to make the ring oscillator completely compatible with standard CMOS processes.

2. VCO circuit design

2.1. Conventional delay cell analysis

The schematic of the conventional delay cell for the dual-loop ring VCO is shown in Fig. 1(a). In this circuit, NM1 and NM2 form the inputs of the primary loop, while PM1 and PM2 serve as the inputs of the secondary loop; the dual-loop technique increases the oscillation frequency of the ring VCO. A pair of PMOS load transistors PM3/PM4 constitutes a CMOS latch and the output voltage oscillates from rail to rail. This reduces the on-time of the transistors in the delay cell and the ring VCO exhibits low phase noise. Frequency fine tuning is achieved by transistors NM3 and NM4, which control the feedback strength of the latch. As $V_{\rm tune}$ increases, the latch becomes strong and resists the voltage switching in the differential delay cell. As a result, delay time is increased and oscillation frequency reduced. Figure 1(b) shows the equivalent circuit of Fig. 1(a) at gate level. The output amplitude and oscillation frequency of the dual-loop ring-VCO composed of the above delay cell can be expressed as[4]:

$$A_{\rm osc} = \frac{8}{\pi} R_{\rm o} \left(\frac{I_{\rm DC,\,in}}{\sqrt{2}} + I_{\rm DC,\,latch} \right), \tag{1}$$

$$\omega_{\rm osc} = \frac{1}{R_0 C_{\rm L}} \frac{\dfrac{I_{\rm DC,\,in}}{\sqrt{2}} + I_{\rm DC,\,aux}}{\dfrac{I_{\rm DC,\,in}}{\sqrt{2}} + I_{\rm DC,\,latch}}, \tag{2}$$

where $I_{\rm DC,\,in}$ is the current of the primary input transistor NM1/NM2, $I_{\rm DC,\,aux}$ is the current of the secondary input transistor PM1/PM2, and $I_{\rm DC,\,latch}$ is the current of the load transistor PM3/PM4. $R_0 C_{\rm L}$ is the time constant at the output node.

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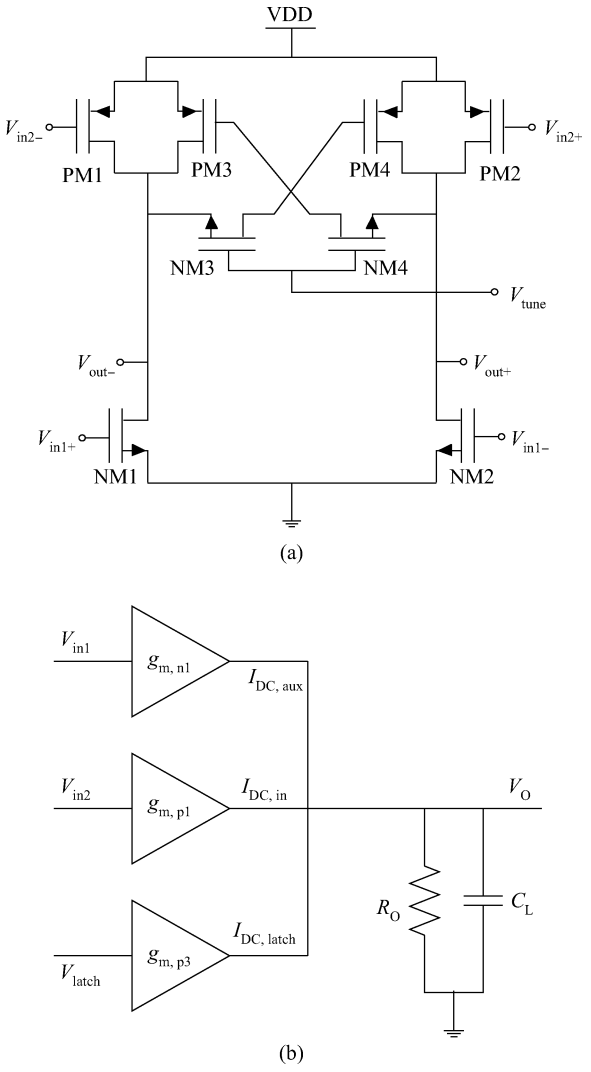


Fig. 1. (a) Circuit of the conventional delay cell. (b) The equivalent circuit of Fig. 1(a).

The drawback of the conventional delay cell in Fig. 1 is that the tuning voltage range is limited. The range in which the output frequency being sensitive to the tuning voltage corresponds to the transistor NM3 and NM4's status from cut-off to fully switched on. For the delay cell shown in Fig. 1(a), $V_{\rm tune}$ should be satisfied:

$$V_{\rm tune} > V_{\rm turn\text{-}on} = V_{\rm gs,\,NM3} + V_{\rm ds,\,NM1}. \tag{3}$$

Figure 2 shows the typical tuning curve of the conventional ring VCO. When $V_{\rm tune}$ is larger than the turn-on voltage, output frequency decreases linearly with $V_{\rm tune}$. When $V_{\rm tune}$ is smaller than the turn-on voltage, NM3/MN4 turn off and output frequency remains constant. This will result in a large $K_{\rm vco}$ if a certain tuning range is required. As the supply voltage decreases with the progress of the CMOS process, such as a 1.2 V supply voltage in a 65 nm CMOS process, the situation becomes worse.

A large $K_{\rm vco}$ means a strong frequency modulation (FM) effect by the noise at the tuning node on the output phase noise. Unlike the "AM-to-FM" effect in a varactor tuned oscillator[5], the noise at the tuning node directly changes the frequency of

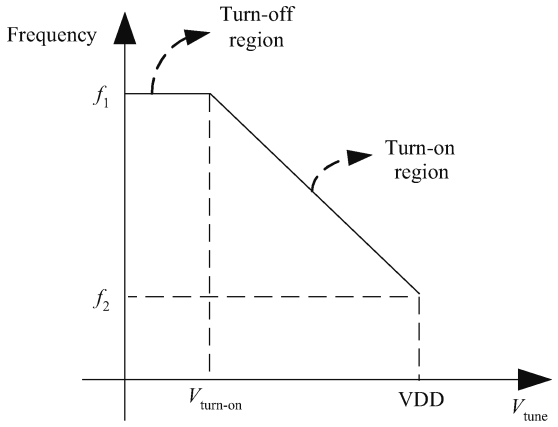


Fig. 2. Typical $V-F$ curve of conventional ring VCO.

the ring oscillator. Suppose a noise voltage $v_{\rm n}$ exists at the tuning node of the ring oscillator, it will influence the oscillation frequency:

$$\omega_{\rm osc}(V_{\rm tune}+v_{\rm n}) = \frac{1}{R_0C_{\rm L}}\frac{\dfrac{I_{\rm DC,\,in}}{\sqrt{2}}+I_{\rm DC,\,aux}}{\dfrac{I_{\rm DC,\,in}}{\sqrt{2}}+(I_{\rm DC,\,latch}+a_{\rm v}g_{\rm m,\,PM3}v_{\rm n})}, \tag{4}$$

where $a_{\rm v}$ denotes the voltage gain between the gate node and drain node of NM4. Based on the fact that $a_{\rm v}g_{\rm m,\,PM3}v_{\rm n}$ is much smaller than $I_{\rm DC,\,latch}$, the above equation can be simplified as:

$$\begin{aligned}\omega_{\rm osc}(V_{\rm tune}+v_{\rm n}) &= \frac{1}{R_0C_{\rm L}}\frac{\dfrac{I_{\rm DC,\,in}}{\sqrt{2}}+I_{\rm DC,\,aux}}{\dfrac{I_{\rm DC,\,in}}{\sqrt{2}}+I_{\rm DC,\,latch}}\\ &\quad\times\left(1-\frac{a_{\rm v}g_{\rm m,\,PM3}v_{\rm n}}{\dfrac{I_{\rm DC,\,in}}{\sqrt{2}}+I_{\rm DC,\,latch}}\right)\\ &= \omega_{\rm osc}(V_{\rm tune})-\frac{1}{R_0C_{\rm L}}\frac{\dfrac{I_{\rm DC,\,in}}{\sqrt{2}}+I_{\rm DC,\,aux}}{\left(\dfrac{I_{\rm DC,\,in}}{\sqrt{2}}+I_{\rm DC,\,latch}\right)^2}a_{\rm v}g_{\rm m,\,PM3}v_{\rm n}.\end{aligned} \tag{5}$$

From Eq. (1), the tuning gain of the ring oscillator can be expressed as:

$$\begin{aligned}K_{\rm vco} &= \frac{\partial\omega_{\rm osc}}{\partial V_{\rm tune}} = \frac{1}{R_0C_{\rm L}}\frac{\dfrac{I_{\rm DC,\,in}}{\sqrt{2}}+I_{\rm DC,\,aux}}{\left(\dfrac{I_{\rm DC,\,in}}{\sqrt{2}}+I_{\rm DC,\,latch}\right)^2}\frac{\partial I_{\rm DC,\,latch}}{\partial V_{\rm tune}}\\ &= \frac{1}{R_0C_{\rm L}}\frac{\dfrac{I_{\rm DC,\,in}}{\sqrt{2}}+I_{\rm DC,\,aux}}{\left(\dfrac{I_{\rm DC,\,in}}{\sqrt{2}}+I_{\rm DC,\,latch}\right)^2}a_{\rm v}g_{\rm m,\,PM3}.\end{aligned} \tag{6}$$

By combining Eqs. (5) and (6), the frequency deviation

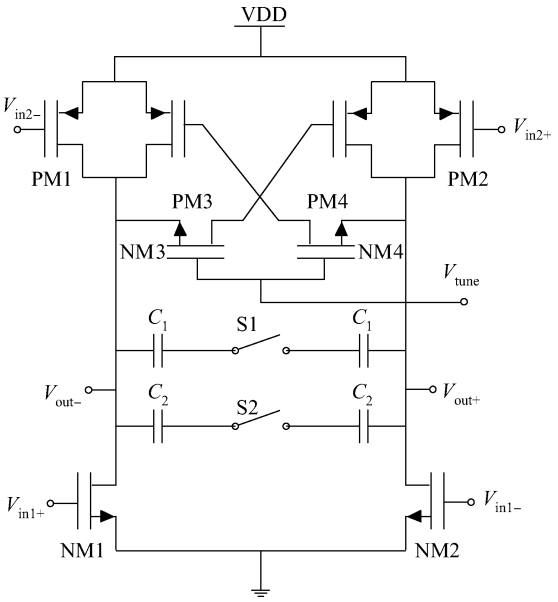


Fig. 3. Structure of the proposed delay cell.

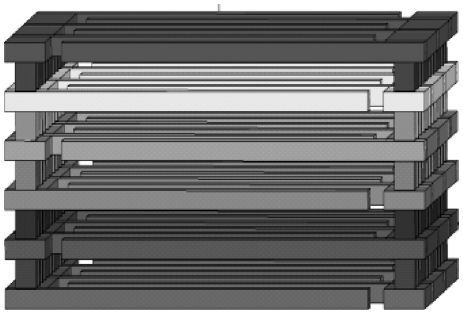


Fig. 4. Structure of the proposed MOM-capacitor.

caused by the noise at the tuning node can be expressed as:

$$\Delta\omega_{\rm osc}(v_{\rm n}) = K_{\rm vco}v_{\rm n}. \tag{7}$$

So as the tuning voltage range is limited, the increased $K_{\rm vco}$ will deteriorate the phase noise performance of the ring oscillator through a direct FM effect, as described by Eq. (7).

2.2. Delay cell with switched capacitor array

It can be seen from Eq. (1) that the oscillation frequency of the ring VCO not only depends on the current of the load transistors, but also on the RC constant at the output node. In order to achieve both wideband tuning and low $K_{\rm vco}$, switched capacitor array, which was adopted in wideband LC-VCO[6], is introduced to the ring VCO, as shown in Fig. 3.

C_1 and C_2 are switched capacitors controlled by digital signals S1 and S2, and coarse frequency tuning is achieved by the switched capacitors. By using this configuration, the tuning frequency range is divided into four sub-curves, each curve covers a certain tuning range and $K_{\rm vco}$ is reduced. A lower $K_{\rm vco}$ means less sensitivity to noise at the tuning node, from Eq. (7), and the phase noise is improved.

From Eq. (1), the value of the switched capacitor can be easily deduced, it should be:

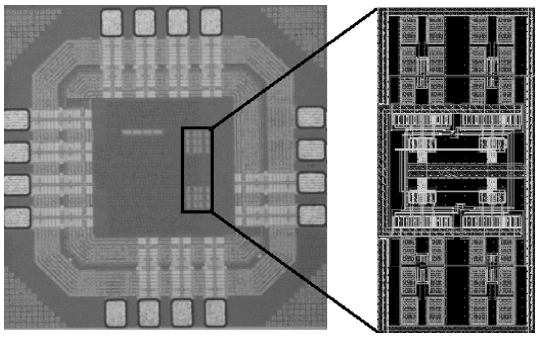


Fig. 5. Microphotograph of the fabricated ring VCO.

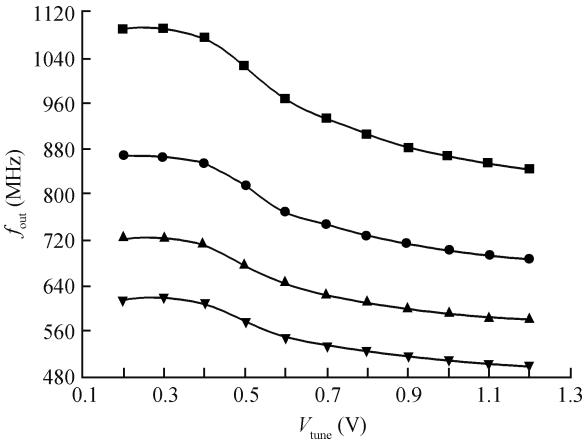


Fig. 6. The measured tuning curves of the proposed ring VCO.

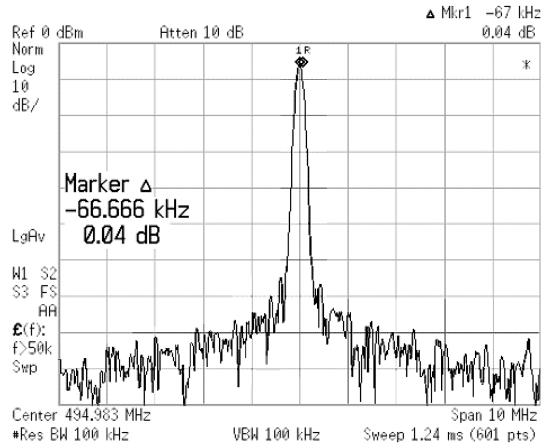
$$\Delta C = R_0 C_{\rm L}^2 \frac{\dfrac{I_{\rm DC,\,in}}{\sqrt{2}} + I_{\rm DC,\,latch}}{\dfrac{I_{\rm DC,\,in}}{\sqrt{2}} + I_{\rm DC,\,aux}} \Delta\omega_{\rm osc}, \tag{8}$$

where $\Delta\omega_{\rm osc}$ is the desired frequency gap between adjacent sub-curves, and $C_{\rm L}$ is the initial capacitance of the delay cell including the parasitic capacitor at the output node of the delay cell and the parasitic capacitor at the input node of the next delay cell.

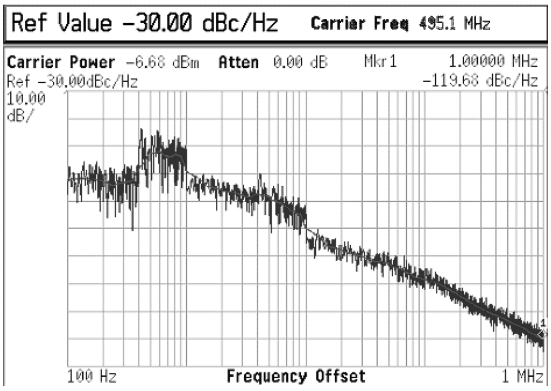
In the design of wideband LC-VCOs with switched capacitor arrays, a metal–insulator–metal (MIM) capacitor is often used since it provides high capacitance density and high $Q_{\rm C}$. The drawback of the MIM capacitor is that extra process steps are needed for the high-quality, very thin insulator, which cannot be integrated in standard CMOS processes. In fact, the ring VCO is often used as a high-speed clock generator in modern digital systems, so compatibility with standard CMOS processes is critical. A two-dimensional MOM capacitor with large capacitance density[7] is adopted to make the ring oscillator completely compatible with standard CMOS processes. Figure 4 shows the structure of the two-dimensional stacked MOM capacitor. Two patterned metals on one layer form an interdigitated capacitor in the horizontal direction. Capacitors formed on different metal layers can be connected in parallel to increase the capacitor density, forming a stacked MOM capacitor in the vertical direction. The metal strips on different metal layers can also form an interdigitated capacitor in the vertical

Table 1. Comparison with other ring oscillator designs.

Parameter	Topology	Frequency (MHz)	Phase noise (dBc/Hz)	Power (mW)	FOM (dBc/Hz)
Ref. [2]	Dual-loop	750–1200	–117 @ 600 kHz	30	–171
Ref. [8]	RC BPF	2250–2750	–95 @ 1 MHz	2.86	–159
Ref. [9]	Two tuning loop	7300–7860	–103 @ 1 MHz	60	–163
This work	Dual-loop with SCR	480–1100	–120 to –108 @ 1 MHz	3.84	–169



(a)



(b)

Fig. 7. The measured (a) output spectrum and (b) phase noise of the proposed ring VCO.

direction; such adjacent capacitors form a stacked MOM capacitor in the horizontal direction. A two-dimensional stacked MOM capacitor can be formed by combining the structure of the above two capacitors.

3. Implement and measurement results

A ring VCO with a four-stage proposed delay cell has been fabricated in a 65 nm standard CMOS process as part of the PLL circuit. The layout and microphotograph of the fabricated VCO are shown in Fig. 5 with a core area of about 176 × 84 μm^2. The VCO core consumes 3.84 mW from a 1.2 V supply. The measured tuning curves are shown in Fig. 6. Four subcurves cover a frequency range from 480 to 1100 MHz, resulting in a tuning range of 78%. The $K_{\rm vco}$ is –175 MHz/V at $V_{\rm tune}$ = 0.6 V and $S_2S_1 = 00$. The measured output spectrum and the phase noise curve at 495 MHz are shown in Fig. 7; the phase noise is –120 dBc/Hz @ 1 MHz.

In order to evaluate the performance of the designed ring VCO, we use the well-known figure-of-merit (FOM) defined as:

$$\mathrm{FOM} = L(\Delta f) - 20\lg\frac{f_0}{\Delta f} + 10\lg\frac{P}{1\,\mathrm{mW}}. \qquad (9)$$

The resulting FOM of the designed ring VCO is −169 dBc/Hz.

Table 1 illustrates the performances of the proposed ring VCO compared with those of recently reported wideband VCOs. As shown in Table 1, the present work achieves very low phase noise while maintaining a wide tuning range. A lower FOM was achieved compared with that of other ring VCOs.

4. Conclusion

A wideband low-phase-noise ring oscillator was implemented in a 65 nm standard CMOS process. A switched capacitor array based on a high density MOM capacitor was used to reduce the ring VCO's tuning sensitivity without impairing the tuning range. The measured operation frequency of the ring VCO ranged from 480 to 1100 MHz, the phase noise of the ring VCO ranged from –108 to –120 dBc/Hz at 1 MHz offset. The VCO core consumed 3.84 mW from a 1.2 V supply voltage, and the corresponding FOM is –169 dBc/Hz at 495 MHz output. The designed ring VCO is well suitable for clock generation in high-speed digital systems.

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