A high linearity downconverter for SAW-less LTE receivers*

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Abstract: This paper presents a high linearity downconverter implemented in a 0.18 μm CMOS process for long term evolution (LTE) receivers without a surface acoustic wave (SAW) filter. The proposed downconverter is composed of a transconductance (G_m) stage, a passive mixer, a current buffer, a transimpedance (TIA) stage, and a DC-offset cancellation (DCOC) loop. The current buffer is utilized to provide very low load impedance for the passive mixer at high frequencies and reduce the output voltage swing induced by out-of-band blockers. This technique improves the input referred third-order intercept point (IIP3) and second-order intercept point (IIP2) of the downconverter by 4.5 dB and 11 dB, respectively. The measured results show that the proposed downconverter achieves a voltage conversion gain of 29.5 dB, double sideband noise figure of 12.7 dB, out-of-band IIP3 of 13 dBm and IIP2 of more than 62 dBm.

Key words: linearity; downconverter; long term evolution (LTE); passive mixer; radio-frequency (RF) receivers
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1. Introduction

In communication systems such as wideband code division multiple access (WCDMA) and frequency division duplexing (FDD) long term evolution (LTE), the transmitted (Tx) power leakage to the receivers, caused by the finite duplexer isolation, results in a stringent out-of-band linearity requirement in the receivers[1]. In the receiver, the desired radio-frequency (RF) signal and the Tx leakage blocker are amplified simultaneously by the low noise amplifier (LNA) and fed into the downconverter. The distortions, mainly the second-order intermodulation distortion (IMD2) and the third-order intermodulation distortion (IMD3) generated by the Tx leakage blocker due to downconverter nonlinearities, might deteriorate the desired RF signal. An off-chip surface acoustic wave (SAW) filter can be inserted between the LNA and the downconverter to suppress the Tx leakage blocker and relieve the linearity requirement of the downconverter. However, inserting a SAW filter increases design complexity and the system cost.

A downconverter usually consists of a transconductance (G_m) stage for voltage-to-current conversion, a mixer for frequency down-conversion, and a transimpedance amplifier (TIA) for current to voltage conversion, as shown in Fig. 1. For better linearity performance of the downconverter, a current commutating passive mixer is usually preferred to an active mixer[1−3]. In addition, in order to ease the linearity requirement for the TIA in the presence of the Tx leakage blocker, large capacitances are usually placed after the mixer to form a low frequency pole and suppress the down-converted out-of-band blocker at the TIA input[1−3]. However, these capacitors usually consume considerable silicon area, especially in the scenario that the Tx leakage is close to the receive band. Furthermore, this pole has to be pushed higher for large signal bandwidths, even if silicon area is not an issue. For example, in the case of LTE receivers, where the received signal bandwidth is 20 MHz and the Tx leakage is only 120 MHz apart from the receive band (LTE Band VII[4]), it is impossible to achieve adequate attenuation of the Tx leakage blocker before the TIA using only the capacitor filtering technique.

This paper presents the design and implementation of a high gain, low noise, and high linearity downconverter operating at a frequency of 2.62 GHz for LTE application. The proposed downconverter consists of a G_m stage, a passive mixer with a modified current buffer, and a TIA/biquad filter and achieves better conversion gain, out-of-band attenuation, and linearity.

2. Linearity analysis

2.1. Conventional downconverter

Assuming the LNA before the downconverter has a 15 dB voltage gain, the required out-of-band linearity of this downconverter is 11 dBm input referred third-order intercept point (IIP3) and 60 dBm input referred second-order intercept point (IIP2) for the SAW-less receiver application[4, 5]. These requirements are difficult, if not impossible, to meet for conventional downconverter design, even using a passive mixer which has higher linearity than active one.

In a conventional passive downconverter, as shown in Fig. 1, the G_m stage generates the intermodulation distortion due to its non-ideal voltage-to-current (V–I) conversion. The small current output from the G_m stage can be expressed in the Taylor series expansion:

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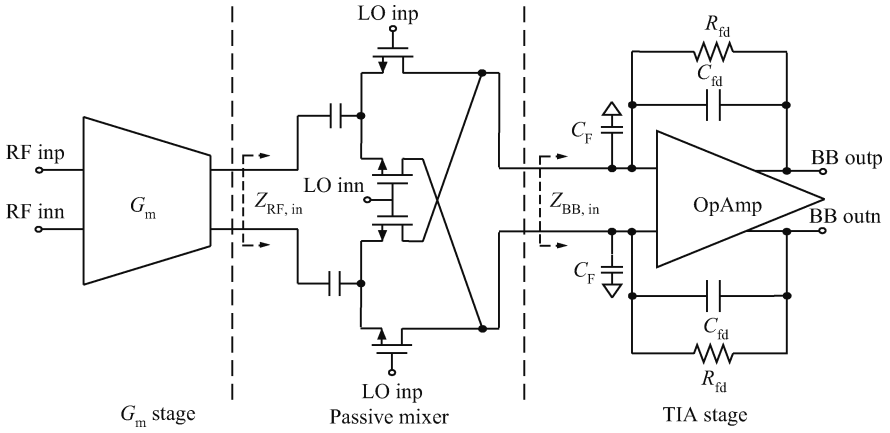

Fig. 1. Block diagram of a conventional passive downconverter.

$$\begin{aligned} i_{ds}(v_{gs}, v_{ds}) = {} & g_m v_{gs} + g_d v_{ds} + g_{m2} v_{gs}^2 \\ & + g_{md} v_{gs} v_{ds} + g_{d2} v_{ds}^2 + g_{m3} v_{gs}^3 \\ & + g_{m2d} v_{gs}^2 v_{ds} + g_{md2} v_{gs} v_{ds}^2 + g_{d3} v_{ds}^3 + \cdots , \end{aligned} \tag{1}$$

where v_{gs} is the input voltage swing, v_{ds} is the output voltage swing, g_m, g_{m2}, g_{m3} are transconductance terms, g_d, g_{d2}, g_{d3} are output conductance terms, and g_{md}, g_{m2d}, g_{md2} are cross-modulation terms that can not be ignored, especially in a deep sub-micron CMOS process. As shown in Eq. (1), in order to achieve less distortion in the G_m stage, the output voltage swing v_{ds} should be reduced and thus the input impedance of the passive mixer, i.e., the load of G_m stage, should be reduced to avoid a large v_{ds} caused by the Tx leakage blocker. The input impedance of the passive mixer, $Z_{RF, in}$, can be defined by[6]:

$$Z_{RF, in}(\omega_{TX}) \approx Z_{SW} + \frac{4}{\pi^2} Z^*_{BB, in}(\omega_{LO} - \omega_{TX}), \tag{2}$$

where Z_{SW} is the switch resistance and $Z_{BB, in}$ is the input impedance of baseband circuits, as illustrated in Fig. 1. $Z_{RF, in}$ at Tx frequency is in proportion to Z_{SW} and $Z_{BB, in}$ at duplex frequency ($\omega_{LO} - \omega_{TX}$) as shown in Eq. (2) and hence low $Z_{BB, in}$ at duplex frequency is highly desirable for less distortion in the G_m stage. Furthermore, low $Z_{BB, in}$ also improves the linearity of a passive mixer[6].

It is well-known that the limited open-loop gain of an operational amplifier (opamp) causes the input impedance of the TIA to increase with frequency. A large size capacitance C_F is usually added at the TIA input to generate low input impedance at high frequencies. The input impedance of a TIA with a large C_F is given by:

$$Z_{BB, in}(\omega) = \frac{Z_{fd}(\omega)}{1 + A(\omega)} || \frac{1}{j\omega C_F}, \quad Z_{fd}(\omega) = R_{fd} || \frac{1}{j\omega C_{fd}}, \tag{3}$$

where $Z_{fd}(\omega)$ is the feedback impedance of a TIA and $A(\omega)$ is the open-loop gain of the opamp. Assuming 3 kΩ R_{fd} and 4 pF C_{fd}, the simulated $Z_{BB, in}$ with three different values of C_F for a typical TIA is shown in Fig. 2. A practical two-stage opamp is utilized in the impedance simulation and the simulated frequency response of $Z_{BB, in}$ can be separated into three

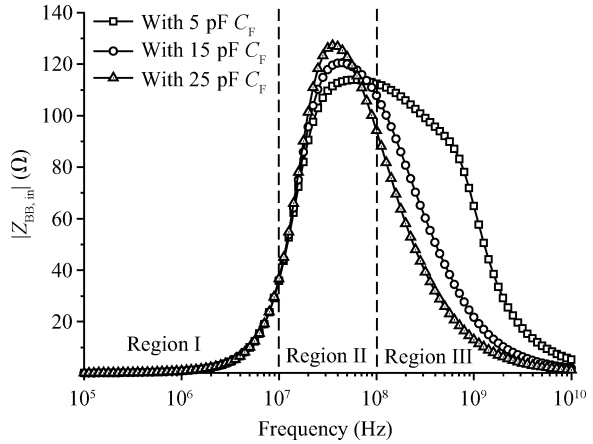

Fig. 2. Simulated $Z_{BB, in}$ with different values of C_F.

regions, as shown in Fig. 2. In region I, where the open-loop gain of opamp is large at low frequencies, the desirable low input impedance is achieved. As the frequency increases in region II, the limited bandwidth of $A(\omega)$ results in the increase of $Z_{BB, in}$. Owing to the low pass feature of $Z_{fd}(\omega)$, $Z_{BB, in}$ finally flattens out in region II. As the frequency continues to increase in region III, C_F becomes dominant and reduces $Z_{BB,in}$ back to a low value. However, as shown in Fig. 2, the input impedance $Z_{BB, in}$ is still relatively large at the duplex frequency of 120 MHz even using a large C_F of 25 pF.

2.2. Proposed downconverter

The proposed downconverter is shown in Fig. 3. Instead of adding large capacitance at the TIA input, a current buffer (CB) is inserted between the passive mixer and the TIA in order to minimize $Z_{BB, in}$. The current buffer based on a common gate stage[7, 8] employs a local negative feedback loop to keep low input impedance at high frequencies. With the current buffer, the input impedance of baseband circuits, $Z'_{BB, in}$, is given by:

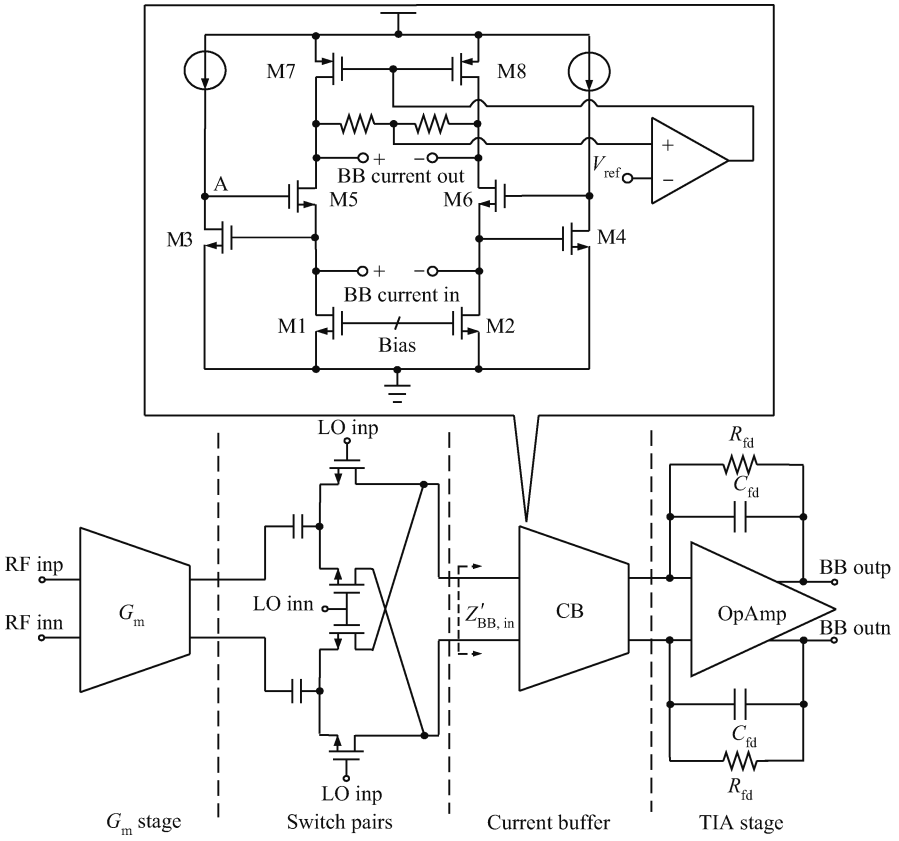

Fig. 3. Proposed downconverter with a current buffer.

$$Z'_{\mathrm{BB,\,in}}(\omega) \approx \left(\frac{1}{g_{\mathrm{m3}} g_{\mathrm{m5}} \left(r_{\mathrm{o3}} \| \dfrac{1}{\mathrm{j}\omega C_{\mathrm{A}}} \right)} \| \frac{1}{\mathrm{j}\omega C_{\mathrm{gs3}}} \right) \times 2$$

$$\approx \left(\frac{1 + \mathrm{j}\omega r_{\mathrm{o3}} C_{\mathrm{A}}}{g_{\mathrm{m3}} g_{\mathrm{m5}} r_{\mathrm{o3}}} \| \frac{1}{\mathrm{j}\omega C_{\mathrm{gs3}}} \right) \times 2, \qquad (4)$$

where g_{m3} and g_{m5} are the transconductance of M3 and M5, respectively, and r_{o3} is the output resistance of M3. C_{A} which represents the total parasitic capacitor at node A (as shown in Fig. 3) determines the high pass corner frequency of $Z'_{\mathrm{BB,\,in}}$ and hence needs to be minimized. Thanks to the wide bandwidth of the local feedback loop in the current buffer, $Z'_{\mathrm{BB,\,in}}$ below 30 Ω can be achieved up to 300 MHz. With identical R_{fd}, C_{fd}, and the opamp mentioned in the $Z_{\mathrm{BB,\,in}}$ simulation, the simulated $Z'_{\mathrm{BB,\,in}}$ is shown in Fig. 4. Compared with $Z_{\mathrm{BB,\,in}}$ in the conventional downconverter as shown in Fig. 2, the proposed downconverter demonstrates a much smaller $Z'_{\mathrm{BB,\,in}}$ at the duplex frequency and thus better linearity performance in the G_{m} stage and the passive mixer can be achieved.

In contrast to current buffers that only employ a common gate stage[7, 8], the proposed structure has two advantages. In Refs. [7, 8], for lower input impedance of the current buffer, the transconductance of the common gate transistor has to be increased. But a larger transconductance induces a larger noise contribution. By using the negative feedback loop, $Z'_{\mathrm{BB,\,in}}$ can be reduced by increasing the transconductance of M5 but not M3 without any additional noise contribution. In addition, I–V conversion is carried out at the output nodes in the buffer in Refs. [7, 8]. A large voltage swing can be generated by the out-of-band blocker. This harms the linearity due to the limited headroom in a low supply voltage CMOS process. In our scheme, the TIA following the buffer converts AC current to voltage mode. There is no large voltage swing at the buffer's output. Therefore, in comparison with the conventional common gate stage, the proposed structure is beneficial to both the noise and the linearity.

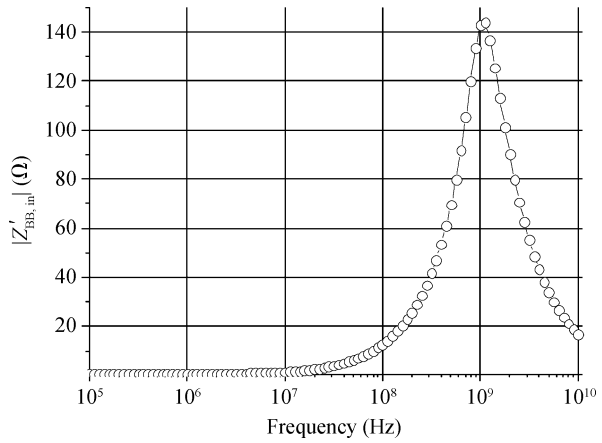

Fig. 4. Simulated $Z'_{\mathrm{BB,\,in}}$ in the proposed downconverter.

3. Circuit implementations

The detailed circuit implementation of the proposed down-

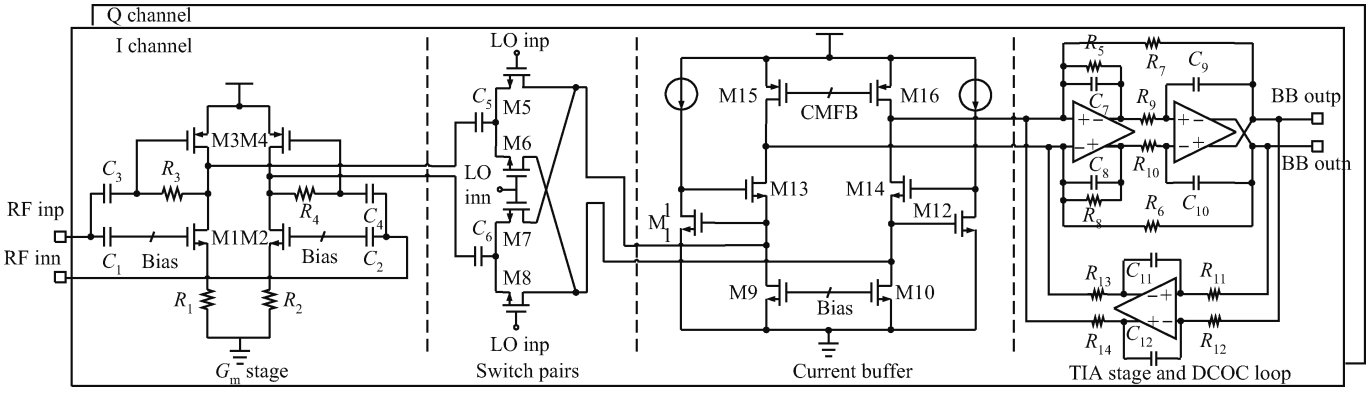

Fig. 5. Detailed circuit implementation of the proposed downconverter.

converter is illustrated in Fig. 5, which does not include the bias circuit for simplicity. In the G_m stage, a current reuse technique is adopted to improve the gain and noise performance. The G_m stage also employs the resistive degeneration to improve its linearity. In consideration of the current efficiency, the degeneration resistors are adopted with NMOS transistors but without PMOS transistors. The diode connection of the PMOS transistors in the G_m stage simplifies the bias circuitry design.

The voltage conversion gain of the proposed downconverter for the in-band signal can be expressed by:

$$\text{Conversion\_Gain} = \frac{2}{\pi} G_m R_5; \quad G_m = g_{m,3} + \frac{g_{m,1}}{1 + g_{m,1} R_1}, \tag{5}$$

where R_1 and R_5 are illustrated in Fig. 5, $g_{m,1}$ and $g_{m,3}$ are the transconductance of M1 and M3, respectively, and G_m is the total transconductance of the G_m stage. To achieve a wide dynamic range, both the low gain mode and the high gain mode are implemented by adjusting the value of R_5. The whole G_m stage dissipates 2.5 mA from a 1.8 V power supply.

The TIA employs a Tow–Thomas biquad filter with an AC input. This topology is becoming increasingly popular due to its easier filter corner tuning, lower filter peaking, and better group delay in comparison with a conventional integrator followed by a biquad[2, 9]. The cutoff frequency of the filter is set to 13 MHz to accommodate the down-converted LTE signal (20 MHz signal bandwidth). An analog DC-offset cancellation (DCOC) loop is also implemented to prevent the circuits from saturation and suppress the flicker noise from the current buffer and the TIA. The opamp in the filter employs a conventional two-stage Miller-compensated amplifier structure. The gain-bandwidth product (GBW) of the opamp is designed to be larger than 300 MHz to reduce its effect on the cutoff frequency of the filter.

The noise of baseband circuits is mostly contributed from the transistors in the current buffer and the first opamp in the biquad filter. Figure 6 illustrates a simplified circuitry for noise analysis. R_S in Fig. 6 is the equivalent switch pair output resistance[3]. Owing to the appearance of R_S, the common gate transistor M13 adds noise current to $I_{n\_CB,\,out}$. The output noise V_{n_out} and the input referred noise V_{n_in} of the baseband circuits can be expressed as:

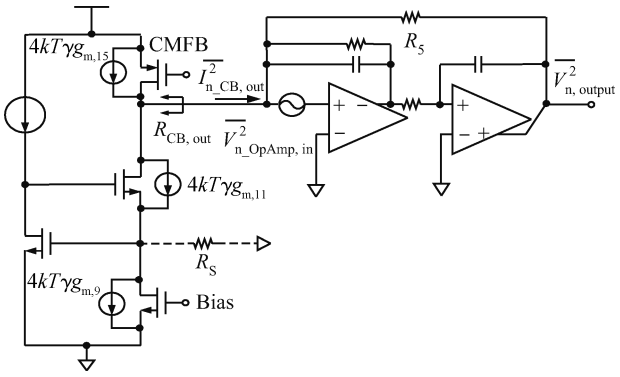

Fig. 6. Simplified baseband circuits for noise analysis.

$$V^2_{n,\,out} = I^2_{n\text{-}CB,out} \times R_5^2 + V^2_{n\text{-}Amp,in} \times \left(1 + \frac{R_5}{R_{CB,\,out}}\right)^2 + 4kTR_5,$$
$$V^2_{n,\,in} \approx \frac{\pi^2}{4} \times \frac{I^2_{n\_CB,\,out} + V^2_{n\_Amp,\,in}/R^2_{CB,\,out}}{G_m^2}, \tag{6}$$

where k is the Boltzmann constant, $R_{CB,\,out}$ is the output resistance of current buffer, $I_{n\_CB,\,out}$ is the output noise current of the current buffer and mostly contributed from the thermal noise of M9, M13, and M15, and $V_{n\_Amp,\,in}$ is the input referred noise voltage of the first opamp in the biquad filter. It can be seen from Eq. (6) that $I_{n\_CB,\,out}$ dominates the noise contribution because $R_{CB,\,out}$ is large enough to neglect $V_{n\_Amp,\,in}$. Since the current through M13 is proportional to $I_{n\_CB,\,out}$ and inversely proportional to $Z'_{BB,\,in}$, there is a trade-off between the noise contribution and the linearity. However, as mentioned in the previous section, a small value of $Z'_{BB,\,in}$ can be achieved by using a negative feedback loop without increasing the current through M13. Therefore, by carefully choosing the transistor size and the bias current, there is no degradation of noise performance in this proposed structure. The current consumption of the current buffer is 1.6 mA.

It is worthwhile mentioning here that the proposed downconverter does not need additional local oscillator (LO) signals, which usually consume a fairly large amount of power. This is an advantage compared with the downconverters proposed in

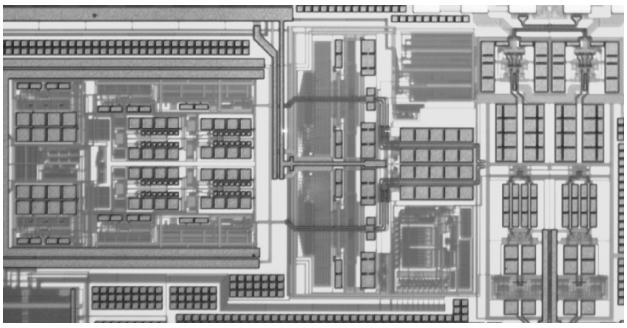

Fig. 7. Chip photograph of the proposed downconverter.

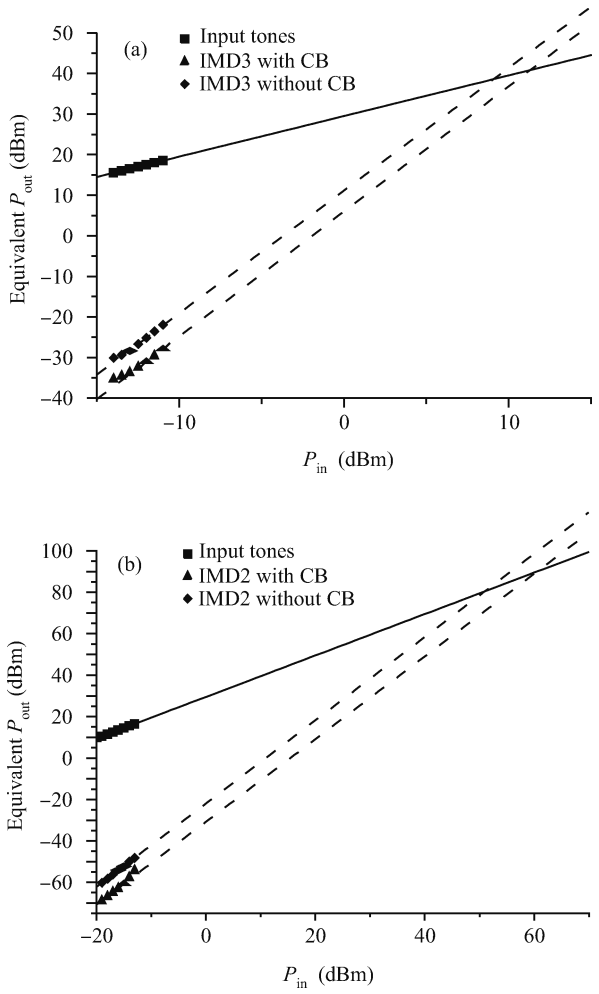

Fig. 8. Measured out-of-band (a) IIP3 and (b) IIP2 with/without the current buffer.

Refs. [10–12].

4. Measurement results

The proposed downconverter with a modified current buffer is fabricated in a 0.18 μm CMOS process. The whole downconverter occupies a silicon area of 700 × 410 μm^2, as shown in Fig. 7, and it consumes a total current of 20 mA from a 1.8 V power supply for both I and Q paths. For fair comparison, a conventional downconverter with identical circuits, except for the current buffer which is replaced with a 10 pF C_F

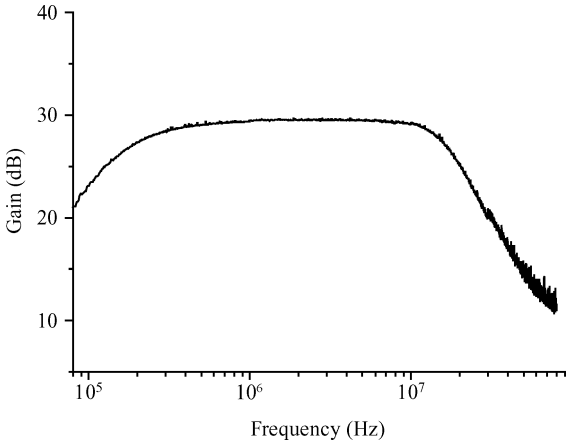

Fig. 9. Measured transfer function.

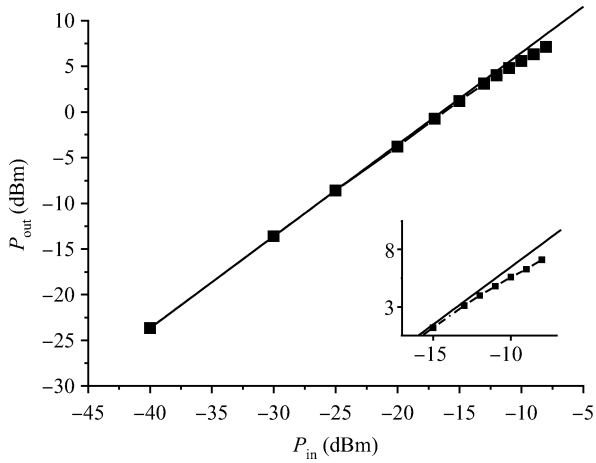

Fig. 10. Measured 1-dB-ICP at low gain mode.

to generate low impedance at the duplex frequency, is also designed and fabricated. An off-chip 50 Ω resistor followed by a balun is placed at the RF input for impedance matching and single-to-differential conversion. The noise figure degradation due to the off-chip resistor and balun insertion loss is calibrated out in the measurements.

Figure 8(a) shows the measured out-of-band IIP3 for both downconverters. Measured with two input tones at 61.5 MHz and 120 MHz frequency offset from the LO, the proposed downconverter with the current buffer demonstrates an out-of-band IIP3 of 13 dBm while the conventional downconverter with a capacitor demonstrates an out-of-band IIP3 of about 4.5 dB worse. Figure 8(b) shows the measured minimum out-of-band IIP2 from 5 chips using two input tones at 120 MHz and 121.5 MHz frequency offset from the LO. Without using IIP2 calibration, an out-of-band IIP2 of 62 dBm at minimum is observed for the proposed downconverter with the current buffer, an improvement of 11 dB compared with the conventional downconverter with a capacitor. The measured transfer function of the proposed downconverter at high gain mode is shown in Fig. 9 and the in-band amplitude ripple is less than 0.5 dB from 0.5 to 10 MHz. The in-band input referred 1dB compression point (1-dB-ICP) is measured at low gain mode and –9 dBm is achieved, as shown in Fig. 10.

Table 1. Correspondence value of MCy and yield.

Parameter	Ref. [3]	Ref. [13]	This work	
			Proposed	Conventional
Process (μm)	0.18	0.13	0.18	0.18
RF-in frequency (GHz)	1.55–2.3	0.7–2.5	2.62	2.62
Signal BW (MHz)	1.23	0.5	20	20
Power (mW)	10 (G_m + OpAmp)	30–36* (G_m + divider + OpAmp)	36 (G_m + CB + BiQuad)	30 (G_m + BiQuad)
Conversion gain (dB)	22.5–25	34.5–35.5	High: 29.5 Low: 16.4	High: 29.3 Low: 16.1
DSB NF (dB)	7.7–9.5	9.5–11.5	12.7	12.8
In band 1-dB-ICP (dBm)	–12	–13.5	–9	–8.7
Out of band IIP3 (dBm)	>7	11	13	8.5
Out of band IIP2 (dBm)	>60	>60	62	51

* 36 mW at 2.5 GHz.

The measured performance of the proposed downconverter and the conventional downconverter is summarized in Table 1. Performance comparison with a state-of-the-art downconverter is also shown. As can be seen from Table 1, the proposed downconverter shows better linearity performance than that reported in Refs. [3, 13]. The larger power consumption of the proposed downconverter is mainly caused by larger signal bandwidth and the fully-functional biquad filter (usually absent or incomplete in other reported downconverters).

5. Conclusion

A high linearity downconverter for SAW-less LTE receivers has been proposed and implemented in a 0.18 μm CMOS process. Instead of using a large capacitor after the passive mixer, a modified current buffer with negative local feedback loop is utilized to generate very low load impedance at the duplex frequency for the passive mixer and thus improve the linearity performance. Compared with a conventional downconverter design, the proposed downconverter demonstrates an improvement of 4.5 dB in out-of-band IIP3 and 11 dB in out-of-band IIP2, respectively.

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